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Introduction

The goal of this book is to give the reader a good understanding of the basic principles of digital and analog electronic circuits. The book emphasizes the application and design of integrated circuits; however, circuit design is most effective when it is carried out with a view toward the overall design process—as well as the particular system of which the circuit is to be a part. Therefore, this first chapter presents an overview of electronic systems, a general discussion of the steps in their design, and basic concepts related to digital systems and electronic amplifiers.

Electronic-circuit design is fun. You can earn a good living from it and impress many people to whom electronics seems like magic. Learning the material in this book is an important step toward a rewarding career as a designer of electronic systems.

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1.1 ELECTRONIC SYSTEMS

Some electronic systems are familiar from everyday life. For example, we encounter radios, televisions, telephones, and computers on a daily basis. Other electronic systems are present in daily life, but are less obvious. Electronic systems control fuel mixture and ignition timing to maximize performance and minimize undesirable emissions from automobile engines. Electronics in weather satellites provide us with a continuous detailed picture of our planet.

Still other systems are even less familiar. For example, a system of satellites known as the **Global Positioning System (GPS)** has been developed by the United States to provide three-dimensional positional information for ships and aircraft anywhere on earth to an accuracy of several tens of meters. This is possible because signals emitted by several satellites can be received by the vehicle. By comparing the time of arrival of the signals and by using certain information contained in the received signals concerning the orbits of the satellites, the position of the vehicle can be determined. In addition, the received signals can be processed to set a local clock to an accuracy of about 100 ns.

Other electronic systems include the air-traffic control system, various radars, compact-disc recording equipment and players, two-way radios for police and marine communication, satellites that relay television and other signals from geosynchronous orbit, electronic instrumentation, manufacturing control systems, computerized monitors for patients in intensive care units, and navigation systems.

Electronic-System Block Diagrams

Electronic systems are composed of subsystems or functional blocks. These functional blocks can be categorized as **amplifiers, filters, signal sources, wave-shaping circuits, digital logic functions, digital memories, power supplies, and converters**. Briefly, we can say that amplifiers increase the power level of weak signals, filters separate desired signals from undesired signals and noise, signal sources generate waveforms such as sinusoids or square waves, wave-shaping circuits change one waveform into another (sinusoid to square wave, for example), digital logic functions process digital signals, memories store information in digital form, power supplies provide necessary dc power to the other functional blocks, and converters change signals from analog form to digital form or vice versa. Later in this chapter, we consider the external characteristics of amplifiers in some detail.

The block diagram of an AM radio is shown in Figure 1.1. Notice that there are three amplifiers and two filters. The local oscillator is an example of a signal source, and the peak detector is a special type of wave-shaping circuit. Digital circuits appear in the user interface (keypad and display) and in the frequency synthesizer. The digital circuits control channel selection and other functions, such as loudness. The complete system description would include detailed specifications for each block. For example, the gain, input impedance, and bandwidth of each amplifier would be given. (We will carefully define these terms later.) Each functional block in turn consists of a circuit composed of resistors, capacitors, inductors, transistors, integrated circuits, and other devices.

Functional blocks of electronic systems include amplifiers, filters, signal sources, wave-shaping circuits, digital logic functions, power supplies, and converters.

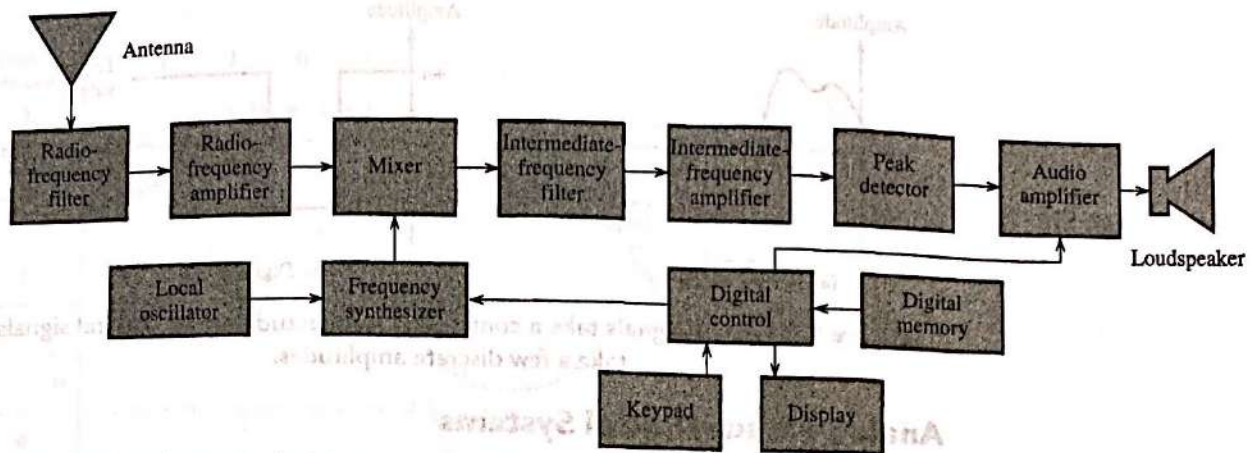


Figure 1.1 Block diagram of a simple electronic system: an AM radio.

The main goal of this book is to give you the basic skills needed to start from the external specifications of a block, such as an amplifier, and to design a practical circuit that meets the desired specifications. The selection of appropriate block diagrams for complex electronic systems is covered in other courses, such as control systems, computer architecture, digital signal processing, or communication systems.

The main goal of this book is to give you the basic skills needed to start from the external specifications of a block, such as an amplifier, and to design a practical circuit that meets the desired specifications.

Information Processing Versus Power Electronics

Many electronic systems fall into one or more of these categories: digital signal-processing systems, communication systems, medical electronics, instrumentation, control systems, and computer systems. A unifying aspect of these categories is that they all involve the collection and processing of information-bearing signals. Thus, the primary concern of many electronic systems is to extract, store, transport, or process the information in a signal.

Often, systems are also required to deliver substantial power to an output device. Certainly, this is true in an audio system, for which power must be delivered to loudspeakers to produce the desired sound level. In a control system for automatic positioning of a communication satellite, information extracted from various sources is used to control small rocket motors that maintain the satellite in its proper position and orientation. A cardiac pacemaker uses information extracted from the electrical signals produced by the heart to determine when to apply a stimulus in the form of a minute pulse of electricity to ensure proper pumping action. Although the output power of a pacemaker is very small, it is very important to consider the efficiency of its circuits to ensure a long life for the battery.

Some electronic systems are concerned mainly with the power content of signals, rather than information. For example, we might want a system to deliver ac electrical power (converted from dc supplied by batteries) to a computer, even when the ac line power fails.

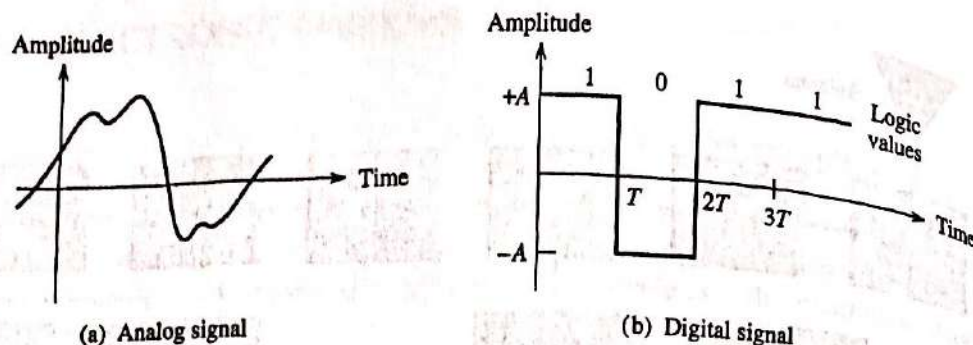


Figure 1.2 Analog signals take a continuum of amplitude values. Digital signals take a few discrete amplitudes.

Analog Versus Digital Systems

Information-bearing signals can be either analog or digital.

Information-bearing signals can be either **analog** or **digital**. An analog signal takes on a continuous range of amplitude values. The amplitude of a typical analog signal is plotted against time in Figure 1.2 (a). Notice that as time increases, the amplitude of the signal varies over a continuous range. On the other hand, a digital signal takes on a finite number of amplitudes. Often, digital signals are binary (i.e., there are only two possible amplitudes); however, more levels are sometimes useful. Frequently, digital signals change amplitude only at uniformly spaced points in time. An example of a digital signal is shown in Figure 1.2 (b).

The signals originally presented to the input of an electronic system by a **transducer** are usually in analog form. (A transducer is a device that converts energy to, or from, electrical form.) Examples of analog signals are sounds converted to electrical signals by a microphone, television signals, seismic vibrations, the output of a temperature transducer in a steam turbine, and so on. Other signals, such as the output of a computer keyboard, originate in digital form.

Conversion of Signals from Analog to Digital Form

Analog signals can be converted to digital form by a two-step process. First, the analog signal is sampled (i.e., measured) at periodic points in time. Then, a code word is assigned to represent the approximate value of each sample. Usually, the code words consist of binary symbols. This process is illustrated in Figure 1.3. Each sample value is represented by a 3-bit code word corresponding to the amplitude zone into which the sample falls. Thus, each sample value is converted into a code word, which in turn can be represented by a digital waveform, as shown in the figure. A circuit for the conversion of signals in this manner is called an **analog-to-digital converter (ADC)**. Conversely, a **digital-to-analog converter (DAC)** converts digital signals back to analog form. (Later in the book, we discuss the design of both types of converters.)

The rate at which a signal must be sampled depends on the frequency content of the signal. (Signals can be considered to consist of sinusoidal components having various frequencies, amplitudes, and phases. Fourier analysis is a branch of mathematics that deals with this representation of signals. No doubt, you have had, or will have, other courses dealing with Fourier theory. We consider the frequency content of signals later in this chapter, but not on a rigorous mathematical basis.) If a signal contains no components

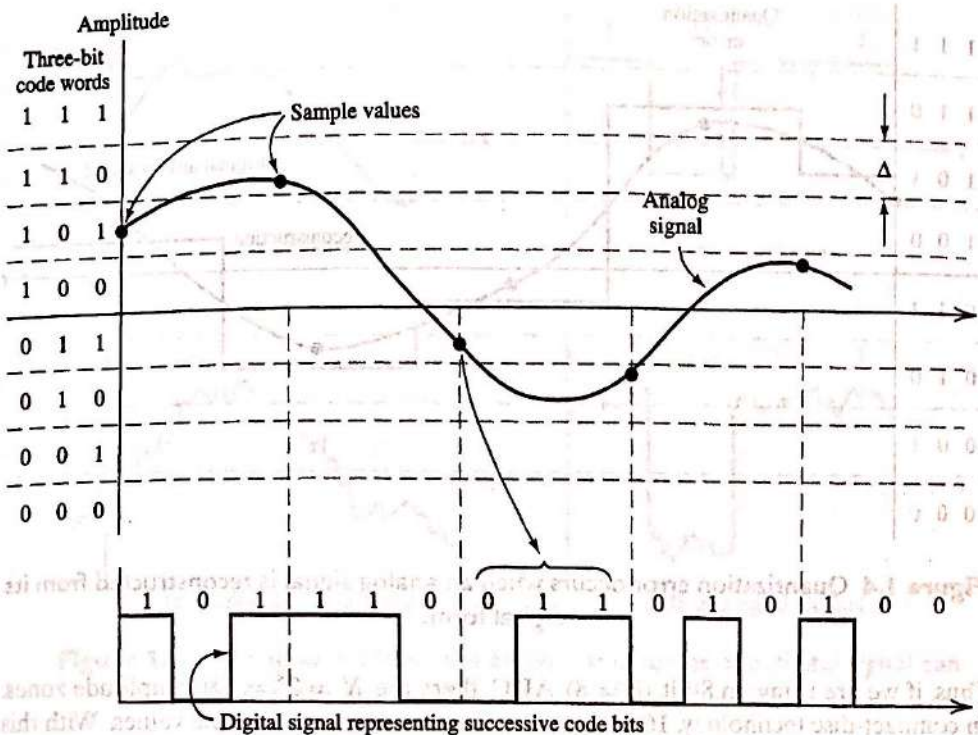


Figure 1.3 An analog signal is converted to an approximate digital equivalent by sampling. Each sample value is represented by a 3-bit code word. (Practical converters use longer code words.)

with frequencies higher than f_H , the signal can be exactly reconstructed from its samples, provided that the sampling rate is selected to be more than twice f_H . For example, audio signals have a highest frequency of about 15 kHz. Therefore, the minimum sampling rate that should be used for audio signals is 30 kHz. Practical considerations dictate a sampling frequency somewhat higher than the theoretical minimum. For instance, audio compact-disc technology converts audio signals to digital form with a sampling rate of 44.1 kHz. Naturally, it is desirable to use the lowest practical sampling rate to minimize the amount of data (in the form of code words) that must be stored or manipulated.

Another consideration that is important in converting analog signals to digital form is the number of amplitude zones to be used. Exact signal amplitudes cannot be represented, because all amplitudes falling into a given zone have the same code word. Thus, when a DAC converts the code words to form the original analog waveform, it is possible to reconstruct only an approximation to the original signal—the reconstructed voltage is in the middle of each zone. This is illustrated in Figure 1.4. Consequently, some **quantization error** exists between the original signal and the reconstruction. This error can be reduced by using a larger number of zones, which requires a longer code word for each sample. The number N of amplitude zones is related to the number k of bits in a code word by

$$N = 2^k \quad (1.1)$$

If a signal contains no components with frequencies higher than f_H , the signal can be exactly reconstructed from its samples, provided that the sampling rate is selected to be more than twice f_H .

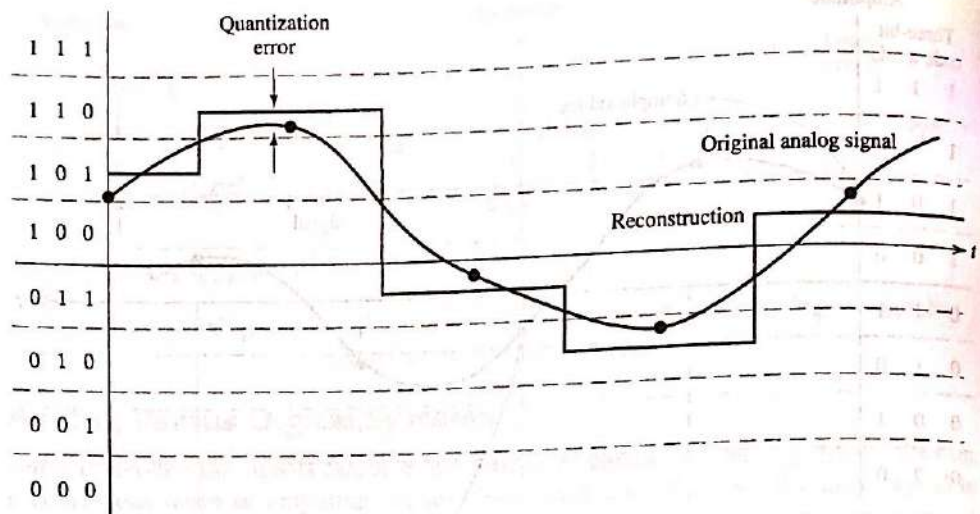


Figure 1.4 Quantization error occurs when an analog signal is reconstructed from its digital form.

Thus, if we are using an 8-bit ($k = 8$) ADC, there are $N = 2^8 = 256$ amplitude zones. In compact-disc technology, 16-bit words are used to represent sample values. With this number of bits, it is very difficult for a listener to detect the effects of quantization error on the reconstructed audio signal.

An electronic system that processes signals in analog form is called an analog system. Similarly, a digital system processes digital signals. Many modern systems contain both digital and analog elements, with converters to allow signals to pass from one side to the other.

Relative Advantages of Analog and Digital Systems

Noise is any undesired disturbance added to the desired signal. It can arise from the thermal agitation of electrons in a resistor, from inductive or capacitive coupling of signals from other circuits, or from a number of other sources. Often these noise signals are random in occurrence and (to some degree) outside the control of the circuit designer. One of the most significant advantages that digital systems have, compared with analog systems, is in the way that noise affects the signals.

Figure 1.5 shows typical analog and digital signals before and after the addition of noise. Notice that the original levels (high or low) of the digital signal can be discerned even after the noise has been added, provided that the peak amplitude of the noise is less than half of the distance between the levels of the digital signal. This is possible because the digital signal takes only specific amplitudes that can still be recognized after some noise is added. Thus, noise can be completely removed from digital signals, provided that the noise amplitude is not too large.

On the other hand, when noise is added to the analog signal, it is not possible to determine the original amplitude of the signal exactly, because all amplitude values are valid. For example, a scratch on an analog phonograph record creates noise that cannot

...noise can be completely removed from digital signals, provided that the noise amplitude is not too large.

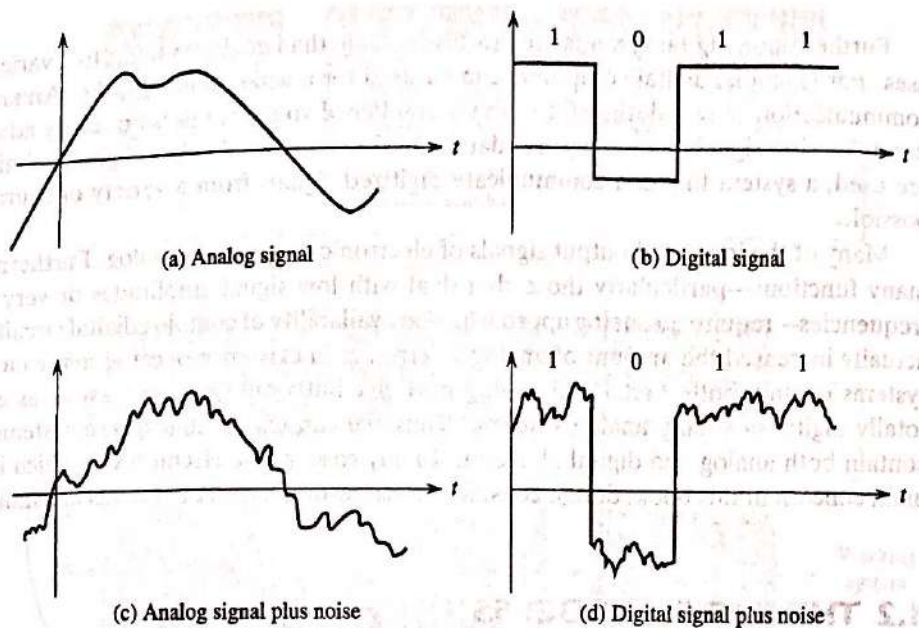


Figure 1.5 After noise is added, the original amplitudes of a digital signal can be determined. This is not true for an analog signal.

...noise tends to accumulate in analog signals each time they are processed.

by some processes that are well defined or a light source, and various other things, digital signals are not affected by noise.

Modern computer chips contain in excess of 10 million components.

...digital circuits tend to be easier than analog circuits to implement with integrated-circuit techniques.

Design is an iterative process.

be removed. If we transfer the signal to analog tape, even more noise is added. Thus, noise tends to accumulate in analog signals each time they are processed.

In general, analog systems require fewer individual circuit components than do digital systems. In the early years of electronics, individual circuit components were manufactured separately and then connected together by a manual process. Such circuits are called **discrete circuits**. Most early systems were designed as analog systems (to minimize the parts count), because the cost of a discrete circuit is nearly proportional to the number of circuit elements.

Modern technology has made it possible to manufacture thousands of circuit components and their interconnections all at one time by a small number of processing steps. Circuits produced in this manner are called **integrated circuits (ICs)**. It is now possible to manufacture a circuit with 100,000 components nearly as economically as a circuit with only 10 similar components. Thus, the cost of a circuit does not increase proportionately with the number of components—provided that all the components are amenable to integrated-circuit construction.

It turns out that digital circuits tend to be easier than analog circuits to implement with integrated-circuit techniques. Analog circuits often require large resistances, capacitances, or inductances that cannot be readily manufactured by such techniques. Thus, although digital systems are often more complex than analog systems, the digital approach to a design usually results in an affordable system with much higher performance. As integrated-circuit technology has developed, the trend of the electronics industry has been toward high-performance digital systems. A comparison of a digital compact disc with the older analog phonograph or tape player reveals this trend clearly, as well as the improved performance of the digital approach.

...digital systems are more adaptable than analog systems to a variety of uses.

Furthermore, digital systems are more adaptable than analog systems to a variety of uses. For example, digital computers can be used for a wide range of tasks. An analog communication system designed to carry a number of voice signals is not easily adapted to a television signal or to computer data. On the other hand, when digital techniques are used, a system that can communicate digitized signals from a variety of sources is possible.

Many of the input and output signals of electronic systems are analog. Furthermore, many functions—particularly those that deal with low signal amplitudes or very high frequencies—require an analog approach. The availability of complex digital circuits has actually increased the amount of analog electronics in existence because many modern systems contain both digital and analog portions, but would not be feasible as either totally digital or totally analog systems. Thus, we can expect that future systems will contain both analog and digital elements. In any case, at the circuit level, which is our main concern in this book, design considerations for both types of systems are similar.

1.2 THE DESIGN PROCESS

In this section, we give a general description of the steps that take place in the creation of complex electronic systems. Often, a large team of engineers—hundreds or thousands—is required to complete the steps from the statement of a problem to a working system. Usually, only part of the system consists of electronic circuits, and many other types of expertise are required. In this book, our main interest is circuit design, but it is always important for circuit designers to consider how their work fits into the total system-design process.

System Design

A flowchart of the design process for electronic systems is shown in Figure 1.6. The process starts with the statement of a problem to be solved. For example, we might want a system that can provide positional information to ships and aircraft.

The first step is to develop detailed system specifications. These include generally applicable items such as size, weight, shape, power consumption, what type of power sources are to be used, and the acceptable system cost. Other specifications pertain to a particular class of systems. For example, in a communication system, we need to know the type of signals to be transmitted, the overall bandwidth required for analog signals, the data rate for the digital signals, the minimum signal-to-noise ratio acceptable at the destination for the analog signals, the maximum acceptable error probability for data transmission, the number and location of transmitters and receivers, and so on.

Design is an iterative process. As a design progresses, we may need to return to the system specification step to refine the specifications. Issues often come up during the design that were not anticipated at the outset. Sometimes the options must be presented to the user of the final system for guidance in setting additional specifications. On the other hand, the design engineers may be able to determine appropriate additional specifications from their knowledge of the purpose of the system.

Design is an iterative process.

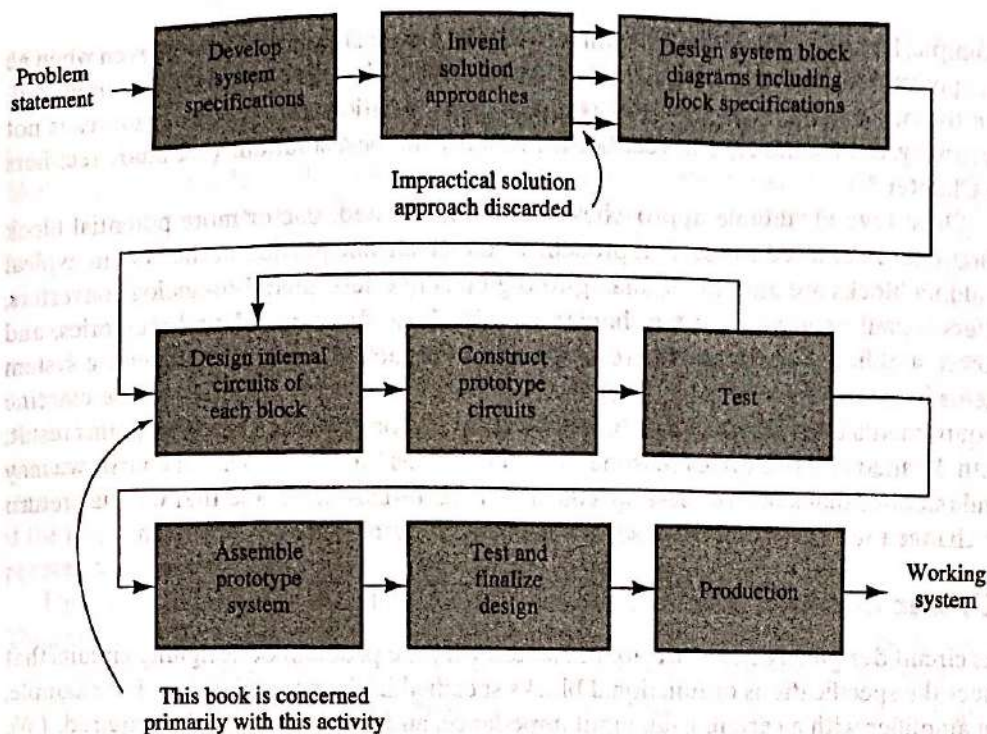


Figure 1.6 Typical flowchart for design of electronic systems.

After the system requirements have been determined, system design engineers consider all the approaches to solving the problem that can be imagined. This is a step where creativity comes into play. Design problems for which a measure of creativity is required are included in later chapters. Fortunately, creative skill is developed with practice and experience. Furthermore, much can be learned by studying the solutions others have created after one has confronted difficult problems requiring creativity for their solution.

Thus, by some process that is not well defined or easily explained, system engineers develop several general approaches to a problem. For example, the problem might be to design a system so that an airplane is not detectable by radar. Various basic approaches are possible, including designing the shape of the airplane so that it does not reflect radar signals, constructing the plane from materials that absorb radar signals, placing a transmitter on the craft that transmits signals to cancel the radar reflections, designing an electronic control system so that the craft can fly close to the ground (out of the path of the radar beam), and possibly a much superior idea not yet conceived.

A simpler example is the design of a system to deliver electrical power to the circuits of a certain computer. First, we need to determine the system specifications. These would include the nominal voltages, the current required from each voltage, the amount of voltage fluctuation allowed, whether or not the supply must be portable, the required level of system reliability, and so on. A number of basic approaches are possible, including the use of primary (not rechargeable) batteries, secondary (rechargeable) batteries, rectifier circuits that convert ac line power to dc, and gasoline-engine-driven electrical generators. Often, some requirement tends to select one or two of the possible approaches. For

...by some process that is not well defined or easily explained, system engineers develop several general approaches.

example, if the power supply is required to deliver large amounts of power, even when ac line power fails for long periods, the gasoline-engine-and-generator approach is indicated. On the other hand, if ac power is available and operation during power failures is not necessary, then some type of rectifier is probably the best solution. (We study rectifiers in Chapter 3.)

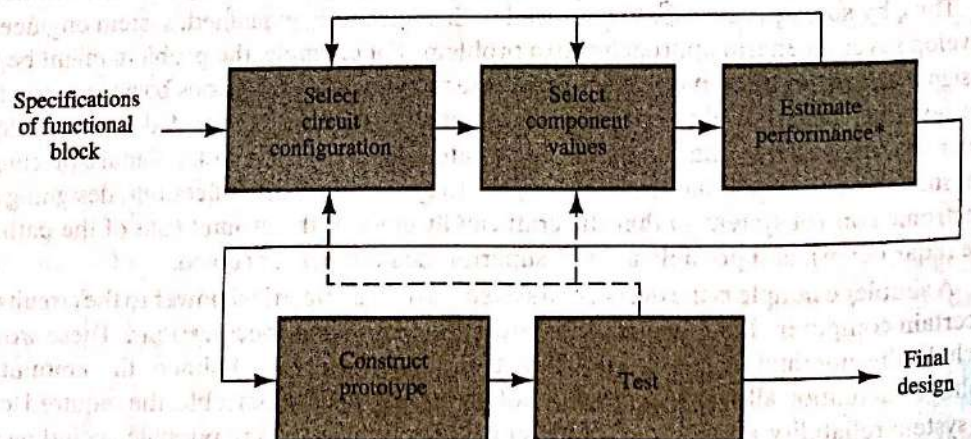
Once several suitable approaches have been selected, one or more potential block diagrams are created for each approach. In the electronic portion of the system, typical building blocks are amplifiers, analog-to-digital converters, digital-to-analog converters, filters, signal generators, wave-shaping circuits, logic functions, digital memories, and power supplies. Specifications are determined for each block so that the entire system meets its goals. At this point, a solution approach may be eliminated because extreme requirements exist for one of its blocks. Eventually, one or more block diagrams result, with detailed and (we hope) reasonable specifications for each block. Of course, we may find out later that some of these specifications are *unreasonable* and that we must return to change the block diagram or select an entirely different system approach.

Circuit Design

As circuit design engineers, we are presented with the problem of designing circuits that meet the specifications of functional blocks specified in the system design. For example, an amplifier with a certain gain, input impedance, and bandwidth may be required. (We consider amplifiers and their specifications later in this chapter.) The internal design process for each system block is similar to the design of the overall system. A flowchart of the circuit-design process is shown in Figure 1.7.

First, a circuit configuration is proposed on the basis of the experience and ingenuity of the design engineer. As you study the material in this book, your collection of useful circuit configurations—and ability to invent new ones—will grow. Next, values for each circuit parameter are selected. This can be done by the substitution of specifications into design equations, using your experience with similar circuits, or in some cases, by educated guesswork. Often, we must perform a mathematical analysis to develop design

Often, we must perform a mathematical analysis to develop design equations tailored to the circuit at hand. Thus, we illustrate analysis techniques for electronic circuits throughout the book.



*By use of theoretical analysis, computer simulation, or actual circuit tests.

Figure 1.7 Flowchart of the circuit-design process.

equations tailored to the circuit at hand. Thus, we illustrate analysis techniques for electronic circuits throughout the book.

Usually, in selecting a circuit configuration and initial parameter values, we are at least partially flying by the seats of our pants. The more difficult the design, the more likely this is. Therefore, we must verify that the configuration and component values selected meet the given specifications. This can be done in several ways: by traditional mathematical circuit analysis; computer simulation of the circuit; or actual construction of the circuit, together with measurement.

Mathematical analysis yields equations relating the performance of a circuit to the values of its components. For example, we can find a formula for the gain of a particular amplifier configuration in terms of resistance values and transistor parameters. Then we can substitute the values selected into the formula to see if the required performance specification is met. The theoretical approach has the important advantage that it sometimes clearly shows how to change component values if specifications are not met. For example, if the amplifier gain is too low and the analysis shows that the gain is proportional to the resistance of a particular resistor, we can increase the value of that resistance.

Unfortunately, circuits are often complex, and theoretical analysis can be difficult. Then we can simplify the analysis (at the expense of accuracy), resort to computer simulation, or, in rare cases, construct and measure the performance of an actual circuit.

Programs are available that can simulate complex integrated circuits to a much higher degree of accuracy than we can usually achieve with a theoretical analysis. However, computer simulation gives numerical data concerning the performance of a circuit with specific component values, but no formulas that can be inspected to see which parameters should be changed to achieve the specifications. Thus, even though the industry trend is toward the heavy use of computers in design, you should also become familiar with traditional mathematical analysis.

Building a circuit and measuring its performance is the ultimate test of determining the performance of the circuit. However, electronic systems are routinely implemented in a highly integrated form, making it virtually impossible to observe their internal operation. Furthermore, the expense and time required for producing integrated-circuit prototypes prohibit extensive experimentation. Thus, it is usually necessary to employ mathematical analysis and computer simulation to verify the proper functioning of our designs before implementing them.

The best approach is usually a simplified theoretical analysis to provide insight and estimates of circuit parameters. This can be followed by computer simulation to refine the circuit values. In design, we try to be economical in the use of our own time, so we tend to adopt the approach that yields the desired result with the least design effort. However, a little time spent investigating a circuit for our own education may be well spent in the long run.

After a design has been completed and shown, by theoretical analysis and computer simulation, to meet the desired specifications, a prototype circuit is constructed to further verify that the design meets the specifications. In those (hopefully rare) cases when the prototype fails, some adjustment of component values may solve the problem. In other cases, a different circuit configuration may be necessary. In even more extreme cases, only a different block diagram or basic approach to the system design will provide the answer.

...even though the industry trend is toward the heavy use of computers in design, you should also become familiar with traditional mathematical analysis.

The primary job of the design engineer is to produce the documentation necessary for others to construct the final system correctly and efficiently.

The Need for Documentation

Accurate and complete documentation throughout the design process is very important. After all, the primary job of the design engineer is to produce the documentation necessary for others to construct the final system correctly and efficiently. Typical documentation consists of circuit diagrams, mechanical drawings, parts lists, testing procedures, records of waveforms or measurements at various points in the circuit, an explanation of the operation of the circuit, and wiring lists. Some of the documentation, such as the circuit schematic, is standard throughout the industry. Other documentation is specific to particular companies.

The systems to be designed can be very complex. Over time, the engineer is called upon to work on a number of systems. Work on a particular block of a system can be spread over a long period of time, with lengthy gaps among various activities. Human memory is not sufficient for efficient progress. Information must be kept in written or machine-readable form, so that it is available to others working on a given system and not entrusted to memory.

Typically, information is stored in a computer network to make the current state of the complete system design continuously available to all of the engineers. This tends to ensure compatibility between various parts of the system and leads to efficiency of the design process.

1.3 INTEGRATED CIRCUITS

We have seen that system engineers design the block diagrams of electronic systems. Circuit designers select the proper devices and determine how to interconnect them to realize the blocks in the system. There are two other groups of electronics professionals that make extremely important contributions to electronic systems. One group consists of the engineers and scientists who conduct basic research on the principles of physical electronics. The second group comprises the process engineers who design the manufacturing processes for devices and integrated circuits.

Basic research on the physical principles of electronic materials and devices underlies all progress in electronic systems. Without an understanding of the physics related to the conduction of electricity, electronics could not exist. The study of the principles of physical electronics is by no means complete. Work continues, and we can expect further important discoveries. Therefore, physical electronics continues to be a very important area of research. We discuss some of the basic principles of physical electronics as the need arises, but the main emphasis of this book is circuit design.

Scientific discoveries in physical electronics have been rapidly followed by applications. Electronics began with the invention of an amplifying and switching device known as the vacuum triode by Lee DeForest in 1906. Vacuum-tube technology led to the spread of radio broadcasting during the 1920s, the development of television in the 1930s, and the first electronic computers in the 1940s.

In 1947, a team working at Bell Laboratories under the direction of William Shockley invented the solid-state transistor. The tremendous potential of this device was immediately recognized, and the development of modern electronics has proceeded therefrom rapidly. Continuing research in solid-state physics provides the flow of basic discoveries that are essential to the advance of electronic systems.

Transistors

Transistors of various kinds are the key elements of modern electronic systems. They are constructed by **doping** a semiconductor, such as a silicon crystal, with carefully selected and controlled impurities. Certain impurity elements produce ***n*-type material**, in which conduction arises mainly from **free electrons**. Other types of impurities produce ***p*-type material** in which conduction is—in effect—by positive particles called **holes**.

One important electronic device is the **bipolar junction transistor (BJT)**, which consists of layers of doped semiconductor as shown in Figure 1.8. The figure shows an ***npn*** transistor, which has a layer of ***p*-type material** between two ***n*-type layers**, however, it is also possible to construct a ***pn*p** BJT.

Another important device is the **metal-oxide-semiconductor field-effect transistor (MOSFET)**, shown in Figure 1.9. This device has a metal **gate *G*** that is insulated from a **channel** of ***n*-type semiconductor** by a layer of silicon dioxide. (Similarly useful devices can be constructed using a channel of ***p*-type material**.) Terminals called the **drain *D*** and the **source *S*** are connected to opposite ends of the channel.

A MOSFET can act as a switch that either connects or disconnects the drain and source terminals, depending on the voltage applied to the gate. For certain ranges of voltage thus applied, the switch is open and no current can flow between the drain and source. For other ranges of gate voltage, the switch is closed and current easily flows between drain and source. This switching action is the basis of digital circuits. As programs run on your computer, millions of MOS transistors switch each second.

Another mode of operation of the MOSFET occurs when the gate voltage lies between the ranges for which the drain to source is open or closed. Then, the current flowing in the channel can be smoothly controlled by the gate voltage. In this region, the MOSFET can amplify analog signals. In your stereo system, transistors rapidly vary the flow of current to the loudspeakers to produce music.

Similarly, BJTs can act either as switches that are useful in digital circuits or as controlled current sources that are useful in analog circuits.

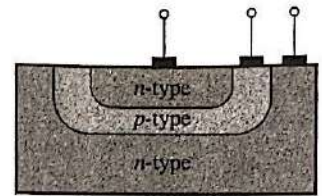


Figure 1.8 The *npn* BJT.

A MOSFET can act as a switch that either connects or disconnects the drain and source terminals, depending on the voltage applied to the gate.

As programs run on your computer, millions of MOS transistors switch each second.

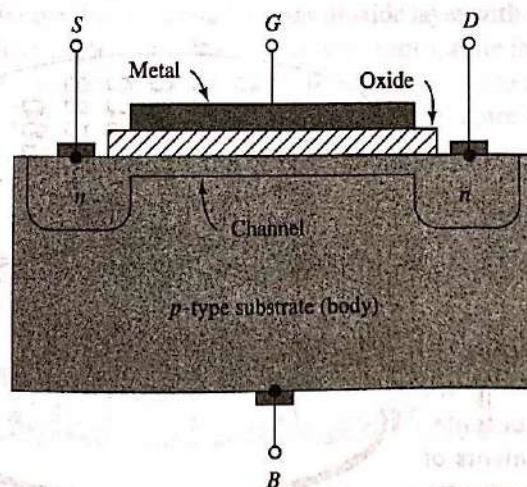


Figure 1.9
A metal-oxide-semiconductor (MOS) transistor.

Integrated Circuits

In 1958, an extremely important device was invented independently by Jack Kilby, working at Texas Instruments, and by Noyce and Moore at Fairchild Semiconductor: the integrated circuit (IC), which combines BJTs, MOSFETs, resistors, and capacitors, as well as their interconnections, into a functional circuit on a single chip.

Next, we very briefly describe, in a simplified fashion, the manufacture of an integrated circuit. The discussion illustrates typical steps employed by process engineers to fabricate ICs.

The process starts with the refinement of silicon to an extremely high degree of purity. Then, selected impurities are added to create *n*-type material and a single crystal is grown. The resulting crystal is typically a cylinder 8 inches (200 mm) in diameter. The crystal is cut into circular wafers 650 to 700 μm in thickness. Eventually, each wafer becomes scores of ICs.

Next, the surface of the wafer is polished so that it has a mirrorlike appearance. The polished surface is exposed to oxygen in a furnace, and a surface layer of silicon dioxide is grown. Then the oxide is coated with **photoresist**. The areas intended to become, for example, the *p*-type regions of transistors are exposed to light through a **mask**, as illustrated in Figure 1.10. Next, the photoresist that has been exposed is removed by chemical means, and the silicon dioxide is etched away, exposing the silicon wafer. This subprocess, called photolithography and illustrated in Figure 1.11, opens windows through the silicon dioxide above the regions that are to become *p*-type material.

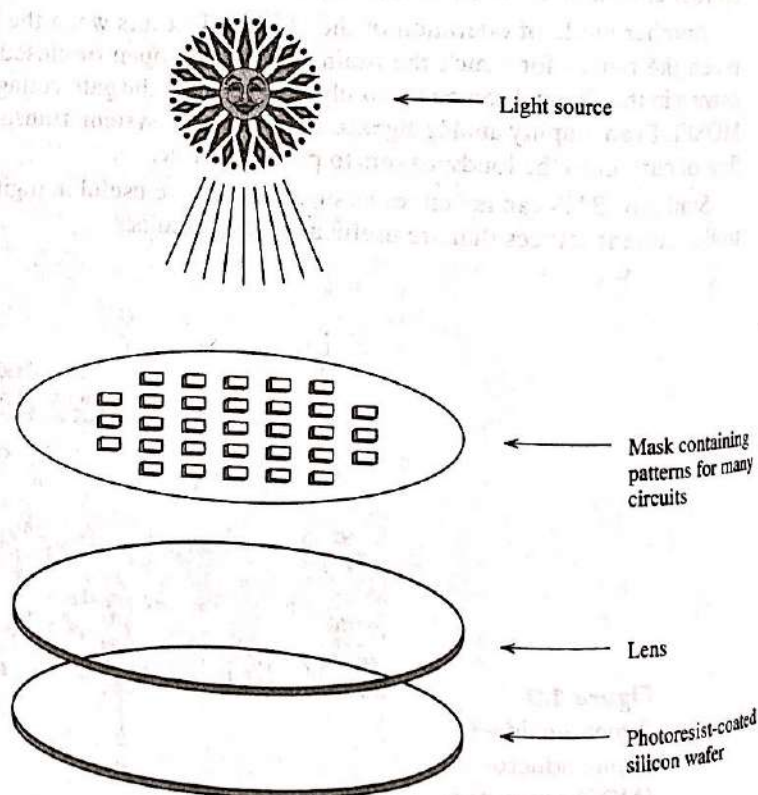


Figure 1.10
In photolithography the photoresist-coated wafer is exposed to a light pattern defining the regions to become specific elements of circuit components.

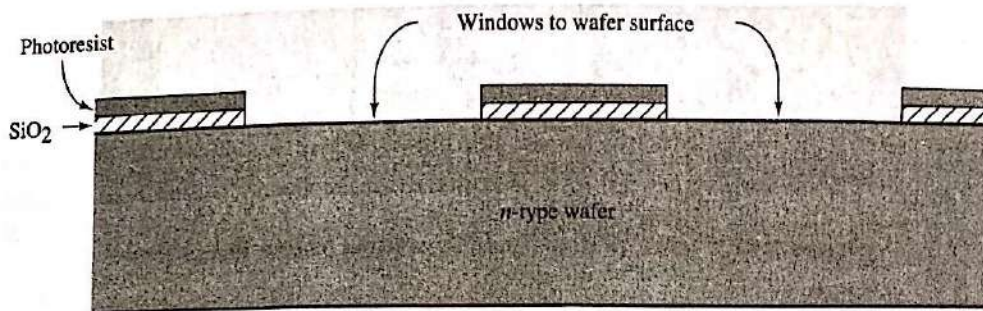


Figure 1.11 Photolithography exposes selected regions of the silicon wafer.

Photolithography is repeated several times in the manufacture of electronic devices.

Following photolithography, the wafer is exposed to appropriate gaseous impurities in a diffusion furnace. These impurities, in the form of atoms, diffuse into the exposed regions of the wafer, changing it from *n*-type to *p*-type. The silicon dioxide acts as a barrier for the impurity atoms, so that the other regions of the surface are unchanged. The depth of the *p*-type region can be controlled by time and temperature in the diffusion furnace. Next, the silicon-dioxide barrier is removed. The result is a wafer of *n*-type material with *p*-type regions, as shown in Figure 1.12.

Photolithography is repeated several times in the manufacture of integrated circuits.



Figure 1.12 Selected regions of the wafer have been changed to *p*-type material by exposure to impurities in a diffusion furnace.

Then, oxidation of the surface, the application of photoresist, exposure through a mask, developing, and etching are repeated to create a silicon-dioxide layer with windows in appropriate locations, as shown in Figure 1.13. Processing with appropriate impurities in a diffusion furnace changes the exposed regions of the wafer back to *n*-type material. This results in a large number of devices on each wafer, as illustrated in Figure 1.14.

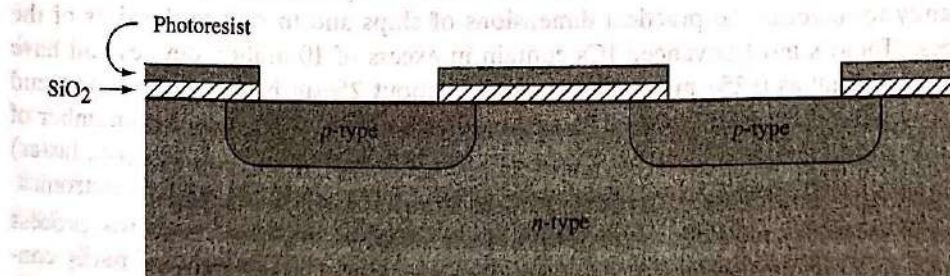


Figure 1.13 Photolithography exposes regions for the next diffusion.

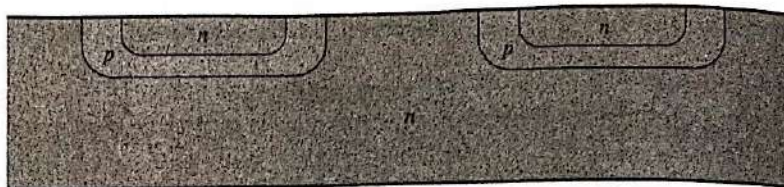


Figure 1.14 The wafer now contains millions of *npn* transistors.

Additional masks and photolithography processes are used to deposit gate regions, silicon-dioxide insulation, and metal interconnections on the surface of the wafer. A modern BiCMOS process capable of producing both bipolar and MOS transistors might contain 16 masks and 70 total processing steps. Eventually, the wafer contains between 100 and several thousand complete ICs.

The wafer is then cut to separate the individual ICs. Finally, leads are attached and the chips are packaged and tested. This can be the most expensive single step in the process. Certainly the other steps are costly, but because many wafers are processed together, each containing many ICs, the cost is small for each circuit. Packaging and testing are carried out on an individual basis and do not benefit from the savings of large-scale parallelism. Furthermore, the interconnections between packages are the least reliable aspects of a system. Therefore, circuit designers are strongly motivated to integrate a system with the fewest number of IC chips possible.

We have given a simplified description of the integrated-circuit manufacturing process. However, several important points are evident:

1. ICs are composed of devices constructed by diffusing impurities into semiconductor wafers and depositing materials such as metal interconnections on their surfaces.
2. Many ICs can be constructed concurrently on a batch of wafers.
3. When the process is highly perfected for a given IC design, the unit cost of an IC is almost independent of its complexity, within practical limits.

In the early 1960s, ICs contained perhaps 100 devices, and the smallest features were about 25 micrometers (μm). Realizing that the cost of complex electronic systems could be reduced dramatically by the use of more complex ICs, process engineers have worked diligently to increase the practical dimensions of chips and to reduce the sizes of the devices. Today's most advanced ICs contain in excess of 10 million devices and have features as small as $0.25 \mu\text{m}$. (A human hair is about $25 \mu\text{m}$ in diameter.) The trend toward smaller devices is expected to continue. In addition to the increased number of devices, the reduction in the size of features results in higher performance (i.e., faster) digital circuits. Thus, we can anticipate even greater advances in the field of electronics.

These advances will result from teamwork by physical electronics scientists, process engineers, circuit designers, and systems designers. Although this book primarily considers circuit design, it provides useful background information for all engineers in the electronics industry.

...circuit designers are strongly motivated to integrate a system with the fewest number of IC chips possible.

One micrometer, also called a micron, equals 10^{-6}m .

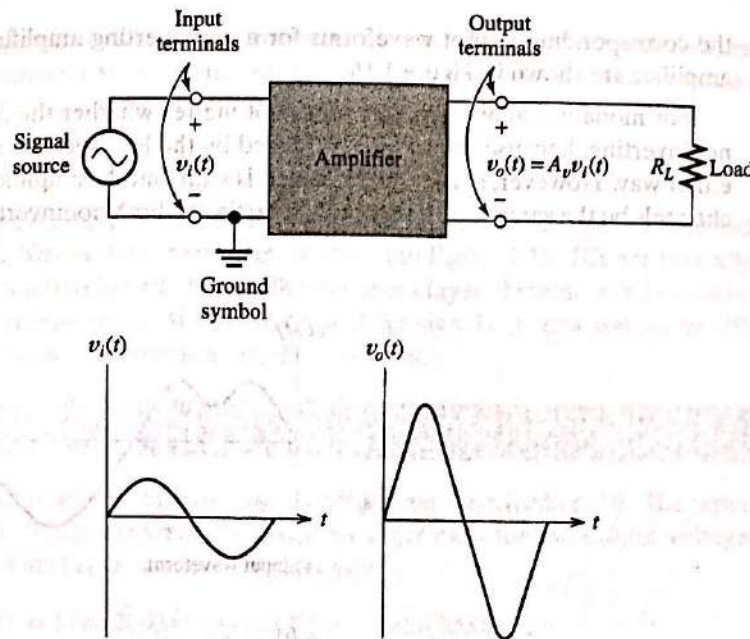


Figure 1.15
Electronic amplifier.

1.4 BASIC AMPLIFIER CONCEPTS

One of the most important functional blocks found in electronic systems is the amplifier. In the remainder of this chapter, we introduce some external amplifier characteristics; the internal design of amplifiers is treated in later chapters.

Probably you are already familiar with the concept of amplification. Ideally, an amplifier produces an output signal with the same waveshape as the input signal, but with a larger amplitude. The concept is illustrated in Figure 1.15. The signal source produces a signal $v_i(t)$ that is applied to the input terminals of the amplifier, which generates an output signal

$$v_o(t) = A_v v_i(t) \quad (1.2)$$

Output voltage equals input voltage times voltage gain.

across a load resistance R_L connected to the output terminals. The constant A_v is called the **voltage gain** of the amplifier. Often, the magnitude of the voltage gain is much larger than unity, but we will see later that useful amplification can take place even if A_v is less than unity in magnitude.

An example of a signal source is a microphone, which typically produces a peak signal of 1 mV as we speak into it. This small signal can be used as the input to an amplifier with a voltage gain of 10,000 to produce an output signal with a peak value of 10 V. If this larger output voltage is applied to a loudspeaker, a much louder version of the sound entering the microphone results.

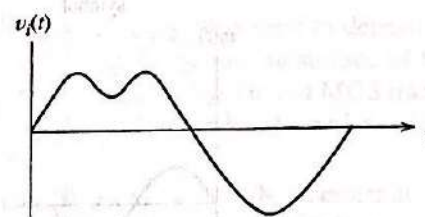
Sometimes, A_v is a negative number, so the output voltage is an inverted version of the input, and the amplifier is then called an **inverting amplifier**. On the other hand, if A_v is a positive number, we have a **noninverting amplifier**. A typical input waveform and

If A_v is a positive number, we have a noninverting amplifier, and if A_v is negative, we have an inverting amplifier.

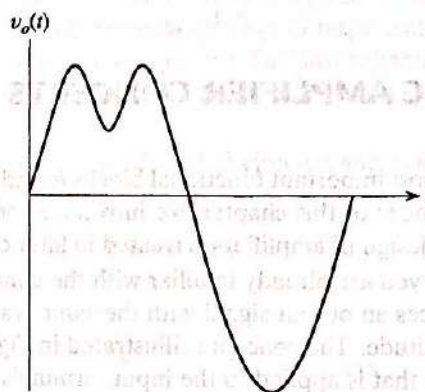
If video signals are inverted, a negative image with black and white interchanged results...

the corresponding output waveforms for a noninverting amplifier and for an inverting amplifier are shown in Figure 1.16.

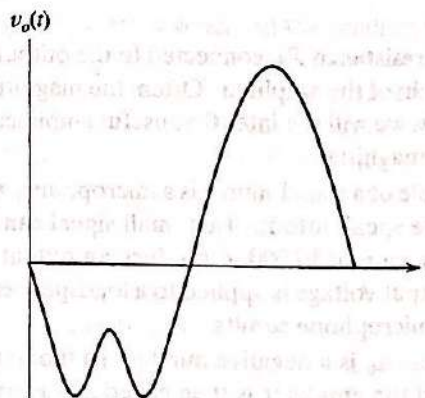
For monaural audio signals, it does not matter whether the amplifier is inverting or noninverting, because the sounds produced by the loudspeaker are perceived the same either way. However, in a stereo system, it is vital that the amplifiers for the left and right channels be the same (i.e., either both inverting or both noninverting), so that the signals



(a) Input waveform



(b) Output waveform of a noninverting amplifier



(c) Output waveform of an inverting amplifier

Figure 1.16
Input waveform
and corresponding
output waveforms.

applied to the two loudspeakers have the proper phase relationship. If video signals are inverted, a negative image with black and white interchanged results, so it is important whether video amplifiers are inverting or noninverting.

The Common Ground Node

Often, one of the amplifier input terminals and one of the output terminals are connected to a common ground. Notice the ground symbol shown in Figure 1.15. ICs are typically mounted on multilayer printed circuit boards that contain a layer of metal called a ground plane. This common ground serves as the return path for signal currents and, as we will see later, the dc power-supply currents in electronic circuits.

EXERCISE

1.1 A certain noninverting amplifier has a voltage gain magnitude of 50. The input voltage is $v_i(t) = 0.1 \sin(2000\pi t)$. (a) Find an expression for the output voltage $v_o(t)$. (b) Repeat Part (a) for an inverting amplifier.

Answer (a) $v_o(t) = 5 \sin(2000\pi t)$; (b) $v_o(t) = -5 \sin(2000\pi t)$.

The Voltage-Amplifier Model

Amplification can be modeled by a controlled source as illustrated in Figure 1.17. Because real amplifiers draw some current from the signal source, a realistic model of an amplifier must include a resistance R_i across the input terminals. Furthermore, a resistance R_o must be included in series with the output terminals to account for the fact that the output voltage of a real amplifier is reduced when load current flows. The complete amplifier model shown in Figure 1.17 is called the **voltage-amplifier model**. Later we will see that other models can be used for amplifiers.

The **input resistance** R_i of an amplifier is the equivalent resistance seen when looking into the input terminals. As we will find later, the input circuitry can sometimes include capacitive or inductive effects, and we would then refer to the **input impedance**, which can be a function of frequency. For example, the input amplifiers of typical oscilloscopes have an input impedance consisting of a 1-M Ω resistance in parallel with a 47-pF capacitance. In this chapter, we assume that the input impedance is purely resistive unless stated otherwise.

Amplification can be modeled by a controlled source.

The **input resistance** R_i of an amplifier is the equivalent resistance seen when looking into the input terminals.

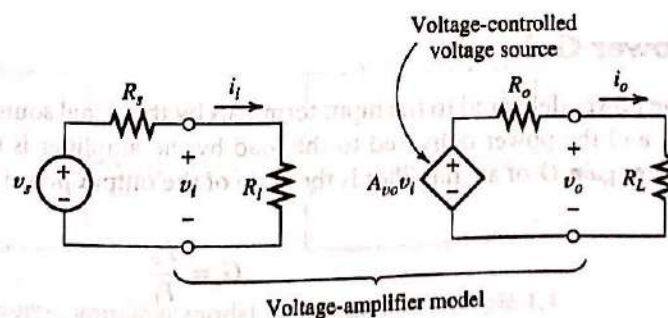


Figure 1.17
Model of an electronic amplifier, including input resistance R_i and output resistance R_o .

Output resistance is the Thévenin resistance seen when looking back into the output terminals of an amplifier.

Open-circuit voltage gain is the ratio of output amplitude to input amplitude with the output terminals open circuited.

Formula for current gain in terms of voltage gain and resistances.

The resistance R_o in series with the output terminals is known as the **output resistance**. Real amplifiers are not able to deliver a fixed voltage to an arbitrary load resistance. Instead, the output voltage becomes smaller as the load resistance R_L becomes smaller, and the output resistance accounts for this reduction. When the load draws current, a voltage drop occurs across the output resistance, resulting in a reduction of the output voltage.

The voltage-controlled voltage source models the amplification properties of the amplifier. Notice that the voltage produced by this source is simply a constant A_{vo} times the input voltage v_i . If the load is an open circuit, there is no drop across the output resistance, and then $v_o = A_{vo}v_i$. For this reason, A_{vo} is called the **open-circuit voltage gain**.

To summarize, the voltage-amplifier model includes the input impedance, the output impedance, and the open-circuit voltage gain in an equivalent circuit for the amplifier.

Current Gain

As shown in Figure 1.17, the input current i_i is the current delivered to the input terminals of the amplifier, and the output current i_o is the current flowing through the load. The **current gain** A_i of an amplifier is the ratio of the output current to the input current:

$$A_i = \frac{i_o}{i_i} \quad (1.3)$$

The input current can be expressed as the input voltage divided by the input resistance, and the output current is the output voltage divided by the load resistance. Thus, we can find the current gain in terms of the voltage gain and the resistances as

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_L}{v_i/R_i} = A_v \frac{R_i}{R_L} \quad (1.4)$$

in which

$$A_v = \frac{v_o}{v_i}$$

is the voltage gain with the load resistance connected. A_v is smaller in magnitude than the open-circuit voltage gain A_{vo} because of the voltage drop across the output resistance.

Power Gain

The power delivered to the input terminals by the signal source is called the input power P_i , and the power delivered to the load by the amplifier is the output power P_o . The **power gain** G of an amplifier is the ratio of the output power to the input power:

$$G = \frac{P_o}{P_i} \quad (1.5)$$

Because we are assuming that the input impedance and load are purely resistive, the average power at either set of terminals is simply the product of the root-mean-square (rms) current and rms voltage. Thus, we can write

$$G = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i} = A_v A_i = (A_v)^2 \frac{R_i}{R_L} \quad (1.6)$$

Formula for power gain in terms of voltage gain and resistances.

Notice that we have used uppercase symbols, such as V_o and I_o , for the rms values of the currents and voltages. We use lowercase symbols, such as v_o and i_o , for the instantaneous values. Of course, since we have assumed, so far, that the instantaneous output is a constant times the instantaneous input, the ratio of the rms voltages is the same as the ratio of the instantaneous voltages and both ratios are equal to the voltage gain of the amplifier.

Example 1.1 Using the Voltage-Amplifier Model

A source with an internal voltage of $V_s = 1 \text{ mV rms}$ and an internal resistance of $R_s = 1 \text{ M}\Omega$ is connected to the input terminals of an amplifier having an open-circuit voltage gain of $A_{vo} = 10^4$, an input resistance of $R_i = 2 \text{ M}\Omega$, and an output resistance of $R_o = 2 \Omega$. The load resistance is $R_L = 8 \Omega$. Find the voltage gains $A_{vs} = V_o/V_s$ and $A_v = V_o/V_i$. Also, find the current gain and power gain.

SOLUTION A model of the source, amplifier, and load is shown in Figure 1.18. We can apply the voltage-divider principle to the input circuit to write

$$V_i = \frac{R_i}{R_i + R_s} V_s = 0.667 \text{ mV rms}$$

The voltage produced by the voltage-controlled source is given by

$$A_{vo} V_i = 10^4 V_i = 6.67 \text{ V rms}$$

Next, the output voltage can be found by using the voltage-divider principle, resulting in

$$V_o = A_{vo} V_i \frac{R_L}{R_L + R_o} = 5.33 \text{ V rms}$$

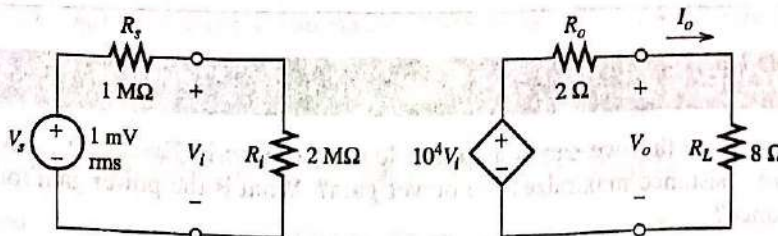


Figure 1.18 Source, amplifier model, and load for Example 1.1.

Now, we can find the required voltage gains:

$$A_v = \frac{V_o}{V_i} = A_{vo} \frac{R_L}{R_L + R_o} = 8000$$

and

$$A_{vs} = \frac{V_o}{V_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} = 5333$$

Using Equations (1.4) and (1.6), we observe that the current gain and power gain are

$$A_i = A_v \frac{R_i}{R_L} = 2 \times 10^9$$

and

$$G = A_v A_i = 16 \times 10^{12}$$

Notice that the current gain is very large, because the high input resistance allows only a small amount of input current to flow, whereas the relatively small load resistance allows the output current to be relatively large. $\square$

Loading Effects

Loading effects reduce the gain of an amplifier.

In example 1.1, we saw that not all of the internal voltage of the source appears at the input terminals of the amplifier. This is because the finite input resistance of the amplifier allows current to flow into the input terminals, resulting in a voltage drop across the internal resistance R_s of the source. Similarly, the voltage produced by the controlled source does not all appear across the load. These reductions in voltage are called **loading effects**. Because of loading effects, the voltage gains (A_v or A_{vs}) realized are less than the internal gain A_{vo} of the amplifier.

EXERCISE

1.2 An amplifier has an input resistance of 2000Ω , an output resistance of 25Ω , and an open-circuit voltage gain of 500. The source has an internal voltage of $V_s = 20 \text{ mV}$ and a resistance of $R_s = 500 \Omega$. The load resistance is $R_L = 75 \Omega$. Find the voltage gains $A_v = V_o/V_i$ and $A_{vs} = V_o/V_s$. Find the current gain and the power gain.

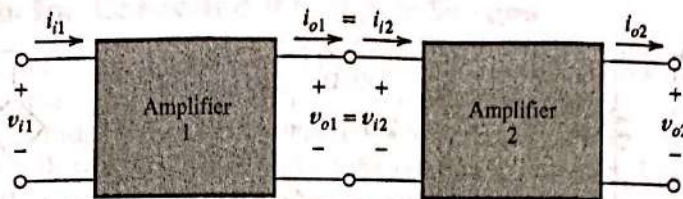
Answer $A_v = 375$, $A_{vs} = 300$, $A_i = 10^4$, $G = 3.75 \times 10^6$.

EXERCISE

1.3 Assume that we can change the load resistance in Exercise 1.2. What value of load resistance maximizes the power gain? What is the power gain for this load resistance?

Answer $R_L = 25 \Omega$, $G = 5 \times 10^6$.

Figure 1.19
Cascade connection of two amplifiers.



1.5 CASCADED AMPLIFIERS

Sometimes we connect the output of one amplifier to the input of another as shown in Figure 1.19. This is called a **cascade connection** of the amplifiers. The overall voltage gain of the cascade connection is given by

$$A_v = \frac{v_{o2}}{v_{i1}}$$

Multiplying and dividing by v_{o1} , this equation becomes

$$A_v = \frac{v_{o1}}{v_{i1}} \times \frac{v_{o2}}{v_{o1}}$$

Referring to Figure 1.19, we see that $v_{i2} = v_{o1}$. Therefore, we can write

$$A_v = \frac{v_{o1}}{v_{i1}} \times \frac{v_{o2}}{v_{i2}}$$

However, $A_{v1} = v_{o1}/v_{i1}$ is the gain of the first stage, and $A_{v2} = v_{o2}/v_{i2}$ is the gain of the second stage, so we have

$$A_v = A_{v1}A_{v2} \quad (1.7)$$

Thus, the overall voltage gain of cascaded amplifier stages is the product of the voltage gains of the individual stages. (Of course, it is necessary to include loading effects in computing the gain of each stage. Notice that the input resistance of the second stage loads the first stage.)

Similarly, the overall current gain of a cascade connection of amplifiers is the product of the current gains of the individual stages. Furthermore, the overall power gain is the product of the individual power gains.

In a cascade connection, the output of one amplifier is connected to the input of another amplifier.

...the overall voltage gain of cascaded amplifier stages is the product of the voltage gains of the individual stages.

Example 1.2 Analysis of a Cascaded Amplifier

Consider the cascade connection of two amplifiers shown in Figure 1.20. Find the current gain, voltage gain, and power gain of each stage and for the overall cascade connection.

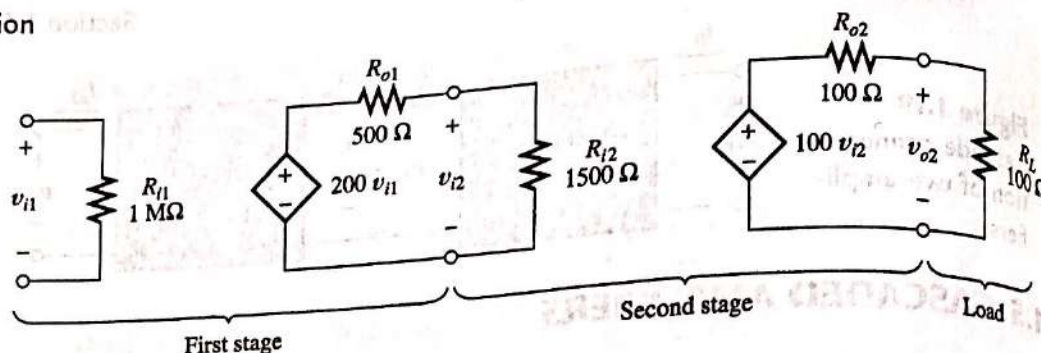


Figure 1.20 Cascaded amplifiers of Example 1.2.

SOLUTION Considering loading by the input resistance of the second stage, we see that the voltage gain of the first stage is

$$A_{v1} = A_{vo1} \frac{R_{i2}}{R_{i2} + R_{o1}} = 150$$

where we have used the fact that $A_{vo1} = 200$, as indicated in Figure 1.20. Similarly,

$$A_{v2} = A_{vo2} \frac{R_L}{R_L + R_{o2}} = 50$$

The overall voltage gain is

$$A_v = A_{v1} A_{v2} = 7500$$

Because R_{i2} is the load resistance for the first stage, we can find the current gain of the first stage by the use of Equation (1.4):

$$A_{i1} = A_{v1} \frac{R_{i1}}{R_{i2}} = 10^5$$

Similarly, the current gain of the second stage is found as

$$A_{i2} = A_{v2} \frac{R_{i2}}{R_L} = 750$$

The overall current gain is

$$A_i = A_{i1} A_{i2} = 75 \times 10^6$$

Now the power gains can be found as

$$G_1 = A_{v1} A_{i1} = 1.5 \times 10^7$$

$$G_2 = A_{v2} A_{i2} = 3.75 \times 10^4$$

and

$$G = G_1 G_2 = 5.625 \times 10^{11}$$

Simplified Models for Cascaded Amplifier Stages

Sometimes we will want to find a simplified model for a cascaded amplifier. The input resistance of the cascade is the input resistance of the first stage, and the output resistance of the cascade is the output resistance of the last stage. The open-circuit voltage gain of the cascade is computed with an open-circuit load on the last stage. However, loading effects of each stage on the preceding stage must be considered. Once the open-circuit voltage gain of the overall cascade connection is found, a simplified model can be drawn.

Example 1.3 Determining the Overall Model for a Cascaded Amplifier

Find the overall simplified model for the cascade connection of Figure 1.20.

SOLUTION The voltage gain of the first stage, accounting for the loading of the second stage, is

$$A_{v1} = A_{vo1} \frac{R_{i2}}{R_{i2} + R_{o1}} = 150$$

With an open-circuit load, the gain of the second stage is

$$A_{v2} = A_{vo2} = 100$$

The overall open-circuit gain is

$$A_{vo} = A_{v1} A_{v2} = 15 \times 10^3$$

The input resistance of the cascade amplifier is

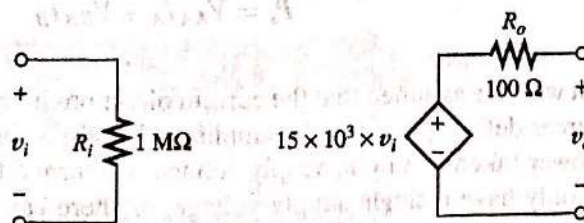
$$R_i = R_{i1} = 1 \text{ M}\Omega$$

and the output resistance is

$$R_o = R_{o2} = 100 \Omega$$

The simplified model for the cascade is shown in Figure 1.21.

Figure 1.21
Simplified
model for the
cascaded am-
plifiers of Fig-
ure 1.20. See
Example 1.3.



To find the voltage-amplifier model for an amplifier, we must determine the open-circuit voltage gain, the input impedance, and the output impedance.

Power dissipation is the power that is converted to heat within the amplifier.

The equation relating power to an amplifier.

It is customary to use uppercase symbols with repeated subscripts, such as V_{ce} , for dc supply voltages in electronic circuits.

EXERCISE

1.4 Three amplifiers with the following characteristics are cascaded.

1. Amplifier 1 : $A_{vo1} = 10$, $R_{i1} = 1 \text{ k}\Omega$, $R_{o1} = 100 \Omega$
2. Amplifier 2 : $A_{vo2} = 20$, $R_{i2} = 2 \text{ k}\Omega$, $R_{o2} = 200 \Omega$
3. Amplifier 3 : $A_{vo3} = 30$, $R_{i3} = 3 \text{ k}\Omega$, $R_{o3} = 300 \Omega$

Find the parameters for the simplified model of the cascaded amplifier. Assume that the amplifiers are cascaded in the order 1, 2, 3.

Answer $R_i = 1 \text{ k}\Omega$, $R_o = 300 \Omega$, $A_{vo} = 5357$.

EXERCISE

1.5 Repeat Exercise 1.4 if the order of the amplifiers is changed to 3, 2, 1.

Answer $R_i = 3 \text{ k}\Omega$, $R_o = 100 \Omega$, $A_{vo} = 4348$.

1.6 POWER SUPPLIES AND EFFICIENCY

Power is supplied to the internal circuitry of amplifiers from a **power supply**. The power supply typically delivers current from several dc voltages to the amplifier—one configuration is illustrated in Figure 1.22. The average power supplied to the amplifier by each voltage source is the product of the average current and the voltage. The total power supplied is the sum of the powers supplied by each voltage source. For example, the total average power supplied to the amplifier of Figure 1.22 is

$$P_s = V_{AA}I_A + V_{BB}I_B \quad (1.8)$$

Note that we have assumed that the current directions in the supply voltages are such that both sources deliver power to the amplifier. Rarely, a condition occurs for which some of the power taken from one supply voltage is returned to another source. Sometimes we may only have a single supply voltage, or there can be several, so the number of terms in a supply-power calculation such as Equation (1.8) is variable. It is customary to use uppercase symbols with repeated uppercase subscripts, such as V_{CC} , for dc supply voltages in electronic circuits.

It is customary to use uppercase symbols with repeated uppercase subscripts, such as V_{CC} , for dc supply voltages in electronic circuits.

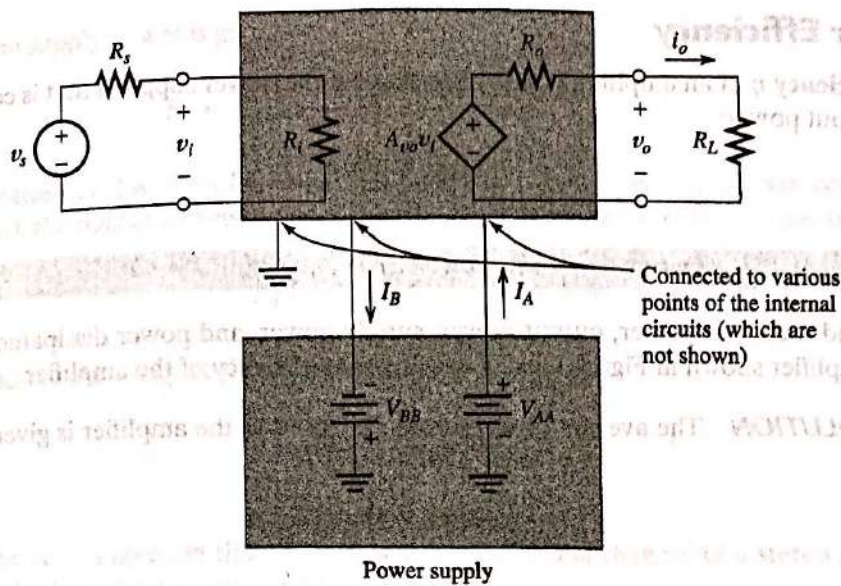


Figure 1.22 The power supply delivers power to the amplifier from several constant voltage sources.

We have seen that the power gain of typical amplifiers can be very large. Thus, the output power delivered to the load is much greater than the power taken from the signal source. This additional power is obtained from the power supply. Furthermore some of the power taken from the power supply is **dissipated** as heat in the internal circuits of the amplifier. Such dissipation is an undesirable effect that we usually try to minimize when designing the internal circuitry of an amplifier.

The sum of the power P_i entering the amplifier from the signal source and the power P_s from the power supply must be equal to the sum of the output power P_o and the power dissipated P_d . That is,

$$P_i + P_s = P_o + P_d \quad (1.9)$$

Power dissipation is the power that is converted to heat within the amplifier.

Key equation relating powers in an amplifier.

which is illustrated in Figure 1.23. Often, the input power P_i from the signal source is insignificant compared with the other terms in this equation.

To summarize, we can view an amplifier as a system that takes power from the dc power supply and converts part of this power into output signal power. For example, a stereo audio system converts part of the power taken from the power supply into signal power that is finally converted to sound by the loudspeakers.

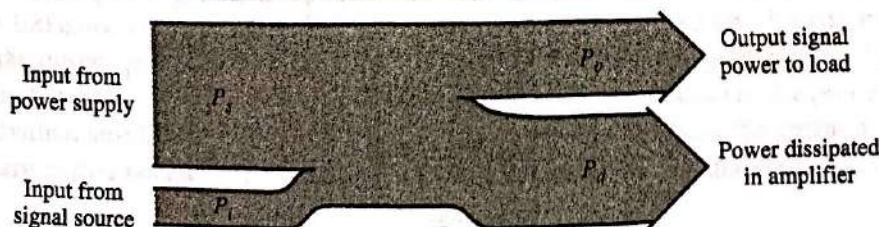


Figure 1.23 Illustration of power flow.

Power Efficiency

The **efficiency** η of an amplifier is the percentage of the power supplied that is converted into output power:

$$\eta = \frac{P_o}{P_s} \times 100\%$$

(1.10)

Key equation defining amplifier efficiency.

Example 1.4 Determining the Power Efficiency of an Amplifier

Find the input power, output power, supply power, and power dissipated in the amplifier shown in Figure 1.24. Also, find the efficiency of the amplifier.

SOLUTION The average signal power delivered to the amplifier is given by

$$P_i = \frac{V_i^2}{R_i} = 10^{-11} \text{ W} = 10 \text{ pW}$$

(Recall that $1 \text{ pW} = 1 \text{ picowatt} = 10^{-12} \text{ W}$.) The output voltage is

$$V_o = A_{vo} V_i \frac{R_L}{R_L + R_o} = 8 \text{ V rms}$$

We find the average output power as

$$P_o = \frac{V_o^2}{R_L} = 8 \text{ W}$$

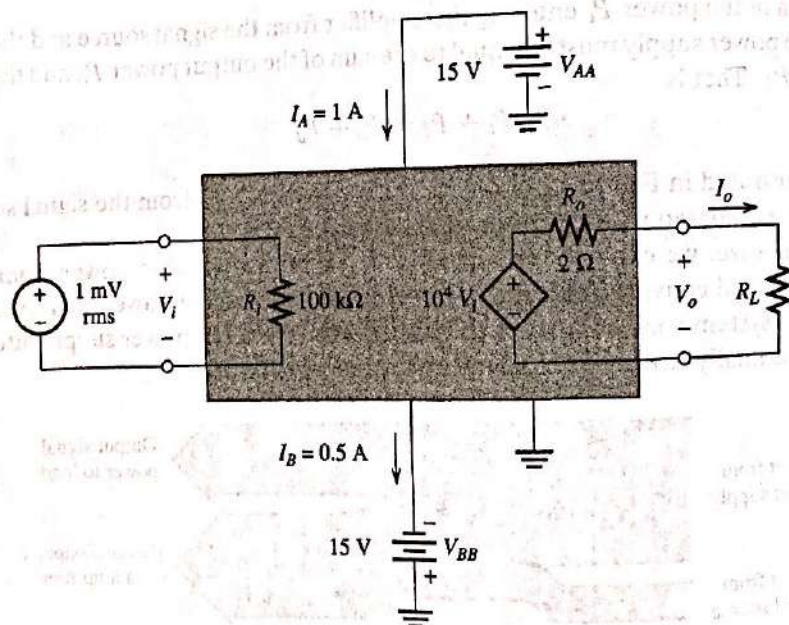


Figure 1.24 Amplifier of Example 1.4.

The supply power is given by

$$P_s = V_{AA}I_A + V_{BB}I_B = 15 + 7.5 = 22.5 \text{ W}$$

Notice that (as often happens) the input signal power is insignificant compared with the output and supply powers. The power dissipated as heat in the amplifier is

$$P_d = P_s + P_i - P_o = 14.5 \text{ W}$$

and the efficiency of the amplifier is

$$\eta = \frac{P_o}{P_s} = 35.6\%$$

The values given in this example are typical of one channel of a stereo amplifier under high-output test conditions. $\square$

EXERCISE

1.6 A certain amplifier is supplied with 1.5 A from a 15-V supply. The output signal power is 2.5 W and the input signal power is 0.5 W. Find the power dissipated in the amplifier and the efficiency.

Answer $P_d = 20.5 \text{ W}$, $\eta = 11.1\%$.

1.7 DECIBEL NOTATION

Power gain is often expressed in decibels (dB) as

$$G_{\text{dB}} = 10 \log G \quad (1.11)$$

where G is the power gain as a ratio and the logarithm is to the base 10. Thus, power gain of $G = 100$ converts to 20 dB, unity gain converts to 0 dB, and so on. An attenuator, for which the output power is smaller than the input power, has a negative decibel gain.

Recall that the overall gain for cascaded amplifiers is the product of the power gains of the individual amplifiers. When the gains are expressed in decibels, the gains of cascaded stages are added because of the properties of the logarithm. To illustrate this point, we have

$$G = G_1 G_2 \quad (1.12)$$

Key equation for conversion of power gain into decibels.

Expressed in decibels, this becomes

$$G_{dB} = 10 \log(G) = 10 \log(G_1 G_2)$$

which can be written as

$$G_{dB} = 10 \log(G_1) + 10 \log(G_2)$$

When the gains are expressed in decibels, the gains of cascaded stages are added.

Finally, we have

$$G_{dB} = G_{1dB} + G_{2dB} \quad (1.13)$$

Power gain can be computed from voltage gain, input resistance, and output resistance as given by Equation (1.6), which is repeated here for convenience:

$$G = A_v^2 \frac{R_i}{R_L}$$

If this expression is converted to decibels, we have

$$G_{dB} = 10 \log A_v^2 + 10 \log R_i - 10 \log R_L$$

which can be written as

$$G_{dB} = 20 \log |A_v| + 10 \log R_i - 10 \log R_L \quad (1.14)$$

Voltage and Current Gains Expressed in Decibels

Perhaps because of Equation (1.14), voltage gain is converted to decibels by

$$A_{v,dB} = 20 \log |A_v| \quad (1.15)$$

... the voltage gain of an amplifier in decibels is not the same as the power gain in decibels, unless $R_i = R_L$.

Thus, a voltage gain of 10 becomes 20 dB, 100 becomes 40 dB, 0.1 becomes -20 dB, and so on. Notice, by comparison of Equations (1.14) and (1.15), that the voltage gain of an amplifier in decibels is not the same as the power gain in decibels unless $R_i = R_L$.

Similarly, current gains are converted to decibels according to the equation

$$A_{i,dB} = 20 \log |A_i| \quad (1.16)$$

Voltages, Currents, and Other Quantities Expressed in Decibels

Electronics engineers often use decibel notation for voltages, currents, powers, or other quantities. To do so, a reference level must be stated or implied. The quantity to be converted to decibel notation is divided by the reference value, and the ratio is converted to decibels by taking 20 times the logarithm of the ratio for currents and voltages. Ten times the logarithm of the ratio is used for powers. Some commonly used reference levels and unit designations are 1 volt (dBV), 1 watt (dBW), and 1 milliwatt (dBmW). For example, +40 dBV is a designation for 100 V, -10 dBmW is equivalent to 0.1 mW, -40 dBW is also 0.1 mW, and so on. Often, we find dBmW abbreviated simply as dBm.

When there is the possibility of confusing decibel gain with ratio gain, we use the dB subscript to identify gains that are in decibels. On the other hand, when it is clear from the context that gains are in decibels, we dispense with the extra subscript. Units often indicate if gains or other quantities have been expressed in decibel form.

EXERCISE

1.7 An amplifier has an input resistance of $2\text{ k}\Omega$, an output resistance of $100\ \Omega$, and an open-circuit voltage gain of $A_{vo} = 2000$. If this amplifier is operated with a load of $R_L = 300\ \Omega$, find the power gain in decibels and the voltage gain $A_v = v_o/v_i$ in decibels.

Answer $A_{v\text{dB}} = 63.5\text{ dB}$ and $G = 71.8\text{ dB}$.

EXERCISE

1.8 Express a power of 5 mW in dBW and in dBm.

Answer -23 dBW and 6.99 dBm .

EXERCISE

1.9 A voltage is given as 23 dBV . Find the voltage.

Answer 14.12 V .

1.8 AMPLIFIER MODELS

The Current-Amplifier Model

Until now we have modeled amplifiers as shown in Figure 1.17, in which the gain property of the amplifier is represented by a voltage-controlled voltage source. An alternative model known as a **current-amplifier model** is shown in Figure 1.25. In this model, the gain property is represented by a current-controlled current source. As before, the input resistance accounts for the current that the amplifier draws from the signal source. The output resistance is now in parallel with the controlled source and accounts for the fact that the amplifier cannot supply a fixed current to an arbitrarily high load resistance.

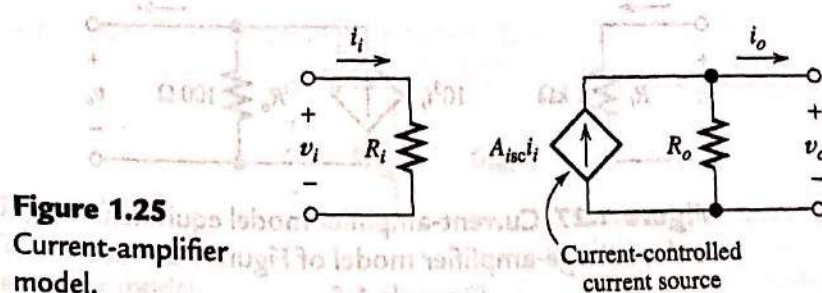


Figure 1.25
Current-amplifier
model.

The short-circuit current gain is the current gain with the output terminals of the amplifier short circuited.

If the load is a short circuit, no current flows through R_o , and the ratio of output current to input current is A_{isc} . For this reason, A_{isc} is known as the **short-circuit current gain**. An amplifier that is initially modeled as a voltage amplifier can also be modeled as a current amplifier. The input resistance and output resistance are the same for both models. The short-circuit current gain can be found from the voltage-amplifier model by connecting a short circuit to the output and computing the current gain.

Notice that we have converted the Thévenin circuit of the voltage-amplifier model to a Norton circuit in the current-amplifier model. Furthermore, we have substituted $v_i = R_i i_i$.

Example 1.5 Converting a Voltage Amplifier to a Current Amplifier

A certain amplifier is modeled by the voltage-amplifier model shown in Figure 1.26. Find the current-amplifier model.

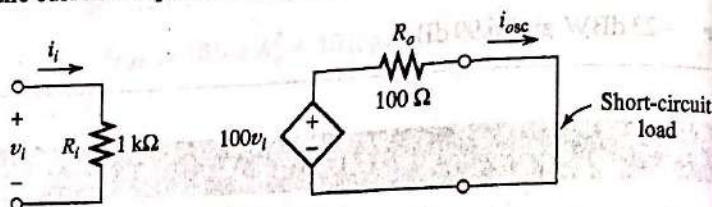


Figure 1.26 Voltage amplifier of Examples 1.5, 1.6, and 1.7.

To find the current amplifier model, we must determine the short-circuit current gain, the input impedance, and the output impedance.

SOLUTION In order to find the short-circuit current gain, we connect a short circuit to the output terminals of the amplifier as shown in Figure 1.26. Then we find

$$i_i = \frac{v_i}{R_i} \text{ and } i_{osc} = \frac{A_{vo} v_i}{R_o}$$

The short-circuit current gain is

$$A_{isc} = \frac{i_{osc}}{i_i} = A_{vo} \frac{R_i}{R_o} = 10^3$$

The resulting current-amplifier model is shown in Figure 1.27.

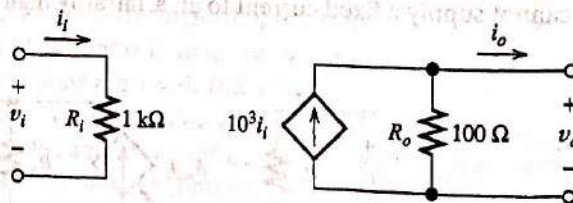


Figure 1.27 Current-amplifier model equivalent to the voltage-amplifier model of Figure 1.26. See Example 1.5.

EXERCISE

1.10 A certain amplifier modeled as a current amplifier has an input resistance of $1\text{ k}\Omega$, an output resistance of $20\ \Omega$, and a short-circuit current gain of 200. Find the parameters for the voltage-amplifier model.

Answer $A_{vo} = 4$, $R_i = 1\text{ k}\Omega$, and $R_o = 20\ \Omega$.

The Transconductance-Amplifier Model

Another model for an amplifier, known as a **transconductance-amplifier model**, is shown in Figure 1.28. In this case the gain is modeled by a voltage-controlled current source, and the gain parameter G_{msc} is called the **short-circuit transconductance gain**. G_{msc} is the ratio of the short-circuit output current i_{osc} to the input voltage v_i .

$$G_{msc} = \frac{i_{osc}}{v_i}$$

The units of transconductance gain are siemens. The input resistance and output resistance model the same effects as they do in the voltage-amplifier and current-amplifier models. A given amplifier can be modeled as a transconductance amplifier if the input resistance, output resistance, and short-circuit transconductance gain can be found.

The input resistance is the resistance seen looking into the input terminals. It has the same value for all models of a given amplifier. Similarly, the output resistance is the Thévenin resistance seen looking back into the output terminals and is the same for all the models.

The units of transconductance gain are siemens.

Example 1.6 Determining the Transconductance-Amplifier Model Parameters

Find the transconductance model for the amplifier of Figure 1.26.

SOLUTION The short-circuit transconductance gain is given by

$$G_{msc} = \frac{i_{osc}}{v_i}$$

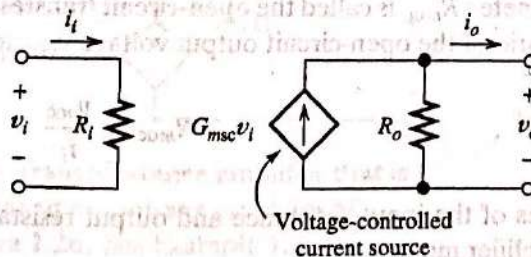


Figure 1.28
Transconductance-amplifier model.

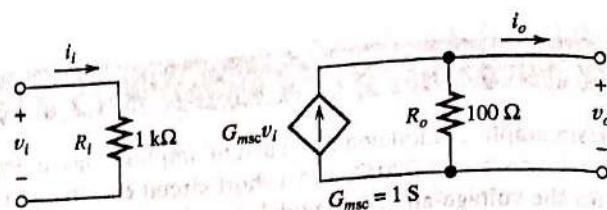


Figure 1.29 Transconductance amplifier equivalent of the voltage amplifier of Figure 1.26. See Example 1.6.

The output current for a short-circuit load is

$$i_{osc} = \frac{A_{vo} v_i}{R_o}$$

Thus, we find that

$$G_{msc} = \frac{A_{vo}}{R_o} = 1.0 \text{ S}$$

The resulting amplifier model is shown in Figure 1.29.

EXERCISE

1.11 A current amplifier has an input resistance of 500Ω , an output resistance of 50Ω , and a short-circuit current gain of 100. Find the parameters for the transconductance-amplifier model.

Answer $G_{msc} = 0.2 \text{ S}$, $R_i = 500 \Omega$, $R_o = 50 \Omega$.

Transresistance gain has units of ohms.

The Transresistance-Amplifier Model

Finally, we can model an amplifier as a **transresistance amplifier** as shown in Figure 1.30. In this case, the gain property is modeled by a current-controlled voltage source. The gain parameter R_{moc} is called the **open-circuit transresistance gain** and has units of ohms. It is the ratio of the open-circuit output voltage v_{oc} to the input current i_i :

$$R_{moc} = \frac{v_{oc}}{i_i}$$

The values of the input resistance and output resistance are the same as in any of the other amplifier models.

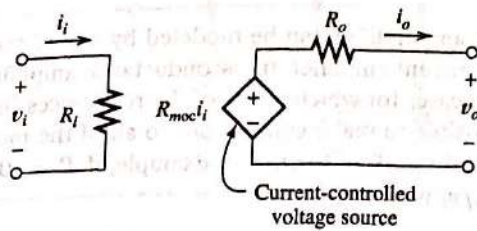


Figure 1.30 Transresistance-amplifier model.

Example 1.7 Determining the Transresistance-Amplifier Model Parameters

Find the transresistance-amplifier model for the amplifier shown in Figure 1.26.

SOLUTION With an open-circuit load, the output voltage is

$$v_{oc} = A_{vo} v_i$$

and the input current is

$$i_i = \frac{v_i}{R_i}$$

Thus, we find the transresistance gain as

$$R_{moc} = \frac{v_{oc}}{i_i} = A_{vo} R_i = 100 \text{ k}\Omega$$

The resulting transresistance model of the amplifier is shown in Figure 1.31. □

EXERCISE

1.12 An amplifier has an input resistance of $1 \text{ M}\Omega$, and an output resistance of 10Ω , $G_{msc} = 0.05 \text{ S}$. Find R_{moc} for this amplifier.

Answer $R_{moc} = 500 \text{ k}\Omega$.

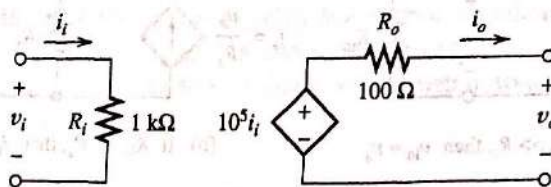


Figure 1.31 Transresistance amplifier that is equivalent to the voltage amplifier of Figure 1.26. See Example 1.7.

... an amplifier can be modeled by any of the following four models: voltage amplifier, current amplifier, transconductance amplifier, and transresistance amplifier.

We have seen that an amplifier can be modeled by any of the following four models: voltage amplifier, current amplifier, transconductance amplifier, and transresistance amplifier. However, in cases for which either of the resistances (input or output) is zero or infinity, it is not possible to make conversions to all of the models, because the gain parameter is not defined for all of them. For example, if $R_i = 0$, then $v_i = 0$, and the voltage gain $A_{vo} = v_o/v_i$ is not defined.

Applications Calling for High or Low Input Impedance

Sometimes we have an application for an amplifier that calls for the internal voltage produced by the source to be amplified. For example, an electrocardiograph amplifies and records the small voltages generated by a subject's heart. These voltages are detected by placing electrodes on the subject's skin. The Thévenin impedance seen looking back into the electrodes is variable from subject to subject and can be quite high in magnitude (mainly due to the resistance of the subject's skin). If the input impedance of the electrocardiograph is low, a variable reduction in voltage occurs because of loading. Thus, the amplitude of the signal can be affected by the contact resistance of the electrodes with the skin and therefore does not truly represent the electrical activity of the heart. On the other hand, if the input impedance of the electrocardiograph is much higher than the source impedance, the actual voltage produced by the heart appears at the input terminals. Hence, the input impedance of an electrocardiograph amplifier should be very high.

Other applications call for the amplifier to respond to the short-circuit current of a source. In that case, a very low input impedance is needed. An example is an electronic ammeter inserted in series with a circuit to measure current. Usually, we do not want the ammeter to change the current that is being measured. This is accomplished by designing the ammeter to have a low enough input impedance so that it does not change the impedance of the circuit significantly.

To summarize, if the input impedance of an amplifier is much higher than the internal impedance of the source, the voltage produced across the input terminals is nearly the same as the internal source voltage. This is illustrated in Figure 1.32a. On the other hand, if the input impedance is very low, the input current is nearly equal to the short-circuit current of the source. This is illustrated in Figure 1.32b.

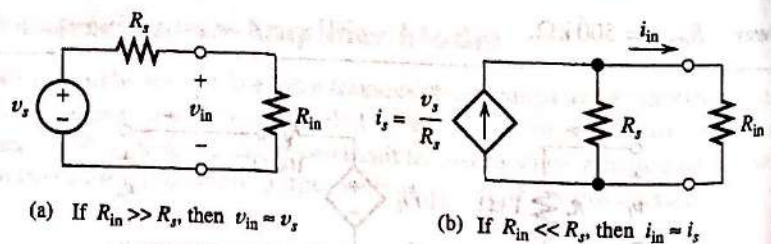


Figure 1.32 If we want to sense the open-circuit voltage of a source, the amplifier should have a high input resistance, as in (a). To sense short-circuit current, low input resistance is called for, as in (b).

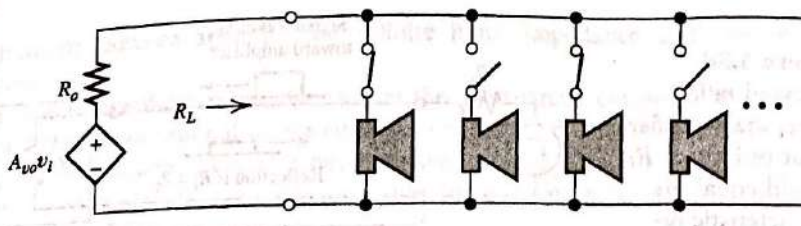


Figure 1.33 If the amplifier output impedance R_o is much less than the (lowest) load resistance, the load voltage is nearly independent of the number of switches closed.

Applications Calling for High or Low Output Impedance

Diverse requirements for output impedance also occur. For example, we could have an audio amplifier that supplies background music to loudspeakers in many rooms of an office building, as shown in Figure 1.33. A switch is provided so that each loudspeaker can be turned off independently of the others (by opening its switch). Therefore, the load impedance presented to the amplifier is quite variable, depending on the number of loudspeakers turned on. If the amplifier output impedance is high compared with the load impedance, the voltage supplied depends on the load impedance. Thus, as loudspeakers are turned off, the voltage applied to the others becomes higher, resulting in louder music. This effect could be undesirable. On the other hand, if the output impedance of the amplifier is very low compared with the load impedance, the output voltage is nearly independent of the load. Thus, in this situation, a low output impedance is better.

Another example occurs in optical communication systems, in which a light-emitting diode (LED) is used to produce a light wave with intensity proportional to a message signal such as a voice waveform. Over a certain range of operation, the intensity of the light output of an LED is proportional to the current through it. Because LEDs have a nonlinear relationship between voltage and current, light intensity is *not* proportional to the voltage across the LED. Thus, it is desirable to force a current proportional to the message waveform to flow through the diode. This can be achieved by designing an amplifier with a very high output impedance to drive the LED. (On the other hand, if a very low output impedance were used, then the voltage supplied to the diode would be proportional to the input signal to the amplifier, but because of the nonlinear relationship between current and voltage for the diode, the light output would no longer be proportional to the message.)

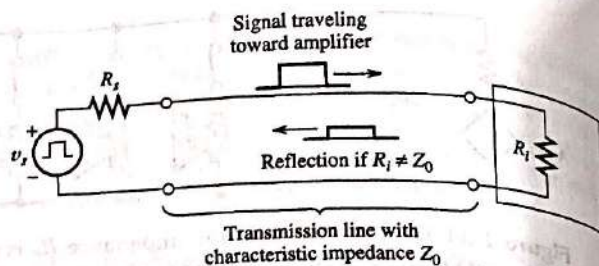
To summarize, we can force a desired voltage waveform to appear across a variable load by designing the amplifier to have a very low output impedance compared with the load impedance. On the other hand, we can force a given current waveform through a variable load by designing the amplifier to have a very high output impedance compared with the load impedance.

Applications Calling for a Particular Impedance

Not all applications call for amplifiers with either very small or very large impedances. For example, consider an amplifier whose input is connected to a source by a transmission

Usually, low output impedance is best if the load impedance is variable.

Figure 1.34
To avoid reflections, the amplifier input resistance R_i should equal the characteristic resistance Z_0 of the transmission line.



line, as shown in Figure 1.34. Coaxial cable is an example of a familiar transmission line that is often used for distributing signals to television receivers.

Each type of transmission line has a **characteristic impedance**, which is $75\ \Omega$ for coaxial cable used to distribute television signals. A signal traveling along a transmission line is partially reflected and travels back toward the source, unless the transmission line is terminated in its characteristic impedance. This concept is illustrated in Figure 1.34. When a transmission line is used to connect an antenna to a television receiver, the reflections can be reflected again at the antenna, so the signal arrives at the receiver a second time. The extra received signals are delayed because of the round-trip travel along the transmission line and can cause the quality of the picture to degrade. (The effect of the reflection is a faint image known as a "ghost" slightly to the right-hand side of the main image.) Therefore, it is important for the input impedance of the television set to be equal to the characteristic impedance of the transmission line so that reflections do not occur.

The output impedance of an audio amplifier is another characteristic that sometimes calls for an intermediate value. The frequency response of a loudspeaker depends on the output impedance of the amplifier driving it. Thus, if high fidelity is a primary consideration, we should design the amplifier so that it has the output impedance that gives the most nearly constant response versus frequency.

1.9 IDEAL AMPLIFIERS

We have seen that certain applications call for amplifiers with very high or very low input impedance (compared with the source impedance) and very high or very low output impedance (compared with the load impedance). Such amplifiers can be classified as follows:

Ideal amplifier types defined.

An **ideal voltage amplifier** senses the open-circuit voltage of the source and produces an amplified voltage across the load. This amplified voltage is independent of the load impedance. Thus, the ideal voltage amplifier has infinite input impedance (so the open-circuit source voltage appears across the input terminals) and zero output impedance (so the output voltage is independent of the load impedance).

An **ideal current amplifier** senses the short-circuit current of the source and forces an amplified version of this current to flow through the load. Thus, an ideal current amplifier has zero input impedance and infinite output impedance.

An **ideal transconductance amplifier** senses the open-circuit voltage of the source and forces a current proportional to this voltage to flow through the load. Thus, the

ideal transconductance amplifier has infinite input impedance and infinite output impedance.

An ideal transresistance amplifier senses the short-circuit current of the source and forces a voltage proportional to this current to appear across the load. Thus, the ideal transresistance amplifier has zero input impedance and zero output impedance.

Table 1.1 shows the input impedance, output impedance, and gain parameter for each type of ideal amplifier.

Classifying Real Amplifiers

In practice, amplifiers do not have either zero or infinite impedances. However, real amplifiers can often be classified as approximately ideal amplifiers. For example, if the input impedance is very large (compared with the source impedance) and the output impedance is very small (compared with the load impedance), we have an approximate ideal voltage amplifier.

Notice that a given amplifier cannot be classed as an approximately ideal amplifier, unless the source and load impedances to be encountered are known in advance. For example, an amplifier with an input impedance of $1000\ \Omega$ and an output impedance of $100\ \Omega$ is classed as an approximately ideal voltage amplifier if the source impedances to be encountered are much less than $1000\ \Omega$ and the load impedances are much greater than $100\ \Omega$. On the other hand, if the source impedances are on the order of $1\ \text{M}\Omega$ and the load impedances are on the order of $1\ \Omega$, the same amplifier is properly classed as an approximately ideal current amplifier.

In general, the "middle range" of impedances in low-power electronic circuits runs from 1 to $100\ \text{k}\Omega$. Impedances less than $100\ \Omega$ are usually considered to be small, and impedances greater than $1\ \text{M}\Omega$ are classed as large. Thus, we would usually be inclined to classify an amplifier with an input impedance of $10\ \Omega$ and an output impedance of $2\ \text{M}\Omega$ as an approximately ideal current amplifier. However, we might want to change this classification, depending on the actual load and source impedances.

Large and small impedance ranges.

EXERCISE

1.13 A certain amplifier has an input resistance of $R_i = 1\ \text{k}\Omega$ and an output resistance of $R_o = 1\ \text{k}\Omega$. R_s is the source resistance, and R_L is the load. Classify the amplifier if (a) R_s is less than $10\ \Omega$ and R_L is greater than $100\ \text{k}\Omega$; (b) R_s is greater than $100\ \text{k}\Omega$ and R_L is less than $10\ \Omega$; (c) R_s is less than $10\ \Omega$ and R_L is less than $10\ \Omega$; (d) R_s is greater than $100\ \text{k}\Omega$ and R_L is greater than $100\ \text{k}\Omega$; (e) R_s is approximately $1\ \text{k}\Omega$ and R_L is less than $10\ \Omega$.

Table 1.1. Characteristics of ideal amplifiers.

Amplifier Type	Input Impedance	Output Impedance	Gain Parameter
Voltage	∞	0	A_{vo}
Current	0	∞	A_{isc}
Transconductance	∞	∞	G_{msc}
Transresistance	0	0	R_{moc}

Answer (a) Approximately ideal voltage amplifier; (b) approximately ideal current amplifier; (c) approximately ideal transconductance amplifier; (d) approximately ideal transresistance amplifier; (e) for this source resistance, the amplifier does not fit into any ideal amplifier category.

1.10 AMPLIFIER FREQUENCY RESPONSE

Signals as a Sum of Sinusoids of Various Frequencies

One of the most important concepts in electrical engineering is that any signal can be considered to consist of a sum of sinusoidal components having various frequencies, phases, and amplitudes.

One of the most important concepts in electrical engineering is that any signal can be considered to consist of a sum of sinusoidal components having various frequencies, phases, and amplitudes. The **spectrum** of a signal gives the amplitudes and phases of the components versus frequency. For example, audible sounds have significant components over a frequency range from about 20 Hz to 15 kHz. Video signals have components that range from dc to about 4.5 MHz. Table 1.2 lists some other signals and the frequency ranges of their components.

Fourier analysis is a collection of mathematical techniques for finding the spectra of various types of signals. For example, Fourier series apply to periodic signals (i.e., signals that repeat a pattern of amplitudes). The symmetrical square wave shown in Figure 1.35a is periodic with period T , and its Fourier series is given by

$$v(t) = \frac{4A}{\pi} \left[\sin(\omega_0 t) + \frac{1}{3} \sin(3\omega_0 t) + \frac{1}{5} \sin(5\omega_0 t) + \dots \right] \quad (1.17)$$

where A is the amplitude of the square wave and $\omega_0 = 2\pi/T$ is the **fundamental angular frequency**. Figure 1.35b shows the result of adding the first five terms in this series. Notice the close approximation to the original square wave. As more terms are added, the approximation becomes better. Notice that the Fourier series of the square wave [given by Equation (1.17)] displays the frequency, amplitude, and phase of each component. Thus, the Fourier series provides a mathematical technique for finding the spectrum of a periodic signal.

Table 1.2. Frequency ranges of selected signals.

Electrocardiogram	0.05 to 100 Hz
Audible sounds	20 Hz to 15 kHz
Analog video signals (United States standards)	Dc to 4.5 MHz
AM radio broadcasting	540 to 1600 kHz
Channel 2 television	54 to 60 MHz
FM radio broadcasting	88 to 108 MHz
UHF television (Channels 14 through 69)	470 to 806 MHz
Cellular telephone	824 to 891.5 MHz
Satellite television downlinks	3.7 to 4.2 GHz

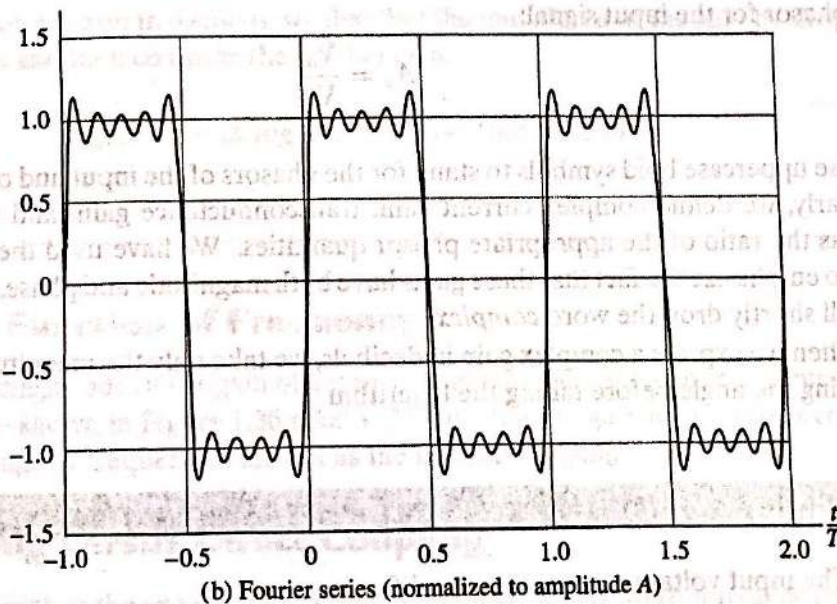
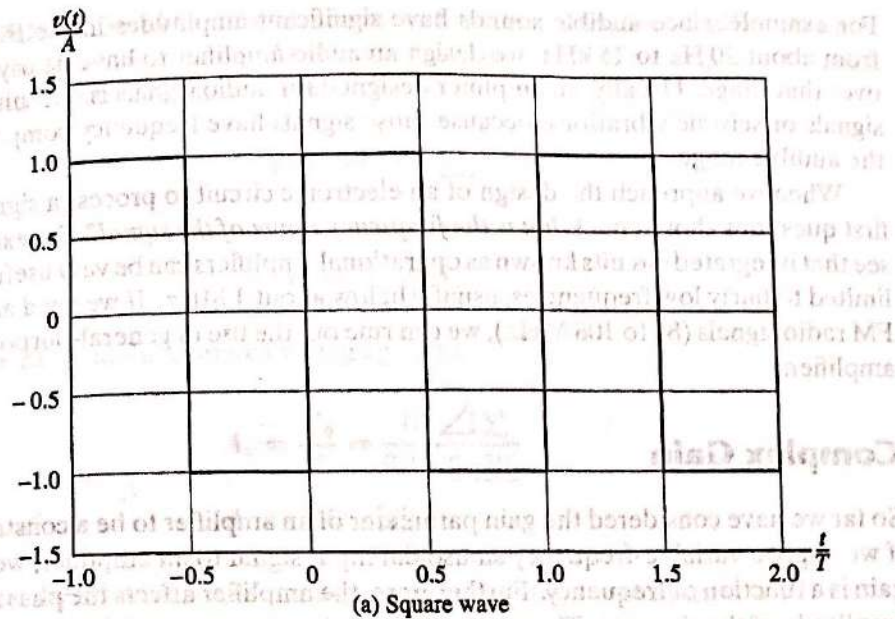


Figure 1.35 Periodic square wave and the sum of the first five terms of its Fourier series.

A linear system is a system to which superposition applies. Linear systems can be analyzed to find how the amplitude and phase of an input sinusoid of a given frequency are changed in passing through the system. This information is contained in the transfer function of the system. (You either have studied this, or soon will, in your other electrical engineering courses.) Hence, if we know the spectrum of a signal and the transfer function of a system, we can draw some conclusions about the effects of the system on the signal.

A linear system is a system to which superposition applies.

When we approach the design of an electronic circuit to process a signal, one of our first questions should be, *What is the frequency range of the signal?*

For example, since audible sounds have significant amplitudes in the frequency range from about 20 Hz to 15 kHz, we design an audio amplifier to have nearly constant gain over that range. Usually, an amplifier designed for audio signals is not suitable for video signals or seismic vibrations, because those signals have frequency components outside the audible range.

When we approach the design of an electronic circuit to process a signal, one of our first questions should be, *What is the frequency range of the signal?* For example, we will see that integrated circuits known as operational amplifiers can be very useful, but they are limited to fairly low frequencies, usually below about 1 MHz. If we need an amplifier for FM radio signals (88 to 108 MHz), we can rule out the use of general-purpose operational amplifiers.

Complex Gain

So far we have considered the gain parameter of an amplifier to be a constant. However, if we apply a variable-frequency sinusoidal input signal to an amplifier, we will find that gain is a function of frequency. Furthermore, the amplifier affects the phase as well as the amplitude of the sinusoid. Therefore, we now give a more general definition of amplifier gain. We define the complex gain to be the ratio of the phasor for the output signal to the phasor for the input signal:

$$A_v = \frac{V_o}{V_i} \quad (1.18)$$

We use uppercase bold symbols to stand for the phasors of the input and output voltages.

We use uppercase bold symbols to stand for the phasors of the input and output voltages. Similarly, we define complex current gain, transconductance gain, and transresistance gain as the ratio of the appropriate phasor quantities. We have used the term *complex gain* to emphasize the fact that these gains have both magnitude and phase. For simplicity, we will shortly drop the word *complex*.

When we express a complex gain in decibels, we take only the magnitude of the gain, dropping the angle before taking the logarithm.

Example 1.8 Determining Voltage Gain as a Complex Number

The input voltage to a certain amplifier is

$$v_i(t) = 0.1 \cos(2000\pi t - 30^\circ)$$

and the output voltage is

$$v_o(t) = 10 \cos(2000\pi t + 15^\circ)$$

Find the complex voltage gain of the amplifier and express the magnitude of the gain in decibels.

SOLUTION The phasor for the input voltage is a complex number whose magnitude is the peak value of the sinusoidal signal and whose angle is the phase angle of the sinusoidal signal. Thus,

$$V_i = 0.1 \angle -30^\circ$$

Similarly,

$$V_o = 10 \angle 15^\circ$$

Now, we can find the complex voltage gain as

$$A_v = \frac{V_o}{V_i} = \frac{10 \angle 15^\circ}{0.1 \angle -30^\circ}$$

$$A_v = 100 \angle 45^\circ$$

The meaning of this complex voltage gain is that the output signal is 100 times larger in amplitude than the input signal. Furthermore, the output signal is phase shifted by 45° relative to the input signal.

To express gain in decibels, we first find the magnitude of the gain by dropping the angle and then compute the decibel gain:

$$|A_v|_{\text{dB}} = 20 \log |A_v| = 20 \log(100) = 40 \text{ dB}$$

Gain as a Function of Frequency

If we plot the magnitude of the gain of a typical amplifier against frequency, a curve such as one of those shown in Figure 1.36 results. Notice that the gain magnitude is constant over a wide range of frequencies known as the **midband region**.

AC Coupling Versus Direct Coupling

In some cases, such as the one shown in Figure 1.36a, the gain drops to zero at dc (zero frequency). Such amplifiers are said to be **ac coupled**, because only ac signals are amplified. These amplifiers are often constructed by cascading several amplifier circuits or stages that are connected together by **coupling capacitors** so that the dc voltages of the amplifier circuits do not affect the signal source, adjacent stages, or the load. This arrangement is illustrated in Figure 1.37. Sometimes transformers are used to couple individual stages together, which also leads to an ac-coupled amplifier with zero gain at dc.

Other amplifiers have constant gain all the way down to dc, as shown in Figure 1.36b. They are said to be **dc coupled** or **direct coupled**. Amplifiers that are realized as integrated circuits are almost always dc coupled because the capacitors or transformers needed for ac coupling cannot be fabricated in integrated form.

If the dc component of a signal is important, we need a direct-coupled amplifier.

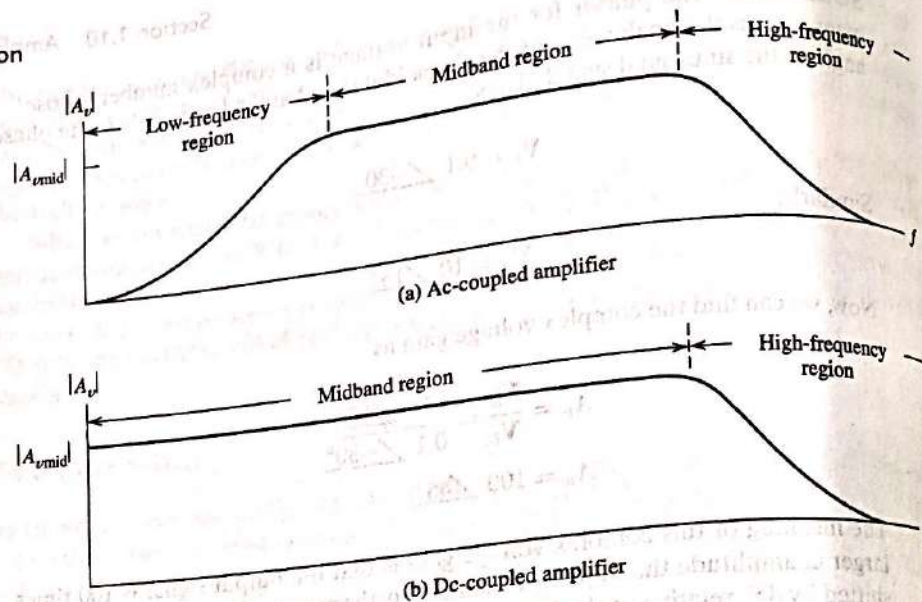


Figure 1.36 Gain versus frequency.

Audio amplifiers are ac coupled because audible sounds span the frequency range from about 20 Hz to 15 kHz. Consequently, there is no need to provide gain down to dc. Furthermore, it is not desirable to apply dc voltages to the loudspeakers.

Electrocardiograph amplifiers are deliberately ac coupled, because a dc voltage of nearly a volt often appears at the input, due to electrochemical contact potentials developed by the electrodes. The ac signal generated by the heart is on the order of 1 mV; therefore, the gain of the amplifier is high—typically 1000 or more. A 1-V dc input would make the amplifier try to produce an output of 1000 volts. It would be difficult (and highly undesirable) to design an amplifier capable of such large outputs. Hence, it is necessary to ac couple the input circuit of an electrocardiograph to prevent the dc component from overloading the amplifier.

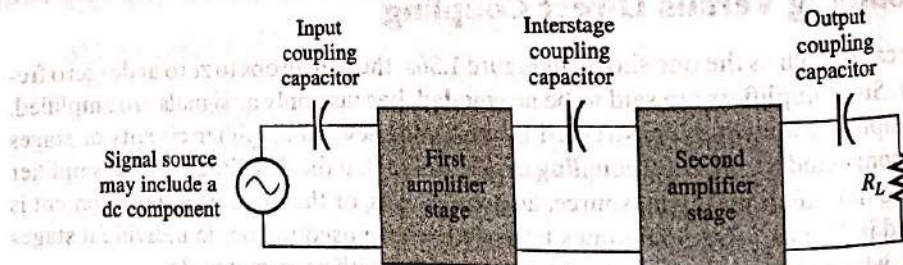


Figure 1.37 Capacitive coupling prevents a dc input component from affecting the first stage, dc voltages in the first stage from reaching the second stage, and dc voltages in the second stage from reaching the load.

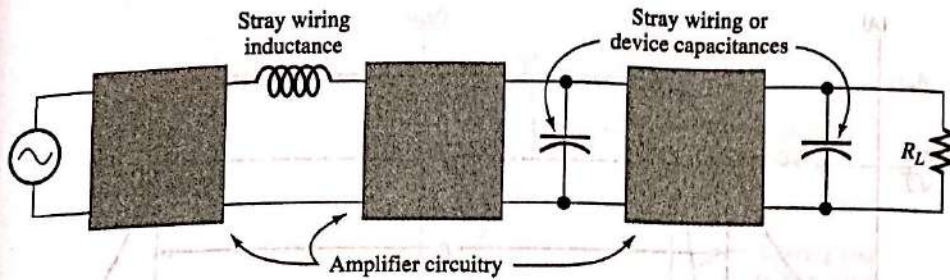


Figure 1.38 Capacitance in parallel with the signal path and inductance in series with the signal path reduce gain in the high-frequency region.

Amplifiers for video signals need to be dc coupled because video signals have frequency components from dc to about 4.5 MHz. Dark pictures result in a different dc component than bright pictures. To obtain pictures with the proper brightness, it is necessary to use a dc-coupled amplifier to preserve the dc component. (Actually, certain video signals are special cases for which it is possible to use an ac-coupled amplifier, followed by a wave-shaping circuit known as a dc restorer that reinserts the proper dc component.)

The High-Frequency Region

As indicated in Figures 1.36a and b, the gain of an amplifier always drops off at high frequencies. This drop is caused either by small amounts of capacitance in parallel with the signal path, or by small inductances in series with the signal path as illustrated in Figure 1.38. Recall that the impedance of a capacitor is inversely proportional to the frequency, resulting in an effective short circuit at sufficiently high frequencies. The impedance of an inductor is proportional to frequency, so it becomes an open circuit at very high frequencies.

Some of these small capacitances occur between signal-carrying conductors and ground. Other capacitances are integral parts of the active devices (transistors) necessary for amplification. Small inductances result from the magnetic fields surrounding the conductors in the circuit. For example, a critically placed piece of wire one-half inch long can have enough inductance to limit severely the frequency response of an amplifier intended to operate in the gigahertz range.

The gain of an amplifier always drops off as frequency approaches infinity.

Half-Power Frequencies and Bandwidth

Usually, we specify the approximate useful frequency range of an amplifier by giving the frequencies for which the voltage (or current) gain magnitude is $1/\sqrt{2}$ times the midband gain magnitude. These are known as the **half-power frequencies**, because the output power level is half the value for the midband region if a constant-amplitude, variable-frequency input test signal is used. Expressing the factor $1/\sqrt{2}$ in decibels, we have $20 \log(1/\sqrt{2}) = -3.01$ dB. Thus, at the half-power frequencies, the voltage (or current) gain is approximately 3 dB lower than the midband gain. The bandwidth B of an amplifier is the distance between the half-power frequencies. These definitions are illustrated in Figure 1.39.

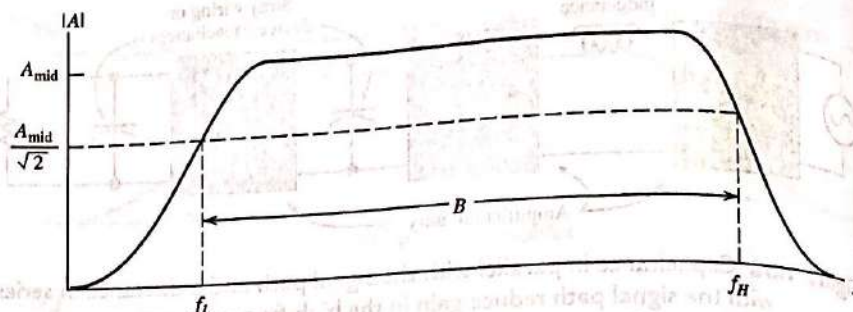


Figure 1.39 Gain versus frequency for a typical amplifier showing the upper and lower half-power (3-dB) frequencies (f_H and f_L) and the half-power bandwidth B .

Wideband Versus Narrowband Amplifiers

Amplifiers that either are dc coupled or have a lower half-power frequency that is a small fraction of the upper half-power frequency are called **wideband** or **baseband amplifiers**. Wideband amplifiers are used for signals that occupy a wide range of frequencies, such as audio signals (20 Hz to 15 kHz) or video signals (dc to 4 MHz).

On the other hand, the frequency response of an amplifier is sometimes deliberately limited to a small bandwidth compared with the center frequency. Such an amplifier is called a **narrowband** or **bandpass amplifier**. The gain versus frequency response of a bandpass amplifier is shown in Figure 1.40. Bandpass amplifiers are used in radio receivers, because it is desired to amplify the signal from one transmitter and reject the signals from other transmitters in adjacent frequency ranges.

Pulse Response

...amplification of pulses calls for a wideband amplifier.

Often we need to amplify a pulse signal such as the one shown in Figure 1.41a. Pulses contain components spread over a wide range of frequencies; therefore, amplification of pulses calls for a wideband amplifier. A typical amplified output pulse is shown in

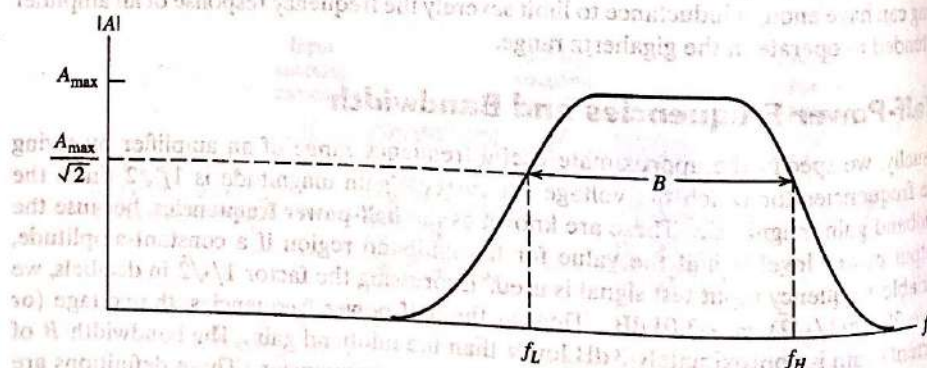


Figure 1.40 Gain magnitude versus frequency for a typical bandpass amplifier.

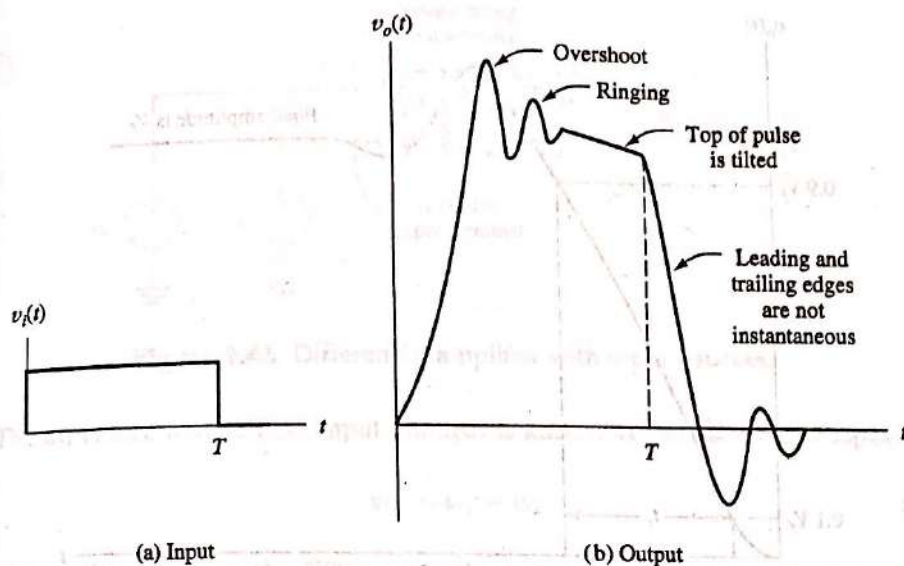


Figure 1.41 Input pulse and typical ac-coupled broadband amplifier output.

Figure 1.41b. The output waveform differs from the input in several important respects: The pulse displays **overshoot** and **ringing**, the leading and trailing edges are gradual rather than abrupt, and if the amplifier is ac coupled, the top of the output pulse is **tilted**.

Rise Time

The gradual rise of the leading edge of the amplifier response is quantified by giving the **rise time** t_r , which is the interval between the point t_{10} at which the output reaches 10% of the eventual amplitude and the point t_{90} at which the output is 90% of the final value. The rise time is illustrated in Figure 1.42.

The rounding of the leading edge can be attributed to the roll-off of gain in the high-frequency region. A rule-of-thumb relationship between the half-power bandwidth B and the rise time t_r of a wideband amplifier is

$$t_r \cong \frac{0.35}{B} \quad (1.19)$$

This relationship is not exact for all types of wideband amplifiers, but it is a useful guide for estimating performance.

Because pulse amplifiers are broadband, the bandwidth is almost equal to the upper half-power frequency. Thus, it is mainly the high-frequency characteristics of the amplifier that restrict rise time. For example, we can use Equation 1.19 to estimate the bandwidth needed for the video amplifiers in television receivers. Television pictures are produced by electron beams that scan the faces of the picture tubes in a series of horizontal lines spaced from top to bottom. As it scans, the electron beam strikes phosphors on the inside face of the tube, creating light. (Actually, there are three beams—one for each primary color.) The intensity of the beam is modulated by a video signal to produce bright and dark regions. From a knowledge of the number of scan lines, the scan rate, and other

Relationship between rise time and upper half-power frequency.

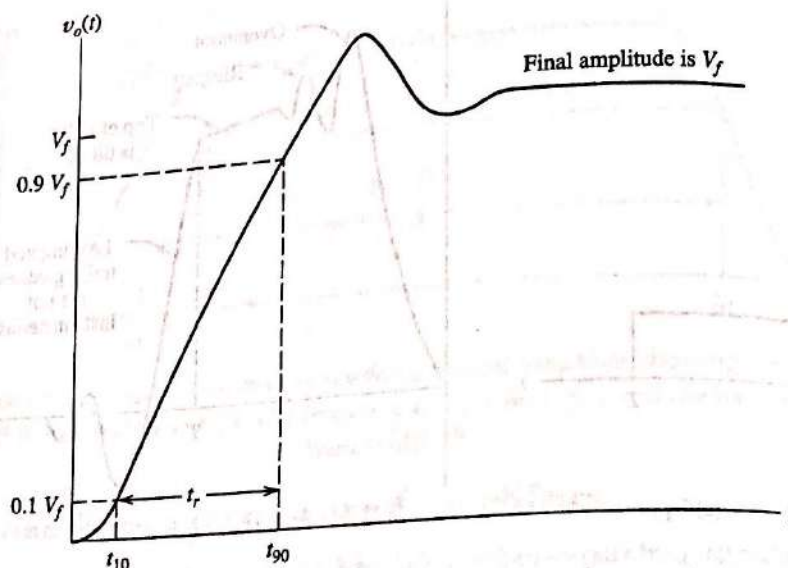


Figure 1.42 Rise time of the output pulse. (Note: No tilt is shown. When tilt is present, some judgement is necessary to estimate the amplitude V_f .)

information, it is estimated that the rise time required for video amplifiers is about 85 ns, assuming United States broadcast standards. On the basis of this information, we can determine the bandwidth required for video amplifiers by the use of Equation 1.19:

$$B = \frac{0.35}{t_r} = \frac{0.35}{85 \times 10^{-9}} = 4.1 \text{ MHz}$$

which is very close to the actual video bandwidth used in television receivers.

1.11 DIFFERENTIAL AMPLIFIERS

Differential amplifiers have many important applications.

Thus far, we have encountered amplifiers that have only one input source. Now we consider **differential amplifiers** that have two input sources, as shown in Figure 1.43. An ideal differential amplifier produces an output voltage proportional to the difference between the input voltages:

$$\begin{aligned} v_o(t) &= A_d[v_{i1}(t) - v_{i2}(t)] \\ &= A_d v_{i1}(t) - A_d v_{i2}(t) \end{aligned} \quad (1.20)$$

Notice that the gain is positive for the voltage applied to terminal 1 and negative for the voltage applied to terminal 2. Therefore, terminal 2 is called an **inverting input**, and terminal 1 is called a **noninverting input**. Inverting input terminals are marked with a $-$ sign and noninverting input terminals with a $+$ sign, as indicated in Figure 1.43.

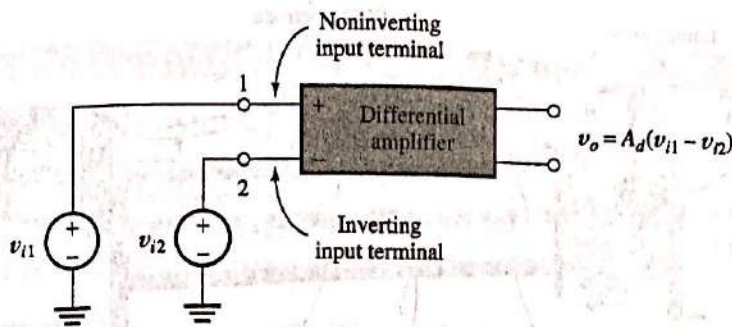


Figure 1.43 Differential amplifier with input sources.

The difference between the input voltages is known as the **differential input signal**

v_{id} :

$$v_{id} = v_{i1} - v_{i2} \quad (1.21)$$

We refer to the gain A_d as the **differential gain**, and we can therefore write the output of the ideal differential amplifier as

$$v_o = A_d v_{id} \quad (1.22)$$

The **common-mode input signal** v_{icm} is the average of the input voltages and is given by

$$v_{icm} = \frac{1}{2}(v_{i1} + v_{i2}) \quad (1.23)$$

The original input sources v_{i1} and v_{i2} can be replaced by the equivalent system of sources shown in Figure 1.44. Thus, we can consider the inputs to the differential amplifier to be the differential signal v_{id} and the common-mode signal v_{icm} .

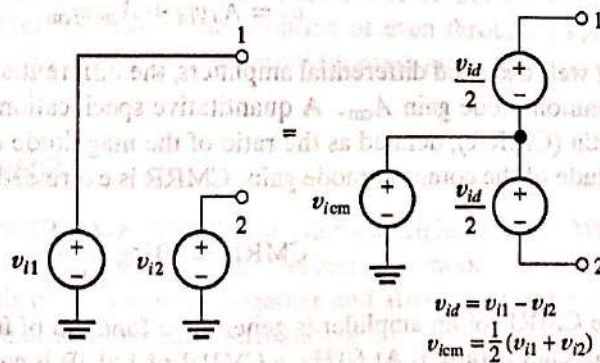
Sometimes, we have a small differential signal that we wish to amplify, but a large common-mode signal is also present that is of no interest. A good example of this is in recording the electrocardiogram (ECG) of a patient. Imagine a patient laying on a bed insulated from electrical ground, as shown in Figure 1.45. A differential signal, generated by the patient's heart, appears between the electrodes when they are placed in contact with each of the patient's arms. This is the signal of interest to the cardiologist. Also, a

Differential-mode signal and differential gain defined.

Common-mode signal and common-mode gain defined.

... we can consider the inputs to the differential amplifier to be the differential signal v_{id} and the common-mode signal v_{icm} .

Figure 1.44
The input sources v_{i1} and v_{i2} can be replaced by the equivalent sources v_{icm} and v_{id} .



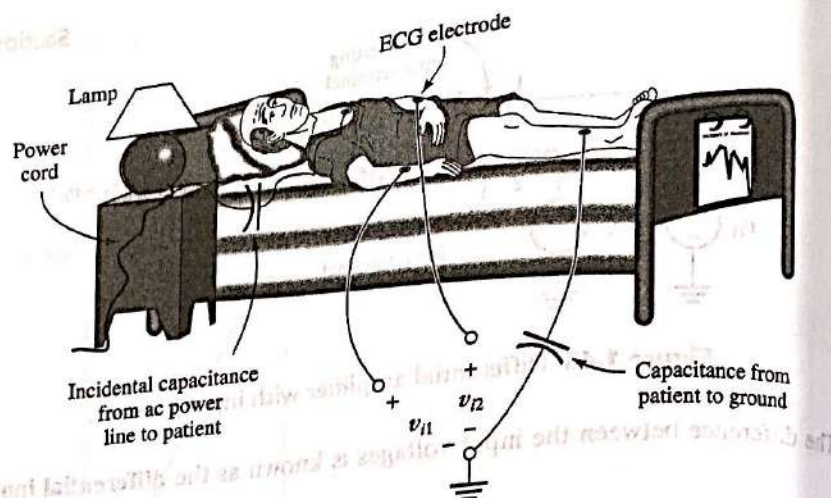


Figure 1.45 Electrocardiographs encounter large 60-Hz common-mode signals.

A large 60-Hz common-mode signal is typically present between each electrode and the local power-system ground. This occurs because the patients are connected to the 60-Hz power line by very small incidental capacitances between their bodies and the line. Similar small capacitances connect the patient to ground. This network of stray capacitances forms a voltage-divider network, so the patient's body is at a significant fraction of the power-line voltage with respect to ground. (You may have observed this 60-Hz common-mode signal in the laboratory if you have touched the input terminals of a high-input-impedance ac meter or oscilloscope.) Thus, at the input to the electrocardiograph amplifier, there exists a differential signal of about 1 mV and a 60-Hz common-mode signal of several tens of volts. Ideally, the electrocardiograph should respond only to the differential signal.

Common-Mode Rejection Ratio

Unfortunately, real differential amplifiers respond to both the common-mode signal and the differential signal. As before, the gain for the differential signal is denoted as A_d . If we denote the gain for the common-mode signal as A_{cm} , the output voltage of a real differential amplifier is given by

$$v_o = A_d v_{id} + A_{cm} v_{icm} \quad (1.24)$$

For well-designed differential amplifiers, the differential gain A_d is much larger than the common-mode gain A_{cm} . A quantitative specification is the **common-mode rejection ratio (CMRR)**, defined as the ratio of the magnitude of the differential gain to the magnitude of the common-mode gain. CMRR is expressed in decibels as

$$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{cm}|} \quad (1.25)$$

The CMRR of an amplifier is generally a function of frequency, becoming lower as the frequency is raised. At 60 Hz, a CMRR of 120 dB is considered good.

Key equation defining common-mode rejection ratio.

Example 1.9 Determination of CMRR Specification

Find the minimum CMRR for an electrocardiograph amplifier if the differential gain is 1000, the desired differential input signal is 1 mV peak, the common-mode input signal is a 100-V-peak 60-Hz sine wave, and it is desired that the output contain a peak common-mode contribution that is 1% or less of the peak output caused by the differential signal.

SOLUTION Because the peak differential input is 1 mV and the differential gain is 1000, the peak output of the desired signal is 1 V. To meet the required specification, the common-mode output signal must have a peak value of 0.01 V or less. Thus, the common-mode gain is

$$A_{cm} = \frac{0.01 \text{ V}}{100 \text{ V}} = 10^{-4} = -80 \text{ dB}$$

(The common-mode gain actually amounts to attenuation.)

Now we can find the CMRR by applying Equation (1.25):

$$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{cm}|} = 20 \log \frac{1000}{10^{-4}} = 140 \text{ dB}$$

Thus, an electrocardiograph requires a very good CMRR specification. $\square$

Perhaps we should note in passing that another simpler—but dangerous—approach exists in regard to solving the common-mode problem for the electrocardiograph: to short out the common-mode signal by attaching another electrode to the patient and connecting it to the power-system ground. This would reduce the 60-Hz interference to a very low level, so an amplifier with a much less stringent CMRR specification could be used. However, once the patient is in good electrical contact with the power-system ground, any contact with power-line voltages is potentially fatal. This is particularly true if the patient is too ill to protest. Even small currents imperceptible under ordinary circumstances can be fatal if conducted directly to the patient's heart. Such small currents can be conducted through other medical instrumentation or even through a surgeon's hands. *Keeping the patient isolated from ground provides some measure of protection from this problem.*

Measurement of CMRR

Measurements to find the CMRR of an amplifier are fairly straightforward. We must find both the differential and common-mode gains. The common-mode gain is found by connecting the input terminals of the amplifier together and attaching a test source as shown in Figure 1.46. Notice that with the input terminals of the amplifier connected together, the differential signal v_{id} is zero, and any output is caused by the common-mode

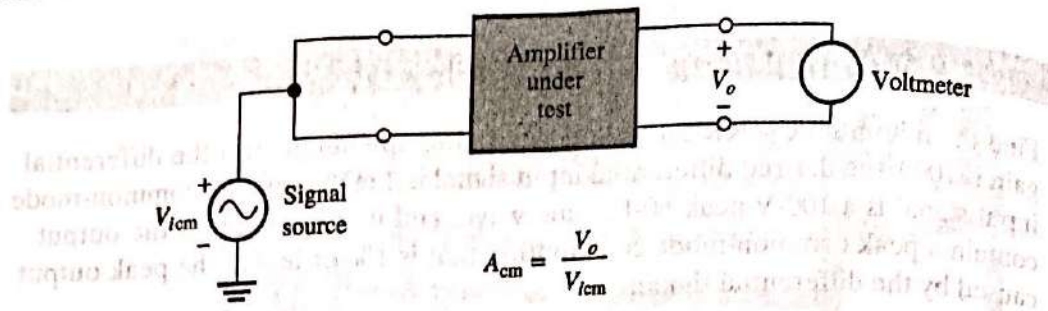


Figure 1.46 Setup for measurement of common-mode gain.

signal applied to both input terminals by the test source. Thus, we measure both the input voltage and output voltage, and then we compute their ratio to find the common-mode gain.

In theory, to apply a pure differential signal, we must provide two sources out of phase with each other at the amplifier input terminals, as shown in Figure 1.47a. However, since the common-mode gain is usually much smaller than the differential gain, only a small error results if a single source is used, as illustrated in Figure 1.47b. (In this figure, the input contains both a differential signal v_{id} and a common-mode signal $v_{icm} = v_{id}/2$.) In any case, the differential gain is found by taking the ratio of the output voltage to the input voltage when the common-mode voltage is zero or negligible. Finally, the CMRR is found by taking the ratio of the gains.

EXERCISE

1.14 A certain amplifier has a differential gain $A_d = 50,000$. If the input terminals are connected together and a 1-V signal is applied to them, an output signal of 0.1 V results. What is the common-mode gain of the amplifier and the CMRR, both expressed in dB?

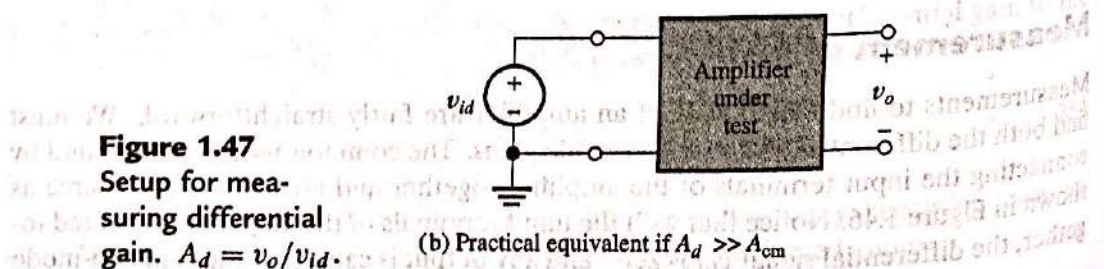
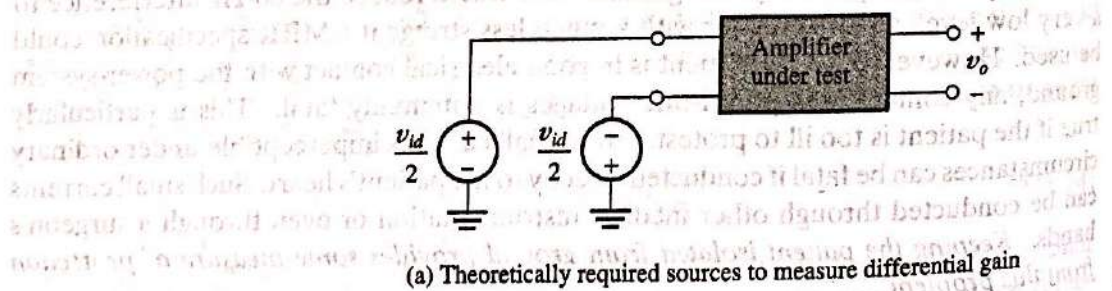


Figure 1.47
Setup for measuring differential gain. $A_d = v_o/v_{id}$.

Answer $A_{cm} = -20 \text{ dB}$ and $\text{CMRR} = 114 \text{ dB}$.

EXERCISE

1.15 A certain amplifier has $v_o = A_1 v_{i1} - A_2 v_{i2}$.

- Assume that $v_{i1} = 1/2$ and $v_{i2} = -1/2$. Find v_{id} and v_{icm} . Find v_o and A_d in terms of A_1 and A_2 .
- Assume that $v_{i1} = 1$ and $v_{i2} = 1$. Find v_{id} and v_{icm} . Find v_o and A_{cm} in terms of A_1 and A_2 .
- Use the results of parts (a) and (b) to find an expression for the CMRR in terms of A_1 and A_2 . Evaluate the CMRR if $A_1 = 100$ and $A_2 = 101$.

Answer

- $v_{id} = 1$, $v_{icm} = 0$, $v_o = A_d = (1/2)A_1 + (1/2)A_2$.
- $v_{id} = 0$, $v_{icm} = 1$, $v_o = A_{cm} = A_1 - A_2$.
- $\text{CMRR} = 20 \log \left| \frac{A_1 + A_2}{2(A_1 - A_2)} \right| = 40.0 \text{ dB}$.

SUMMARY

- Electronic systems are composed of functional blocks, which can be categorized as amplifiers, filters, signal sources, wave-shaping circuits, digital logic functions, digital memories, power supplies, and converters.
- Electronic systems can be classified as information-processing systems or as power-control systems.
- Analog signals can be converted to digital form. First, the signal is sampled at a rate greater than twice its highest frequency. Then each sample is represented approximately as a digital word. Because digital words of finite length cannot precisely represent all amplitudes, quantization error occurs in analog-to-digital conversion.
- Digital systems have several advantages compared to analog systems. First, it is possible to totally remove noise and degradation from a digital signal, provided that the digital levels can still be discerned. Thus, a digital signal can be regenerated at various points as it travels through a system. By contrast, noise and distortion tend to be cumulative for analog signals. Another advantage of digital systems is that they lend themselves to a higher degree of integration than analog systems. Also, they are more readily adaptable to a variety of tasks than analog systems are.

- Flowcharts illustrating the design of electronic systems and circuits are shown in Figure 1.6 on page 9 and in Figure 1.7 on page 10, respectively.
- Some important groups of electronics professionals are systems engineers, circuit designers, process engineers, and basic researchers. This book is concerned mainly with circuit design.
- The components of multiple integrated circuits and their interconnections are manufactured concurrently on a semiconductor wafer by a sequence of photolithographic processing steps. The components of a discrete circuit are manufactured separately and then interconnected, usually on a circuit board. To attain complex systems with high performance, small size, and reasonable cost, we strive to implement them in highly integrated form. We avoid discrete components wherever possible.
- Amplifiers can be modeled as voltage amplifiers, current amplifiers, transresistance amplifiers, or transconductance amplifiers.
- Ideal amplifiers of various types are characterized in Table 1.1 on page 39.
- When a load is connected to an amplifier, the output voltage or current of the amplifier may become smaller due to the output impedance of the amplifier. Similarly, when an amplifier is connected to a source, the current or voltage appearing at the amplifier input may be less than the internal source value, due to the output impedance of the source and the input impedance of the amplifier. We refer to these effects as “loading.”
- Two amplifiers are cascaded by connecting the input of the second to the output of the first. The overall voltage, current, or power gains are the product of the respective individual gains, taking loading of the first stage by the second into account.
- Power must be supplied to an amplifier from one or more dc sources. Part of this power is converted to output signal power and part is dissipated as heat. Amplifier power efficiency is the percentage of the dc input power that is converted to output signal power.
- All signals can be considered to be composed of sine waves of various amplitudes, frequencies, and phases. To amplify a signal without distortion, the amplifier must have constant gain for all of the frequencies contained in the signal.
- The rise time of the output of a broadband amplifier for a pulse input is related to the upper half-power frequency by

$$t_r \cong \frac{0.35}{B}$$
- A differential amplifier has two input terminals. Ideally, the output signal is a constant times the difference between the input signals.
- The common-mode-rejection ratio is the ratio of the gain for the differential input signal to the gain for the common-mode input signal.

PROBLEMS

Section 1.1: Electronic Systems

- 1.1. List five examples of electronic systems. Try to think of new examples that have not been mentioned in this chapter.
- 1.2. List five types of functional blocks found in electronic systems.
- 1.3. Discuss some of the distinctions between information-processing electronics and power electronics.
- 1.4. Explain how analog signals can be converted to digital form. Sketch an analog waveform and illustrate its digital equivalent using 4-bit code words.
- 1.5. List the relative advantages of digital systems compared to analog systems and vice versa.
- 1.6. An analog signal is to be converted to digital form as illustrated in Figure 1.3, except that 16-bit code words (instead of 3-bit code words) are used to represent each amplitude zone. The signal is sampled at 44.1 kHz. (These are the values for each channel of audio on a compact disc.) How many bits per second result? How many amplitude zones can be represented by 16-bit code words? Suppose that the highest amplitude represented is +5 V and the lowest is -5 V. Determine the width Δ (illustrated in Figure 1.3) of each quantization zone.
- 1.7. Consider analog-to-digital conversion of an electrocardiogram signal that has a highest frequency of $f_H = 100$ Hz. What minimum sampling frequency is required? Suppose that this signal has peak amplitudes of ± 5 mV and we want to convert it to digital form with quantization zones of width $\Delta = 0.01$ mV or less. What is the smallest number N of quantization zones needed? What is the smallest number k of bits per code word? Assuming that the minimum sampling frequency is used, what number of bits per second results?

Section 1.2: The Design Process

- 1.8. List the steps in the design of an electronic system.
- D1.9. **Voltage-divider design**¹. Suppose that we need to supply 5 ± 1 V to a computer that draws a variable current ranging from 0 to 300 mA. A constant 14-V source is available. Design a circuit composed of resistors to supply the required voltage to the computer. Assume that resistors having any nominal value needed are available, but that the resistors have tolerances of $\pm 5\%$. (Later in the book, we will learn how to improve this design using electronic components.) Use a resistive voltage divider.

¹ D denotes design problems.

Section 1.3: Integrated Circuits

- 1.10. List the four important groups of professionals involved in electronics, and briefly describe the activities of each group.
- 1.11. Compare an integrated circuit with a discrete circuit. What is the chief advantage of implementing complex systems in highly integrated form?
- 1.12. Suppose that each MOS transistor occupies a 10-micron (μm) square region on the surface of a silicon chip. How many MOS transistors can be placed on a square chip measuring 2 cm by 2 cm?

Section 1.4: Basic Amplifier Concepts

- 1.13. How is an inverting amplifier different from a noninverting amplifier?
- 1.14. What are "loading effects" in an amplifier circuit?
- 1.15. A signal source with an open-circuit voltage of $V_s = 2$ mV rms and an internal resistance of 50 k Ω is connected to the input terminals of an amplifier having an open-circuit voltage gain of 100, an input resistance of 100 k Ω and an output resistance of 4 Ω . A 4 - Ω load is connected to the output terminals. Find the voltage gains $A_{vs} = V_o/V_s$ and $A_v = V_o/V_i$. Also, find the power gain and current gain.
- 1.16. A certain amplifier has an open-circuit voltage gain of unity, an input resistance of 1 M Ω , and an output resistance of 100 Ω . The signal source has an internal voltage of 5 V and an internal resistance of 100 k Ω . The load resistance is 50 Ω . If the signal source is connected to the amplifier input terminals and the load is connected to the output terminals, find the voltage across the load and the power delivered to the load. Next, consider connecting the load directly across the signal source without the amplifier, and again find the load voltage and power. Compare the results. What do you conclude about the usefulness of a unity-gain amplifier in delivering signal power to a load?
- 1.17. An FM radio receiver has an input resistance of 75 Ω . The input signal provided by a distant transmitter is 5 μV rms, and the receiver supplies 5 V rms to an 8 - Ω loudspeaker. Calculate the power gain of the receiver.
- 1.18. An amplifier has an open-circuit voltage gain of 100. With a 10 -k Ω load connected, the voltage gain is found to be only 90. Find the output resistance of the amplifier.
- 1.19. The output voltage v_o of the circuit of Figure P1.19 is 100 mV with the switch closed. With the switch open, the output voltage is 50 mV. Find the input resistance of the amplifier.

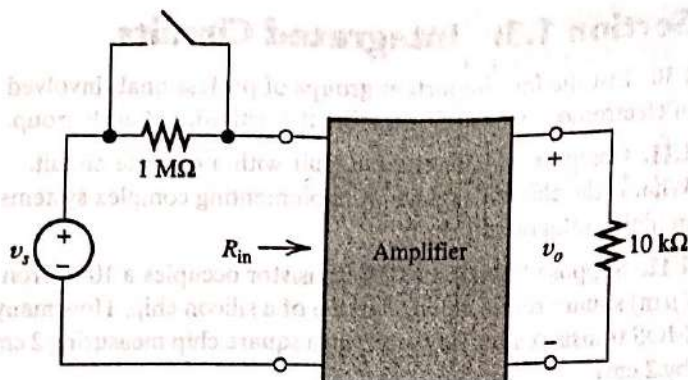


Figure P1.19

Section 1.5: Cascaded Amplifiers

1.20. Draw the cascade connection of two amplifiers. What is the open-circuit voltage gain of the cascade connection in terms of the voltage gains of the individual amplifiers?

1.21. Two amplifiers have the characteristics shown in Table P1.21. If the amplifiers are cascaded in the order A–B, find the input impedance, output impedance, and open-circuit voltage gain of the cascade. Repeat if the order is B–A.

Table P1.21 Amplifier Characteristics for Problem 1.21.

Amplifier	Open-Circuit Voltage Gain	Input Resistance	Output Resistance
A	100	3 kΩ	400 Ω
B	500	1 MΩ	20 Ω

1.22. Consider cascading amplifiers with an ideal transformer between them as shown in Figure P1.22. Find the turns ratio n of the transformer that maximizes the magnitude of the open-circuit voltage gain of the cascade. Find the answer in terms of R_{oA} and R_{iB} .

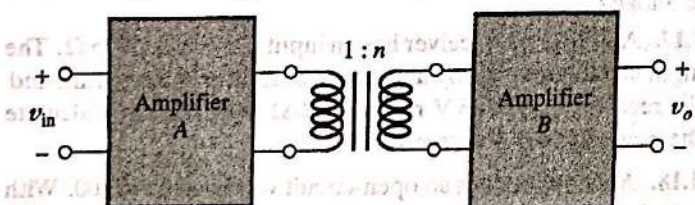


Figure P1.22

D1.23. Cascaded amplifier design. Suppose that you have available a number of amplifier stages with $R_i = 1 \text{ k}\Omega$, $A_{vo} = 10$, and $R_o = 100 \Omega$. The signal source has an open-circuit voltage of 20 mV rms and a short-circuit current of 1 μA rms. You need to supply an amplified signal of at least 10 V rms to a 100-Ω load. Design a cascaded amplifier using the fewest

number of stages. How many stages are required, and what is the resulting output voltage?

1. Determine the voltage gain $A_{vs} = v_o/v_s$ required.
2. Determine the internal impedance of the source.
3. Assume that n -stages are required, and find an expression for A_{vs} , taking loading effects into account.
4. Use trial and error to determine n .

D1.24. Cascaded amplifier design. Amplifier stages having the characteristics shown in Table P1.24 are available. The signal source has an open-circuit voltage of 20 mV rms and an internal resistance of 2 MΩ. The load is a 20-Ω resistance. Design a cascaded amplifier using the smallest number of stages that provides at least 1 W to the load. What are the values of the input resistance, the output resistance, and the open-circuit voltage gain of your amplifier?

1. Select the input stage based on the input resistance required.
2. Select the output stage based on the output resistance required.
3. Add stages between the input stage and the output stage as needed to attain the gain required.

Table P1.24 Amplifier characteristics for Problem D1.24.

Amplifier Stage Type	Open-Circuit Voltage Gain	Input Resistance	Output Resistance
A	1	10 MΩ	4 kΩ
B	5	1 kΩ	1 Ω
C	10	20 kΩ	100 Ω

D1.25. Cascaded amplifier design. Repeat Problem D1.24 if the source resistance is changed to 100 Ω.

Section 1.6: Power Supplies and Efficiency

1.26. Define the efficiency of a power amplifier. What is dissipated power in an amplifier? What form does dissipated power take?

1.27. A certain amplifier has an input voltage of 100 mV rms and an input resistance of 100 kΩ. It produces an output of 10 V rms across an 8-Ω load resistance. The power supply has a voltage of 15 V and delivers an average current of 2 A. Find the power dissipated in the amplifier and the efficiency of the amplifier.

1.28. Find the net power delivered to the amplifier by the three dc supply voltages shown in Figure P1.28.

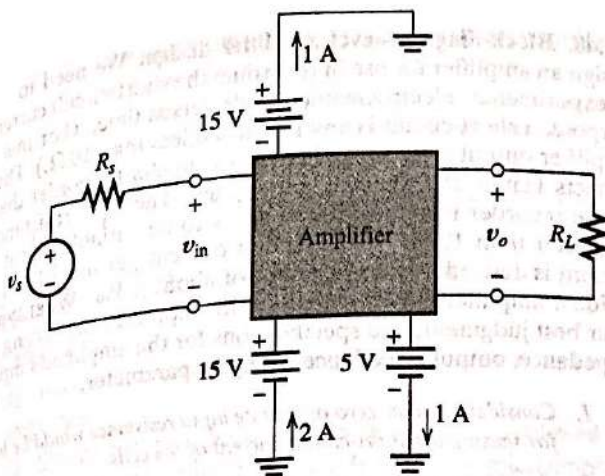


Figure P1.28

1.29. A certain power amplifier supplies a 20-V peak 100-Hz sine wave to an $8\text{-}\Omega$ load resistance, as illustrated in Figure P1.29. The currents supplied by the power supplies are half-cycle sinusoid pulses, as shown in the figure. Find the average current for each supply, the average power supplied by each source, and the efficiency of the amplifier.

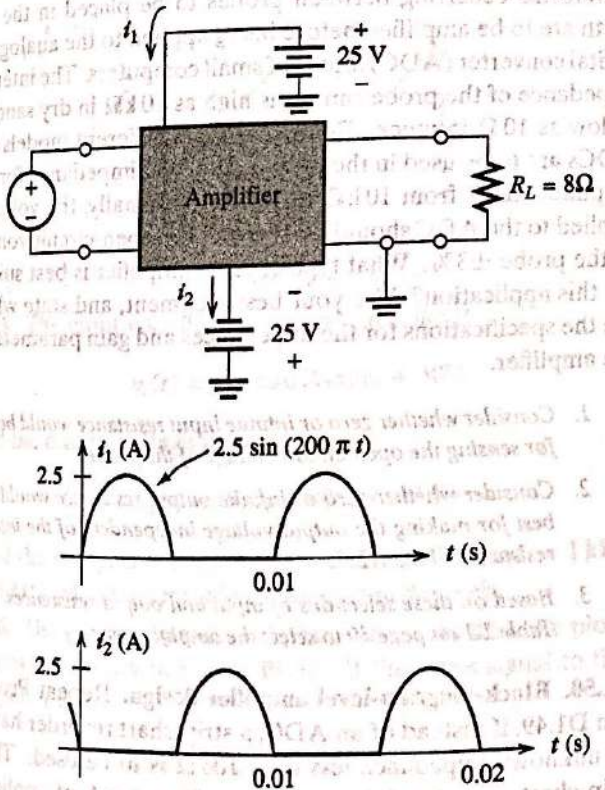


Figure P1.29

Section 1.7: Decibel Notation

- 1.30. How is power gain converted to decibels? How is voltage gain converted?
- 1.31. An amplifier has an input voltage of 10 mV rms and an output voltage of 5 V rms across a $10\text{-}\Omega$ load. The input current is $1\text{ }\mu\text{A rms}$. Assume that the input and output impedances are purely resistive. Find the input resistance. Find the voltage gain, current gain, and power gain as ratios and in decibels.
- 1.32. An amplifier operating with a load resistance of $8\text{ }\Omega$ has a voltage gain of unity and an input resistance of $100\text{ k}\Omega$. Determine the current gain and power gain in decibels.
- 1.33. An amplifier has a voltage gain of 30 dB and a current gain of 70 dB . What is the power gain in decibels? If the input resistance is $100\text{ k}\Omega$, what is the load resistance?
- 1.34. Find the voltages across a $50\text{-}\Omega$ resistance corresponding to (a) 10 dBV , (b) -30 dBV , (c) 10 dBmV , and (d) 20 dBW .
- 1.35. Find the power levels in watts corresponding to (a) 20 dBm , (b) -60 dBW , and (c) 10 dBW .

Section 1.8: Amplifier Models

- 1.36. Draw the voltage-amplifier model. Is the gain parameter measured under open-circuit or short-circuit conditions? Repeat for a current-amplifier model, a transresistance-amplifier model, and a transconductance-amplifier model.
- 1.37. An amplifier has an input resistance of $20\text{ }\Omega$, an output resistance of $10\text{ }\Omega$, and a short-circuit current gain of 3000 . The signal source has an internal voltage of 100 mV rms and an internal impedance of $200\text{ }\Omega$. The amplifier load is a $5\text{-}\Omega$ resistance. Find the current gain, voltage gain, and power gain of the amplifier. If the power supply has a voltage of 12 V and supplies an average current of 2 A , find the power dissipated in the amplifier.
- 1.38. An amplifier has an input resistance of $100\text{ }\Omega$, an output resistance of $10\text{ }\Omega$, and a short-circuit current gain of 500 . Draw the voltage-amplifier model for the amplifier, including numerical values for all parameters. Repeat for the transresistance and transconductance models.
- 1.39. An amplifier has a short-circuit current gain of 10 . When the amplifier is operated with a $50\text{-}\Omega$ load, the current gain is 8 . Find the output resistance of the amplifier.
- 1.40. Amplifier A has an input resistance of $1\text{ M}\Omega$, an output resistance of $200\text{ }\Omega$, and an open-circuit transresistance gain of $100\text{ M}\Omega$. Amplifier B has an input resistance of $50\text{ }\Omega$, an output impedance of $500\text{ k}\Omega$, and a short-circuit current gain of 100 . Find the voltage-amplifier model for the cascade of A followed by B. Find the corresponding transconductance-amplifier model.
- 1.41. Repeat Problem 1.40 if the order of the cascade is changed to B-A.

Section 1.9: Ideal Amplifiers

1.42. Give the input and output impedances for an ideal voltage amplifier. Repeat for each of the other ideal amplifier types.

1.43. An ideal transconductance amplifier having a short-circuit transconductance gain of 0.1 S is connected as shown in Figure P1.43. Find the resistance $R_x = v_x/i_x$ seen from the input terminals.

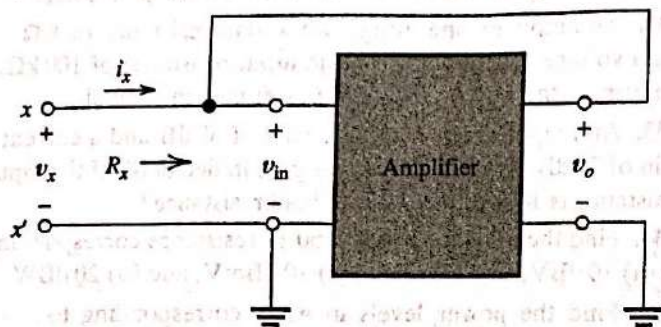


Figure P1.43

1.44. Repeat Problem 1.43 if the amplifier has an input resistance of $1000\ \Omega$, an output impedance of $20\ \Omega$, and an open-circuit transresistance gain of $10\text{ k}\Omega$.

1.45. An amplifier has an input resistance of $1\ \Omega$, an output resistance of $1\ \Omega$, and an open-circuit voltage gain of 10 . Classify this amplifier as an approximate ideal type and find the corresponding gain parameter. In deciding on an amplifier classification, assume that the source and load impedances are on the order of $1\text{ k}\Omega$.

1.46. Repeat problem 1.45 if the input impedance is $1\text{ M}\Omega$, the output impedance is $1\text{ M}\Omega$, and the open-circuit voltage gain is 100 .

D1.47. Block-diagram-level amplifier design. In a certain application, an amplifier is needed to sense the open-circuit voltage of a source and force current to flow through a load. The source resistance and load resistance are variable. The current delivered to the load is to be nearly independent of both the source resistance and load resistance. What type of ideal amplifier is needed? If the source resistance varies from $1\text{ k}\Omega$ to $2\text{ k}\Omega$ and this causes a 1% decrease in load current, what is the value of the input resistance? If the load resistance varies from $100\ \Omega$ to $300\ \Omega$ and this causes a 1% decrease in load current, what is the value of the output resistance?

1. Consider whether zero or infinite input resistance would be best for sensing the open-circuit voltage of the source.
2. Consider whether zero or infinite output resistance would be best for making the load current independent of the load resistance.
3. Based on these selections of input and output resistances, use Table 1.1 on page 39 to select the amplifier type.

D1.48. Block-diagram-level amplifier design. We need to design an amplifier for use in recording the short-circuit current of experimental electrochemical cells versus time. (For this purpose, a short circuit is any resistance less than $10\ \Omega$.) The amplifier output is to be applied to a strip-chart recorder that deflects $1\text{ cm} \pm 1\%$ for each volt applied. The input resistance of the recorder is unknown and likely to be variable, but it is greater than $10\text{ k}\Omega$. A deflection of 1 cm per mA of cell current is desired with an accuracy of about $\pm 3\%$. What type of ideal amplifier is best suited for this application? Using your best judgment, find specifications for the amplifier's input impedance, output impedance, and gain parameter.

1. Consider whether zero or infinite input resistance would be best for sensing the short-circuit current of the cells.
2. Consider whether zero or infinite output resistance would be best for making the output voltage independent of the input resistance of the chart recorder.
3. Based on these selections of input and output resistances, use Table 1.1 on page 39 to select the amplifier type.

D1.49. Block-diagram-level amplifier design. An amplifier is needed for the documentation of voltages in the earth created by a Navy extremely low frequency (ELF) antenna in northern Michigan (used for communication with submarines). Voltage waveforms occurring between probes to be placed in the earth are to be amplified before being applied to the analog-to-digital converter (ADC) inputs of small computers. The internal impedance of the probe can be as high as $10\text{ k}\Omega$ in dry sand or as low as $10\ \Omega$ in muck. Because several different models of ADCs are to be used in the project, the load impedance for the amplifier varies from $10\text{ k}\Omega$ to $1\text{ M}\Omega$. Nominally, the voltage applied to the ADC should be 10 times the open-circuit voltage of the probe $\pm 3\%$. What type of ideal amplifier is best suited for this application? Use your best judgment, and state what are the specifications for the impedances and gain parameter of the amplifier.

1. Consider whether zero or infinite input resistance would be best for sensing the open-circuit voltage of the probes.
2. Consider whether zero or infinite output resistance would be best for making the output voltage independent of the input resistance of the ADC.
3. Based on these selections of input and output resistances, use Table 1.1 on page 39 to select the amplifier type.

D1.50. Block-diagram-level amplifier design. Repeat Problem D1.49, if instead of an ADC, a strip-chart recorder having an unknown impedance less than $100\ \Omega$ is to be used. The strip-chart recorder deflects $1\text{ cm} \pm 1\%$ per mA of applied current. It is desired that the amplifier be designed so that the recorder deflects 1 cm for each 0.1 V of probe voltage.

1. Consider whether zero or infinite input resistance would be best for sensing the open-circuit voltage of the probes.
2. Consider whether zero or infinite output resistance would be best for making the output current independent of the input resistance of the strip-chart recorder.
3. Based on these selections of input and output resistances, use Table 1.1 on page 39 to select the amplifier type.

Section 1.10: Amplifier Frequency Response

1.51. Briefly discuss what the spectrum of a signal is and why it is important.

1.52. Sketch the gain magnitude of a typical dc-coupled amplifier against frequency. Repeat for an ac-coupled amplifier.

1.53. How is a wideband amplifier different from a narrowband amplifier?

1.54. The triangular waveform shown in Figure P1.54 has the Fourier series

$$v_i(t) = \frac{1}{2} - \frac{1}{\pi} \sin(2000\pi t) - \frac{1}{2\pi} \sin(4000\pi t) - \frac{1}{3\pi} \sin(6000\pi t) - \dots$$

Using a computer program of your choice, plot the sum of the first 5 terms of this series. Repeat for the first 25 terms.

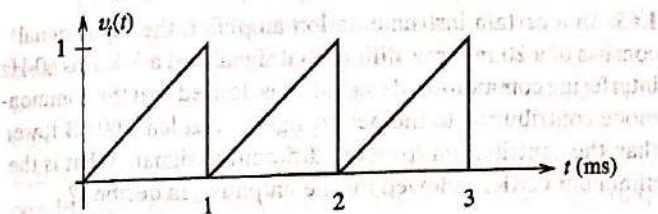


Figure P1.54

1.55. The input voltage to a certain amplifier is

$$v_i(t) = 0.1 \cos(2000\pi t + 30^\circ)$$

and the output voltage is

$$v_o(t) = 10 \sin(2000\pi t + 15^\circ)$$

Find the complex voltage gain of the amplifier at $f = 1$ kHz, and express the magnitude of the gain in decibels.

1.56. The gain magnitude and phase of an amplifier are plotted against frequency in Figure P1.56. If the input signal to the amplifier is

$$v_i(t) = 0.5 + \cos(200\pi t) + \cos(2000\pi t)$$

find an expression for the output signal as a function of time.

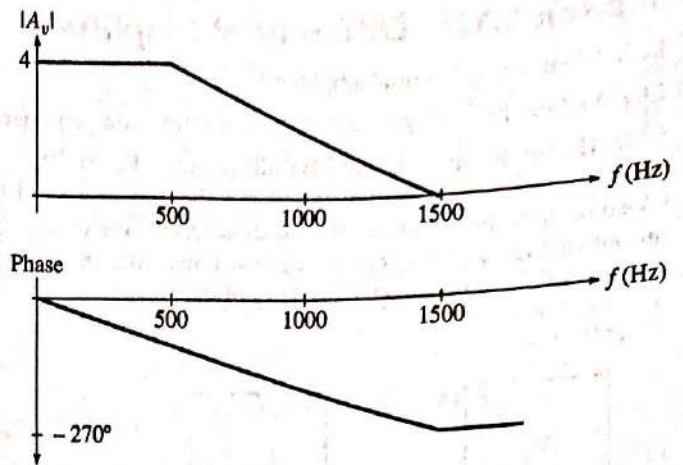


Figure P1.56

1.57. An ideal transconductance amplifier has a $0.01\text{-}\mu\text{F}$ load, as illustrated in Figure P1.57. Derive an expression for $A_v = V_o/V_s$. Evaluate your expression for $f = 1$ kHz, 10 kHz, and 100 kHz. Plot $|A_v|_{\text{dB}}$ to scale against frequency, using a logarithmic scale for the latter.

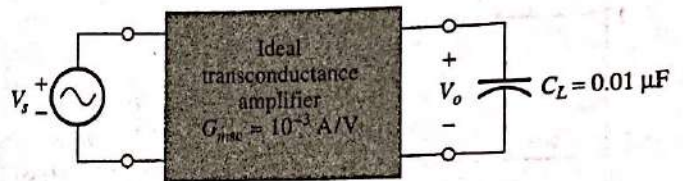


Figure P1.57

1.58. The model of an electret microphone and an amplifier is shown in Figure P1.58. The dc voltage of 2 V is present because a dc supply is required for the microphone to operate properly. The ac source V_s results from sound waves striking the microphone. The $0.1\text{-}\mu\text{F}$ coupling capacitor is needed to keep the dc voltage from being amplified. Derive an expression for the voltage gain $A_{vs} = V_o/V_s$ as a function of frequency. Evaluate for $f = 0$, 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz. Plot $|A_{vs}|_{\text{dB}}$ to scale against frequency, using a logarithmic scale for the latter.

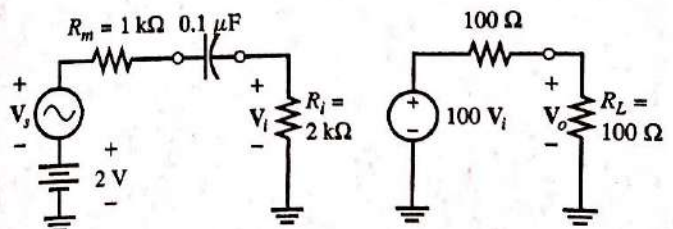


Figure P1.58

Section 1.11: Differential Amplifiers

1.59. What is a differential amplifier?

1.60. Define the common-mode rejection ratio of an amplifier.

1.61. The input signals v_{i1} and v_{i2} illustrated in Figure P1.61 are the inputs to a differential amplifier with a gain of $A_d = 10$. (Assume that the common-mode gain is zero.) Sketch the output of the amplifier to scale against time. Sketch the common-mode input signal to scale against time.

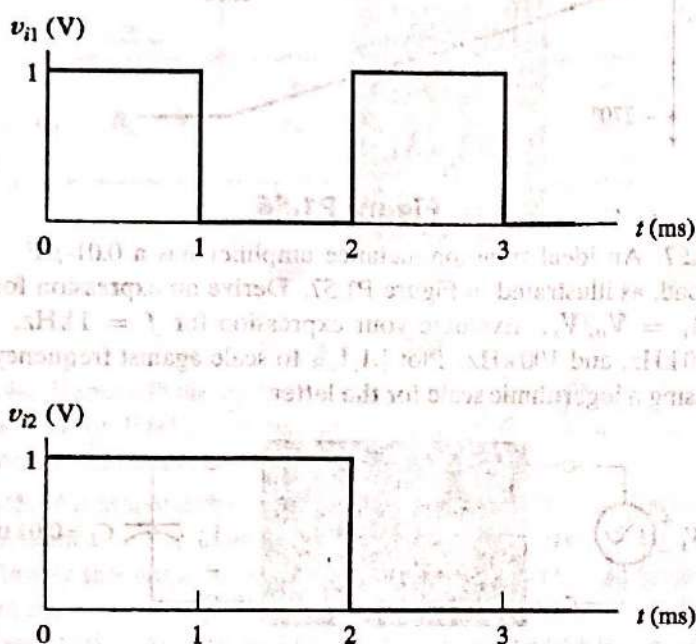


Figure P1.61

1.62. Figure P1.62 shows the equivalent circuit of a differential amplifier. (a) Derive expressions for the differential and common-mode voltage gains in terms of G_{m1} , G_{m2} , and R_L . (b) Evaluate the results for $G_{m1} = G_{m2} = 1$ mS and $R_L = 10$ k Ω . Also, determine the CMRR in dB. (c) Repeat part (b) for $G_{m1} = 1$ mS, $G_{m2} = 0.99$ mS, and $R_L = 10$ k Ω .

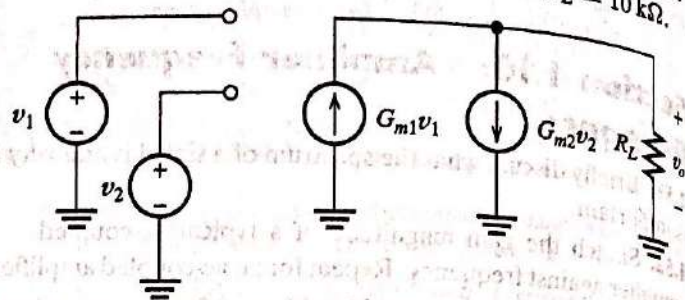


Figure P1.62

1.63. A differential amplifier has $v_o(t) = A_1 v_1(t) - A_2 v_2(t)$. If $A_1 = 1000$, and $A_2 = 999$, determine the CMRR of this amplifier.

1.64. A certain amplifier has a differential gain of 500. If the two input terminals are tied together and a 10-mV rms input signal is applied, the output signal is 20 mV rms. Find the CMRR for this amplifier.

1.65. In a certain instrumentation amplifier, the input signal consists of a 20-mV-rms differential signal and a 5-V-rms 60-Hz interfering common-mode signal. It is desired that the common-mode contribution to the output signal be at least 60 dB lower than the contribution from the differential signal. What is the minimum CMRR allowed for the amplifier, in decibels?

Operational Amplifiers

In Chapter 1, we discussed the external characteristics of amplifiers in general. In this chapter, we introduce an important electronic building block known as the **operational amplifier**.

Currently, the term *operational amplifier*, or, less formally, *op amp*, refers to an integrated circuit that is employed in a wide variety of general-purpose applications. However, this type of amplifier originated in analog-computer circuits, in which it was used to perform such operations as integration or addition of signals—hence, the name *operational amplifier*.

We will see that op amps are most useful when part of the output signal is returned to the input through a **feedback network**. Then the signal flows in a closed loop from the input through the op amp to the output and then through the feedback network back to the input, and we say that the circuit is operating in **closed-loop** conditions. When feedback is not present, we say that the op amp is operating under **open-loop** conditions.

Integrated-circuit op amps can be combined with resistive feedback networks to form many types of amplifiers. Furthermore, the characteristics of these circuits can be made to depend on the circuit configuration and the resistance values, but only weakly on the op amp—which can have large unit-to-unit variations in some of its parameters.

2

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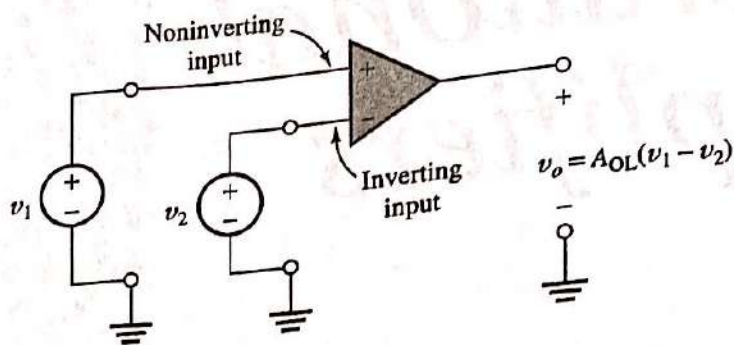


Figure 2.1 Circuit symbol for the op amp.

2.1 THE IDEAL OPERATIONAL AMPLIFIER

The circuit symbol for the operational amplifier is illustrated in Figure 2.1. The operational amplifier is a differential amplifier having both inverting and noninverting input terminals. (We discussed differential amplifiers in Section 1.11 starting on page 48.) The input signals are denoted as $v_1(t)$ and $v_2(t)$. (As usual, we use lowercase letters to represent general time-varying voltages. Often, we will omit the time dependence and refer to the voltages simply as v_1 , v_2 , and so on.)

Recall that the average of the input voltages is called the **common-mode signal** v_{icm} , given by

$$v_{icm} = \frac{1}{2}(v_1 + v_2)$$

Also, the difference between the input voltages, called the **differential signal**, is given by

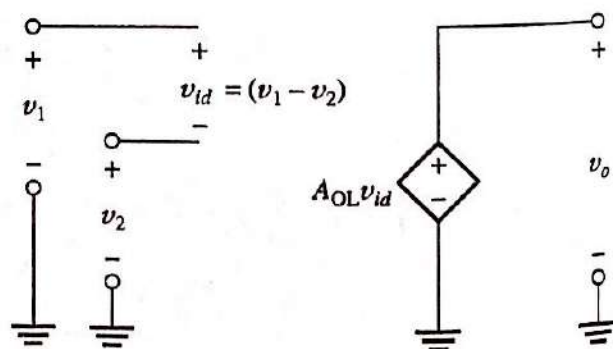
$$v_{id} = v_1 - v_2$$

An ideal operational amplifier has the following characteristics:

- Infinite input impedance.
- Infinite open-loop gain A_{OL} for the differential signal.
- Zero gain for the common-mode signal.
- Zero output impedance.
- Infinite bandwidth.

An equivalent circuit for the ideal operational amplifier consists simply of a controlled source, as illustrated in Figure 2.2. The **open-loop gain** A_{OL} is very large—ideally infinite.

Figure 2.2
Equivalent circuit
for the ideal op
amp. A_{OL} is very
large (approaching
infinity).



For now, we assume that the open-loop gain A_{OL} is constant versus frequency and the output voltage v_o has a waveshape identical to that of the differential input $v_{id} = v_1 - v_2$. (Later, we will see that A_{OL} is a function of frequency for real op amps.)

Power-Supply Connections

For a real op amp to function properly, one or more dc supply voltages must be applied, as shown in Figure 2.3. Often, however, we do not explicitly show the power-supply connections in circuit diagrams. (As indicated in the figure, it is standard practice to use uppercase symbols with repeated uppercase subscripts to represent dc power-supply voltages.)

2.2 THE SUMMING-POINT CONSTRAINT

Operational amplifiers are almost always used with **negative feedback**, in which part of the op-amp output signal is returned to the input in *opposition* to the source signal. (It is also possible to construct circuits with positive feedback, in which the signal returned to the input *aids* the original source signal. However, as we will see, negative feedback turns out to be more useful in amplifier circuits.) Later in the book, we discuss the important topic of negative feedback in more detail. In this chapter, an adequate analysis of op-amp circuits is achieved by assuming an ideal op amp and employing a concept known as the **summing-point constraint**.

For an ideal op amp, we assume that the open-loop gain A_{OL} approaches infinity, and then even a very tiny differential input voltage results in a very large output voltage. In a negative-feedback circuit, the feedback network returns a fraction of the output to the inverting input terminal, forcing the differential input voltage toward zero. Assuming infinite gain, the differential input voltage is driven to zero exactly. Because the differential input voltage of the op amp is zero, the input current is also zero. We refer to the fact that the differential input voltage and the input current are forced to zero as the **summing-point constraint**.

Ideal op-amp circuits are analyzed by the following steps:

1. Verify that negative feedback is present. Usually this takes the form of a resistor network connected to the output terminal and to the inverting input terminal.
2. Assume that the differential input voltage and the input current of the op amp are forced to zero. (This is the summing-point constraint.)
3. Apply standard circuit analysis principles, such as Kirchhoff's laws and Ohm's law, to solve for the quantities of interest.

We illustrate this type of analysis in the next several sections for some commonly used circuits.

2.3 THE INVERTING AMPLIFIER

An op-amp circuit known as the **inverting amplifier** is shown in Figure 2.4. We will determine the closed-loop voltage gain $A_v = v_o/v_{in}$ by assuming an ideal op amp and employing the summing-point constraint. However, before starting analysis of an op-amp circuit, we should always check to make sure that negative feedback is present, rather than positive feedback.

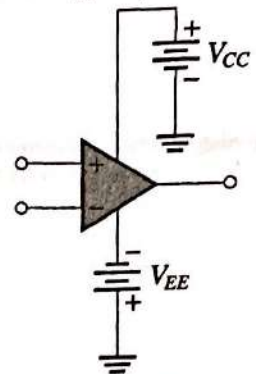


Figure 2.3 Op-amp symbol showing power supplies.

We refer to the fact that the differential input voltage and the input current are forced to zero as the **summing-point constraint**.

Steps for analysis of circuits containing ideal op amps.

The inverting amplifier is a very important op-amp circuit.

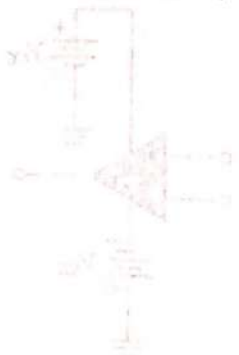


Figure 2.4
Inverting amplifier.

Step 1: Verify that negative feedback is present.

Step 2: Assume that the differential input voltage and the input current of the op amp are forced to zero.

Step 3: Apply standard circuit analysis principles, such as Kirchhoff's laws and Ohm's law, to solve for the quantities of interest.

In Figure 2.4, the feedback is negative, as we shall demonstrate. For example, suppose that due to the input source v_{in} , a positive voltage v_x appeared at the inverting input. Then a negative output voltage of large (theoretically, infinite) magnitude would result at the output. Part of this output voltage would be returned to the inverting input by the feedback path through R_2 . Thus, the initially positive voltage at the inverting input is driven toward zero by the feedback action. A similar chain of events occurs for the appearance of a negative voltage at the inverting input terminal. Hence, the output voltage of the op amp takes precisely the value needed to oppose the source and produce (nearly) zero voltage at the op-amp input.

Figure 2.5 shows the inverting amplifier, including the conditions of the summing-point constraint at the input of the op amp. Notice that the input voltage v_{in} appears across R_1 . Thus, the current through R_1 is

$$i_1 = \frac{v_{in}}{R_1} \quad (2.1)$$

Because the current flowing into the op-amp input terminals is zero, the current flowing through R_2 is

$$i_2 = i_1 \quad (2.2)$$

Thus, we have

$$i_2 = \frac{v_{in}}{R_1} \quad (2.3)$$

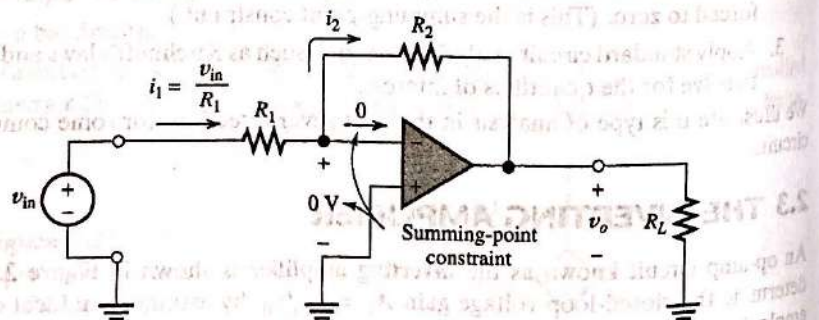


Figure 2.5 We make use of the summing-point constraint in the analysis of the inverting amplifier.

Writing a voltage equation around the loop that includes the output terminals, the resistor R_2 , and the op-amp input terminals, we obtain

$$v_o + R_2 i_2 = 0 \quad (2.4)$$

Key equation: Voltage gain of the op-amp inverter.

Using Equation (2.3) to substitute for i_2 in Equation (2.4) and solving for the closed-loop voltage gain, we have

$$A_v = \frac{v_o}{v_{in}} = -\frac{R_2}{R_1} \quad (2.5)$$

Thus, under the ideal op-amp assumption, the closed-loop voltage gain is determined solely by the ratio of the resistances. This is a very desirable situation, because resistances can have precise and stable values. Notice that the voltage gain is negative, indicating that the amplifier is inverting (i.e., the output voltage is out of phase with the input voltage).

The input impedance of the inverting amplifier is

$$Z_{in} = \frac{v_{in}}{i_1} = R_1 \quad (2.6)$$

The input impedance of the inverting amplifier equals R_1 .

Hence, we can control the input impedance of the circuit by our choice of R_1 .

Rearranging Equation (2.5), we have

$$v_o = -\left(\frac{R_2}{R_1}\right) v_{in} \quad (2.7)$$

We see that the output voltage is independent of the load resistance R_L . We conclude that the output acts as an ideal voltage source (as far as R_L is concerned). In other words, the output impedance of the inverting amplifier is zero.

...the output impedance of the inverting amplifier is zero.

Later, we will see that the characteristics of the inverting amplifier are influenced by nonideal properties of the op amp. Nevertheless, in many applications, the departure of actual performance from the ideal is insignificant. Of course, if the resistance values R_1 and R_2 are inaccurate, then the closed-loop gain will be inaccurate.

The Virtual-Short-Circuit Concept

Sometimes the condition at the op-amp input terminals of Figure 2.5 is called a **virtual short circuit**. This terminology is used because, even though the differential input voltage of the op amp is forced to zero (as if by a short circuit to ground), the op-amp input current is also zero. The terminology can be confusing, unless it is realized that it is the action at the output of the op amp acting through the feedback network that forces the differential input voltage to zero. (Possibly it would be just as valid to call the condition at the op-amp input terminals a "virtual open circuit," because no current flows.)

Variations of the Inverter Circuit

Several useful versions of the inverter circuit exist. Analysis of these circuits follows the pattern that we have used for the basic inverter: Verify that *negative feedback* is present, assume the summing-point constraint, and then apply basic circuit laws.

Example 2.1 Analysis of an Inverting Amplifier

Figure 2.6 illustrates a version of the inverting amplifier that can have high gain magnitude without resorting to as wide a range of resistance values as needed in the standard inverter configuration. Derive an expression for the closed-loop voltage gain under the ideal op-amp assumption. Also, find the input impedance and output impedance. Evaluate the results for $R_1 = R_3 = 1 \text{ k}\Omega$ and $R_2 = R_4 = 10 \text{ k}\Omega$. Then consider the standard inverter configuration of Figure 2.5 with $R_1 = 1 \text{ k}\Omega$, and find the value of R_2 required to achieve the same gain.

SOLUTION First, we verify that negative feedback is present. Assume a positive value for v_i . This results in a negative output voltage of very large magnitude. Part of the negative voltage is returned through the resistor network and opposes the original input voltage. Thus, we conclude that negative feedback is present.

Next, we assume the summing-point-constraint conditions:

$$v_i = 0$$

$$i_i = 0$$

Then we apply Kirchhoff's current law, Kirchhoff's voltage law, and Ohm's law to analyze the circuit. To begin, we notice that v_{in} appears across R_1 (because $v_i = 0$). Thus, we can write

$$i_1 = \frac{v_{in}}{R_1} \quad (2.8)$$

Next, we apply Kirchhoff's current law to the node at the right-hand end of R_1 to obtain

$$i_1 = i_2 \quad (2.9)$$

(Here we have used the fact that $i_i = 0$.)

Writing a voltage equation across the op-amp input terminals, R_2 , and R_3 , we find that

$$R_2 i_2 = R_3 i_3 \quad (2.10)$$

Applying Kirchhoff's current law at the top end of R_3 yields

$$i_4 = i_2 + i_3 \quad (2.11)$$

Writing a voltage equation for the loop containing v_o , R_4 , and R_3 gives

$$v_o = -R_4 i_4 - R_3 i_3 \quad (2.12)$$

Next, we use substitution to eliminate the current variables (i_1 , i_2 , i_3 , and i_4) and obtain an equation relating the output voltage to the input voltage. Equating the right-hand sides of Equations (2.8) and (2.9), we obtain

$$i_2 = \frac{v_{in}}{R_1} \quad (2.13)$$

Step 1: Verify that negative feedback is present.

Step 2: Assume the summing-point constraint.

Step 3: Apply basic circuit laws.

Then we use Equation (2.13) to substitute for i_2 in Equation (2.10) and rearrange terms to get

$$i_3 = v_{in} \frac{R_2}{R_1 R_3} \quad (2.14)$$

Using Equations (2.13) and (2.14) to substitute for i_2 and i_3 in Equation (2.11) yields

$$i_4 = v_{in} \left(\frac{1}{R_1} + \frac{R_2}{R_1 R_3} \right) \quad (2.15)$$

Finally, using Equations (2.14) and (2.15) to substitute for i_3 and i_4 in Equation (2.12) gives

$$v_o = -v_{in} \left(\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_4 R_2}{R_1 R_3} \right) \quad (2.16)$$

Thus, the closed-loop voltage gain of the circuit is

$$A_v = \frac{v_o}{v_{in}} = - \left(\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_4 R_2}{R_1 R_3} \right) \quad (2.17)$$

The input resistance is obtained from Equation (2.8):

$$R_{in} = \frac{v_{in}}{i_1} = R_1$$

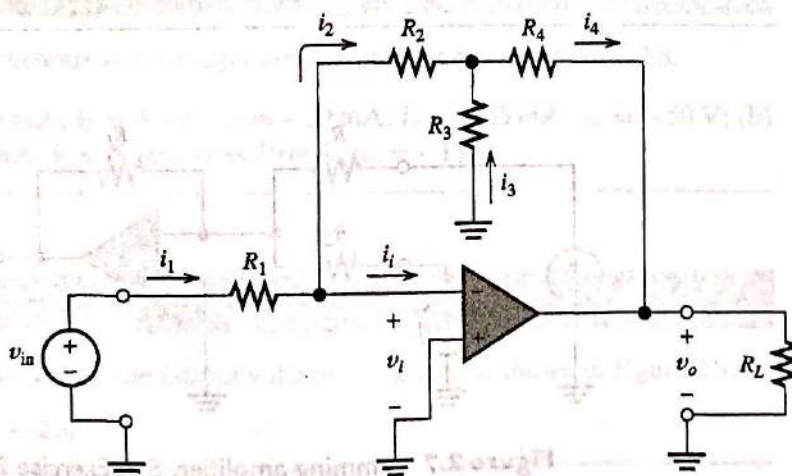
Inspection of Equation (2.16) shows that the output voltage is independent of the load resistance. Thus, the output appears as an ideal voltage source to the load. In other words, the output impedance of the amplifier is zero.

Evaluating the voltage gain for the resistance values given ($R_1 = R_3 = 1 \text{ k}\Omega$ and $R_2 = R_4 = 10 \text{ k}\Omega$) yields

$$A_v = -120$$

Figure 2.6

An inverting amplifier that achieves high gain with a smaller range of resistor values than required for the basic inverter.



The circuit of Figure 2.6 has the advantage of requiring a smaller range of resistances than the basic inverter, especially when high gain magnitude is desired.

In the basic inverter circuit of Figure 2.5, the voltage gain is given by

$$A_v = -\frac{R_2}{R_1}$$

Thus, to achieve a voltage gain of -120 , we would require $R_2 = 120 \text{ k}\Omega$. Notice that the sum of the resistances required for the basic inverter is $121 \text{ k}\Omega$, whereas the circuit of Figure 2.6 requires a total resistance of $22 \text{ k}\Omega$. In implementing these circuits in integrated form, the chip area consumed by the resistors is approximately proportional to the total resistance. Hence, for large gain magnitude, the circuit of Figure 2.6 is preferable to the basic inverter illustrated in Figure 2.5 for implementation as an integrated circuit.

Now that we have demonstrated how to make use of the summing-point constraint in analyzing ideal-op-amp circuits having negative feedback, we provide some exercises for practice in applying the technique. Each of these circuits has negative feedback, and if we assume ideal op amps, the summing-point constraint applies.

EXERCISE

2.1 A circuit known as a **summing amplifier** is illustrated in Figure 2.7. (a) Use the ideal-op-amp assumption to solve for the output voltage in terms of the input voltages and resistor values. (b) What is the input resistance seen by v_A ? (c) By v_B ? (d) What is the output resistance seen by R_L ?

Answer

- (a) $v_o = -(R_f/R_A)v_A - (R_f/R_B)v_B$.
- (b) The input resistance for v_A is equal to R_A .
- (c) The input resistance for v_B is equal to R_B .
- (d) The output resistance is zero.

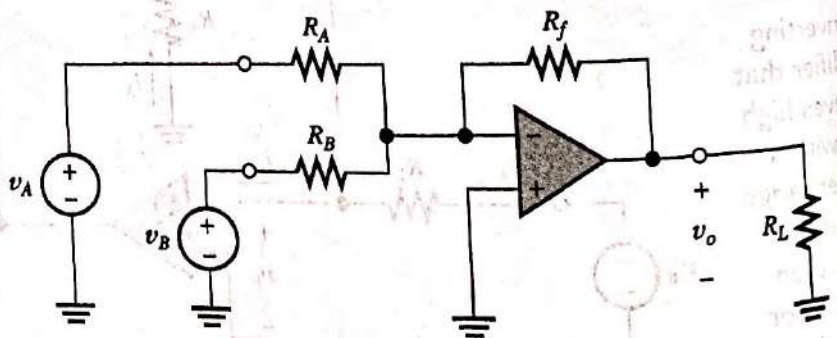


Figure 2.7 Summing amplifier. See Exercise 2.1.

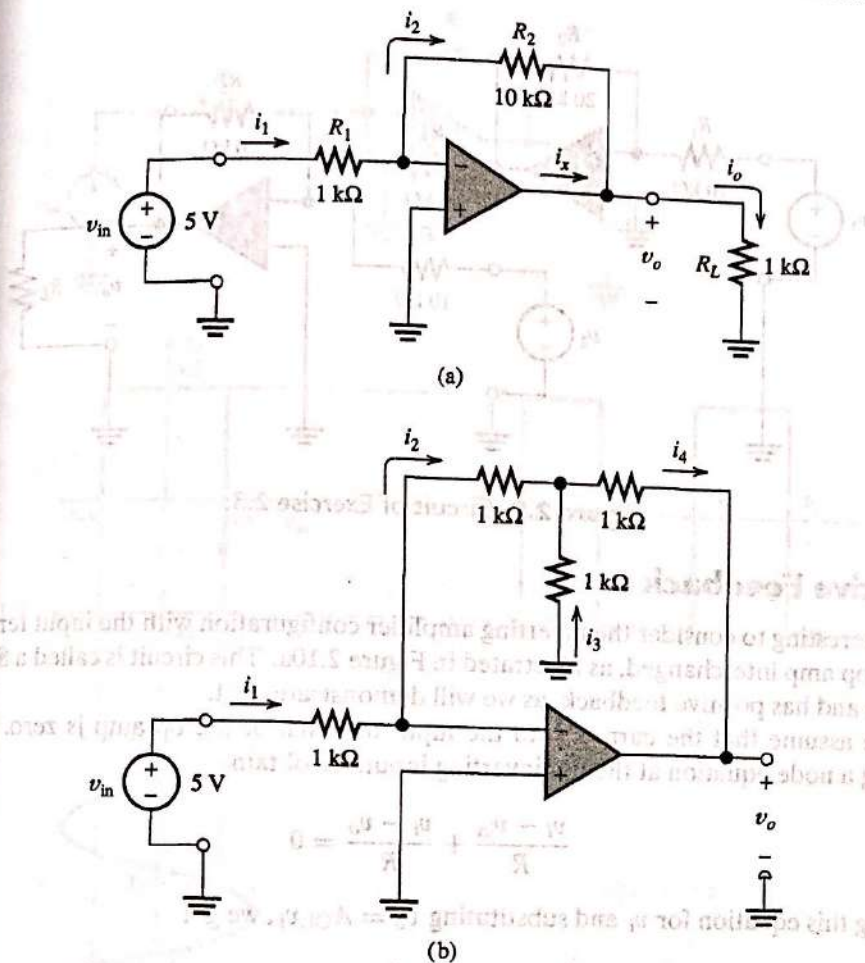


Figure 2.8 Circuits of Exercise 2.2.

EXERCISE

2.2 Solve for the currents and voltages labeled in the circuits of Figure 2.8.

Answer (a) $i_1 = 5 \text{ mA}$, $i_2 = 5 \text{ mA}$, $i_o = -50 \text{ mA}$, $i_x = -55 \text{ mA}$, $v_o = -50 \text{ V}$; (b) $i_1 = 5 \text{ mA}$, $i_2 = 5 \text{ mA}$, $i_3 = 5 \text{ mA}$, $i_4 = 10 \text{ mA}$, $v_o = -15 \text{ V}$.

EXERCISE

2.3 Find an expression for the output voltage of the circuit shown in Figure 2.9.

Answer $v_o = 4v_1 - 2v_2$.

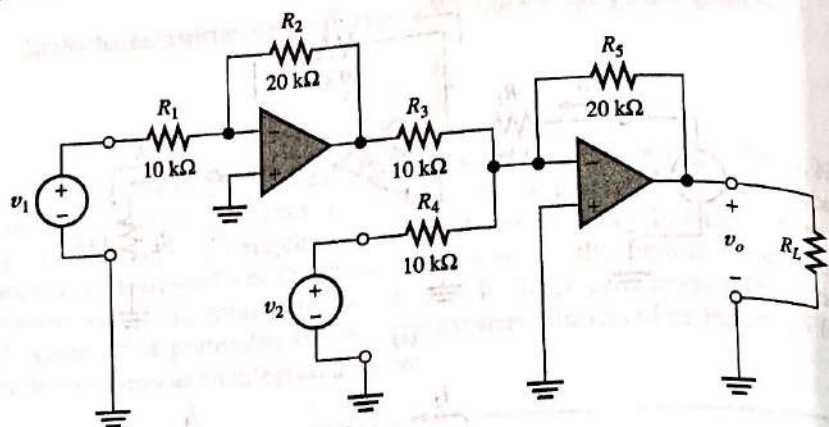


Figure 2.9 Circuit of Exercise 2.3.

Positive Feedback

It is interesting to consider the inverting amplifier configuration with the input terminals of the op amp interchanged, as illustrated in Figure 2.10a. This circuit is called a **Schmitt trigger** and has positive feedback, as we will demonstrate next.

We assume that the current into the input terminal of the op amp is zero. Then, writing a node equation at the noninverting input, we obtain

$$\frac{v_i - v_{in}}{R} + \frac{v_i - v_o}{R} = 0$$

Solving this equation for v_i and substituting $v_o = A_{OL}v_i$, we get

$$v_i = \frac{1}{2}(v_{in} + v_o) = \frac{1}{2}(v_{in} + A_{OL}v_i) \quad (2.18)$$

Notice that the amplified input voltage $v_o = A_{OL}v_i$ makes a positive contribution to the op-amp input voltage v_i , showing that the circuit has positive feedback.

Suppose that initially we have $v_{in} = 0$ and $v_o = 0$. Then in an ideal circuit, v_i would be zero. However, in real circuits, certain imperfections (such as input bias current or offset voltage, which we discuss in detail later in this chapter) cause v_i to assume a small value. Suppose that this v_i is positive; then a positive output voltage results. As shown by Equation (2.18), half of the output voltage is returned to the op-amp input by the feedback network. Thus, the input voltage v_i becomes larger, causing an even larger output voltage.

A real op amp cannot produce infinite output voltage; instead, the output voltage magnitude cannot exceed a particular value. Let us assume that the op amp shown in Figure 2.10a has extreme output voltages of ± 5 V. Thus, the circuit does not function as an amplifier—the output voltage becomes stuck either at $+5$ V or at -5 V, depending on the initial polarity of v_i .

Suppose that $v_o = +5$ V. Then, as long as we have $v_{in} > -5$ V, the input voltage v_i is greater than zero and v_o remains $+5$ V. This is apparent from Equation 2.18. However,

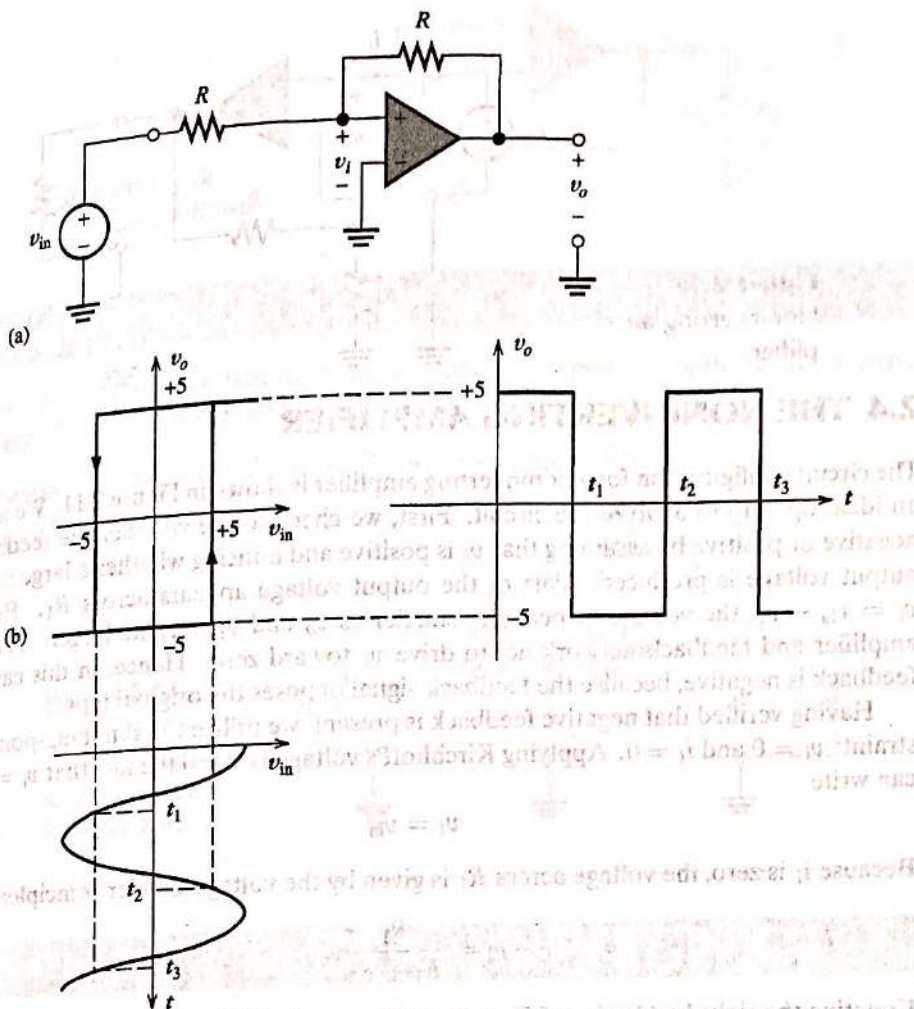


Figure 2.10 Schmitt trigger circuit and waveforms.

if v_{in} becomes less than -5 V , v_i becomes negative and the output voltage v_o quickly switches to -5 V . Then v_o will remain at -5 V until v_{in} exceeds $+5\text{ V}$. A plot of v_o versus v_{in} is illustrated in Figure 2.10b.

The figure also illustrates a sinusoidal input voltage and the resulting output voltage, which is a square wave. Of course, in an amplifier circuit, a sinusoidal input results in a sinusoidal output. Even though the Schmitt trigger circuit is not an amplifier, it is useful as a waveshaping circuit. We will consider variations of this circuit and other wave shapers later in the book.

If we were to ignore the fact that the circuit of Figure 2.10a has positive rather than negative feedback and were to apply the summing-point constraint erroneously, we would obtain $v_o = -v_{in}$, just as we did for the circuit with negative feedback. This illustrates the importance of verifying that negative feedback is present before using the summing-point constraint.

Positive feedback drives the output voltage to either extreme.

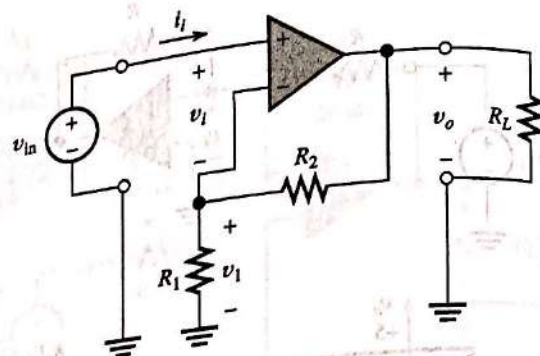


Figure 2.11
Noninverting amplifier.

2.4 THE NONINVERTING AMPLIFIER

Step 1: Verify that negative feedback is present.

Step 2: Assume the summing-point constraint.

Step 3: Apply basic circuit laws to analyze the circuit.

The circuit configuration for a noninverting amplifier is shown in Figure 2.11. We assume an ideal op amp to analyze the circuit. First, we check to see whether the feedback is negative or positive by assuming that v_i is positive and noticing whether a large positive output voltage is produced. Part of the output voltage appears across R_1 . Because $v_i = v_{in} - v_1$, the voltage v_i becomes smaller as v_o and v_1 become larger. Thus, the amplifier and feedback network act to drive v_i toward zero. Hence, in this case, the feedback is negative, because the feedback signal opposes the original input.

Having verified that negative feedback is present, we utilize the summing-point constraint: $v_i = 0$ and $i_i = 0$. Applying Kirchhoff's voltage law and the fact that $v_i = 0$, we can write

$$v_1 = v_{in} \quad (2.19)$$

Because i_i is zero, the voltage across R_1 is given by the voltage-divider principle:

$$v_1 = \frac{R_1}{R_1 + R_2} v_o \quad (2.20)$$

Equating the right-hand sides of Equations (2.20) and (2.19) and rearranging them, we find the closed-loop voltage gain:

$$A_v = \frac{v_o}{v_{in}} = 1 + \frac{R_2}{R_1} \quad (2.21)$$

Key equation: Voltage gain of the noninverting amplifier.

Notice that the circuit is a noninverting amplifier (A_v is positive), and the gain is set by the ratio of the feedback resistors.

... under the ideal-op-amp assumption, the noninverting amplifier is an ideal voltage amplifier.

The input impedance of the circuit is theoretically infinite because the input current is zero. Since the voltage gain is independent of the load resistance, the output voltage is independent of the load resistance. Thus, the output impedance is zero. Therefore, under the ideal-op-amp assumption, the noninverting amplifier is an ideal voltage amplifier. (Ideal amplifiers are discussed in Section 1.9.)

The Voltage Follower

Notice from Equation (2.21) that the minimum gain magnitude is unity, which is obtained with $R_2 = 0$. Usually, we choose R_1 to be an open circuit for unity gain. The resulting circuit is called a **voltage follower** and is illustrated in Figure 2.12.

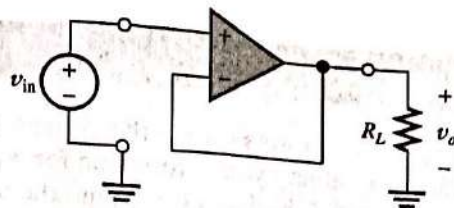


Figure 2.12
Voltage follower.

EXERCISE

2.4 Find the voltage gain $A_v = v_o/v_{in}$ and input impedance of the circuit shown in Figure 2.13 (a) with the switch open and (b) with the switch closed.

Answer (a) $A_v = +1$, $R_{in} = \infty$; (b) $A_v = -1$, $R_{in} = R/2$.

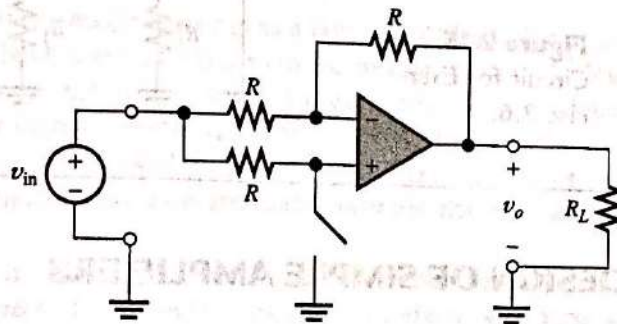


Figure 2.13
Inverting or noninverting amplifier. See Exercise 2.4.

The circuits shown on this page are important applications of op amps.

EXERCISE

2.5 Find an expression for the output voltage in terms of the resistances and input voltages for the differential amplifier shown in Figure 2.14.

Answer $v_o = (R_2/R_1)(v_2 - v_1)$.

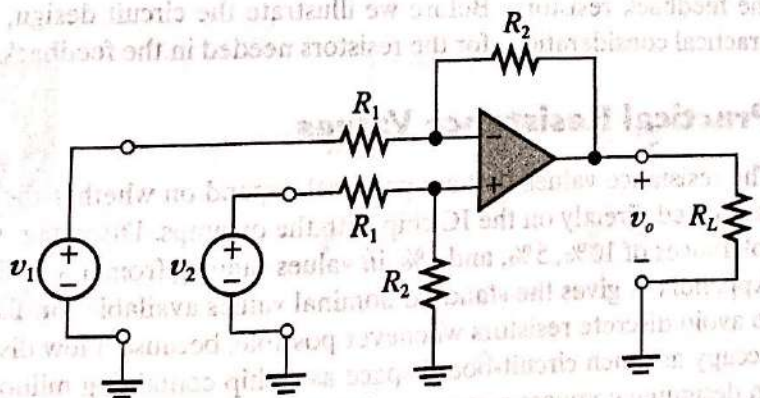


Figure 2.14
Differential amplifier. See Exercise 2.5.

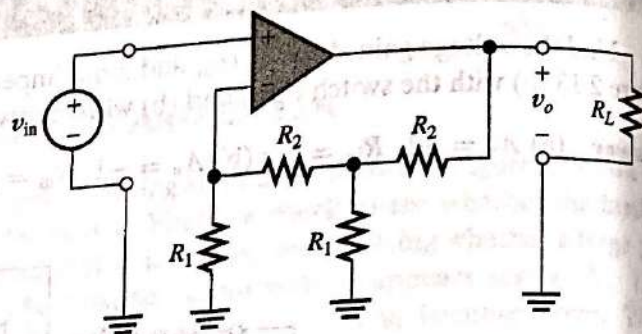
In designing compact systems with high functionality and reasonable cost, we must use the most efficient components as a first resort.

EXERCISE

2.6 (a) Derive an expression for the voltage gain v_o/v_{in} of the circuit shown in Figure 2.15. (b) Evaluate your expression for $R_1 = 1\text{ k}\Omega$ and $R_2 = 10\text{ k}\Omega$. (c) Find the input resistance of this circuit. (d) Find the output resistance.

Answer (a) $A_v = 1 + 3(R_2/R_1) + (R_2/R_1)^2$; (b) $A_v = 131$; (c) $R_{in} = \infty$; (d) $R_o = 0$.

Figure 2.15
Circuit for Exercise 2.6.



2.5 DESIGN OF SIMPLE AMPLIFIERS

Many useful amplifiers can be designed by using resistive feedback networks with op amps. For now, we assume ideal op amps; later in this chapter, we consider the effects of the nonideal properties of real op amps. Often in practice the performance requirements of the circuits to be designed are not extreme, and design can be carried out assuming ideal op amps. (Of course, we need to keep in mind that resistor tolerances lead to inaccuracies in the closed-loop gains.)

Later in this section, we illustrate a design by using the op-amp circuits that we have considered in the previous sections (including the exercises). For these circuits, the design mainly consists of selecting a suitable circuit configuration and the values for the feedback resistors. Before we illustrate the circuit design, we discuss some of the practical considerations for the resistors needed in the feedback network.

Practical Resistance Values

The resistance values that are practical depend on whether the resistors are discrete or fabricated directly on the IC chip with the op amps. Discrete resistors are available with tolerances of 10%, 5%, and 1%, in values ranging from a few ohms to tens of megohms. Appendix A gives the standard nominal values available for discrete resistors. We want to avoid discrete resistors whenever possible, because a few discrete resistors can easily occupy as much circuit-board space as a chip containing millions of integrated devices. In designing compact systems with high functionality and reasonable cost, we resort to discrete components only as a last resort.

In designing compact systems with high functionality and reasonable cost, we resort to discrete components only as a last resort.

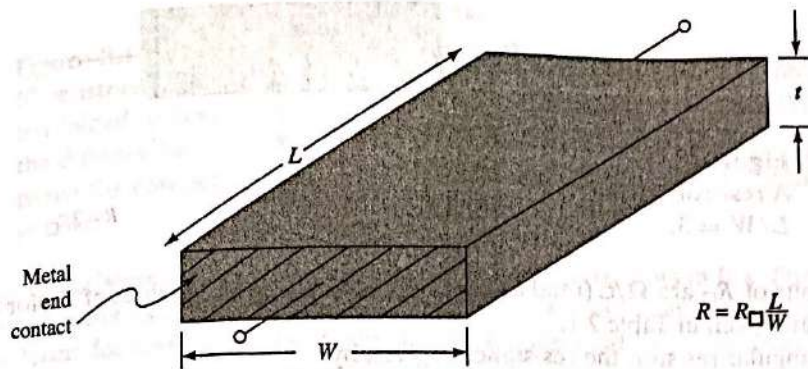


Figure 2.16 IC resistors are fabricated from a layer of conductive material.

One way to fabricate an integrated resistor is as a layer of conducting material with metal contacts at the ends. Such a resistor is illustrated in Figure 2.16. Typically, the thickness t and conductivity of the materials used to fabricate resistors are predetermined by the requirements of other devices on the chip. We can vary the length L , vary the width W , and select from the several available materials in designing a resistor. Virtually any nominal value (within practical limits) is attainable because the ratio L/W can be adjusted as needed.

An important parameter in the design of an integrated-circuit resistor is the **sheet resistance** $R_{\square}$ of the layer used to fabricate the resistor. The sheet resistance of a film layer is the resistance of a square resistor (i.e., $L = W$) constructed from the film. It turns out that the resistance of a square resistor does not depend on the side length of the square, provided that the thickness and conductivity of the material are fixed and that contact is made along the entire length of the opposing sides of the resistor. As an illustration, consider the square resistor shown in Figure 2.17, which can be divided into four smaller squares. Suppose that the resistance of each of the smaller squares is $R_{\square}$. The smaller squares can be considered to be connected in series and parallel, as shown in the figure. Thus, the resistance of the larger square is also equal to $R_{\square}$.

...the resistance of a square resistor does not depend on the side length of the square...

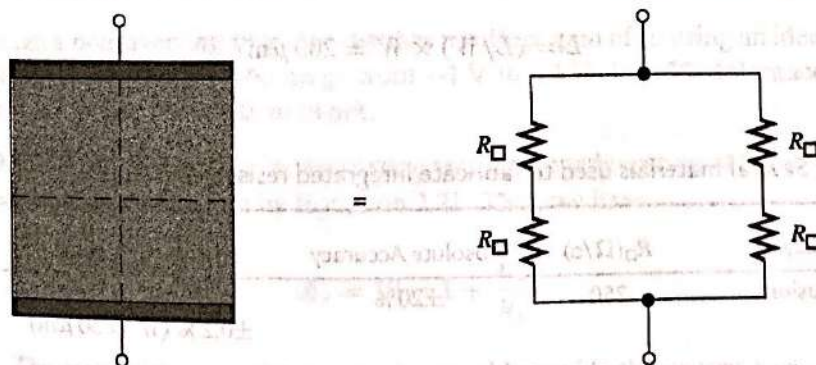


Figure 2.17 The resistance of the larger square is the same as the resistance of each of the smaller squares.

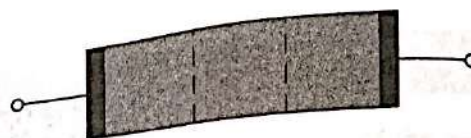


Figure 2.18
A resistor having
 $L/W = 3$.

$$\frac{L}{W} = 3$$

$$R = 3R_{\square}$$

The units of $R_{\square}$ are $\Omega/\square$ (read as ohms per square). Typical values of $R_{\square}$ for various IC layers are given in Table 2.1.
For a rectangular resistor, the resistance is given by

$$R = R_{\square} \frac{L}{W} \quad (2.22)$$

Key formula: Resistance of an integrated resistor.

For example, the resistor shown in Figure 2.18 has a length-to-width ratio of three and a resistance of $R = 3R_{\square}$.

Design of an Integrated Resistor

Suppose that we need to design a $10\text{-k}\Omega$ resistor, which is a fairly high value for IC implementation. First, we consider the various films available for the process to be used. Suppose that we are limited to the materials listed in Table 2.1. The resistance needed is fairly large, and we would want to select a material having a high sheet resistance to minimize the chip area consumed by the resistor. Therefore, we choose the base diffusion layer, which has a sheet resistance of $250 \Omega/\square$. Then, using Equation 2.22, we determine that

$$L/W = R/R_{\square} = 40$$

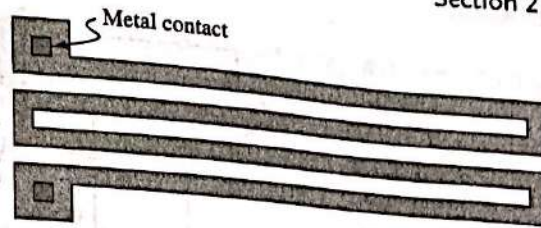
To keep the chip area consumed by the resistor small, we want to choose W as small as possible. However, as W becomes smaller, the tolerance of the resistance becomes larger because of variations in the manufacturing process. Suppose that the resistor to be designed requires moderate accuracy, and a width of $W = 5 \mu\text{m}$ is suitable. Then the length of the resistor would be

$$L = (L/W) \times W = 200 \mu\text{m}$$

Table 2.1. Several materials used to fabricate integrated resistors.

Name of Layer	$R_{\square}(\Omega/\square)$	Absolute Accuracy	Matching Accuracy
Base Diffusion	250	$\pm 20\%$	$\pm 2\%$ ($W = 5 \mu\text{m}$) $\pm 0.2\%$ ($W = 50 \mu\text{m}$)
Polysilicon Gate	20	$\pm 20\%$	$\pm 2\%$
Emitter Diffusion	5	$\pm 20\%$	$\pm 2\%$

Figure 2.19
IC resistors are often folded to keep the distance between the contacts smaller.



Typically, resistors take up much more space than do transistors in ICs. For example, our 10-k Ω resistor occupies an area of $L \times W = 1000 \mu\text{m}^2$, compared with areas as small as $2 \mu\text{m}^2$ for transistors. (Actually, the area consumed by the resistor would be greater than $L \times W$, because some space is needed between the resistor and adjacent components.) Minimizing chip area is a major concern in designing ICs. Thus, as circuit designers, we try very hard to use few resistors and to keep their values small. Later in this book, we will see that many clever circuit configurations substitute transistors for resistors to conserve chip area.

To avoid having resistor terminals relatively far apart compared with the size of other components on the chip, large resistances are commonly folded. (See Figure 2.19.) Furthermore, contacts to the film are made from the top surface using a “dog-bone” contact pad. It turns out that in such a layout, the corner squares count as approximately 0.56 square each and the end pads count for 0.65 square each.

In general, the tolerance of the resistor becomes progressively larger as we consider resistors on a chip, on a wafer, in a single lot, or in different lots. We have seen that the gains of many op-amp circuits depend on the ratios of resistance values. When the resistors are fabricated in the same manner, close together on the same chip, resistance ratios can be maintained with a **matching accuracy** of $\pm 1\%$, or even $\pm 0.1\%$ with laser trimming. On the other hand, resistance values on circuits fabricated in different lots typically have an **absolute accuracy** of $\pm 20\%$.

Minimizing chip area is a major concern in designing ICs.

An important advantage of IC resistors is that resistance ratios tend to be nearly the same on all chips.

Amplifier Design Using Op Amps

Example 2.2 Noninverting-Amplifier Design

Design a noninverting amplifier that has a voltage gain of 10 using an ideal op amp. The input signals lie in the range from -1 V to $+1 \text{ V}$. Use 5%-tolerance discrete resistors for the feedback network.

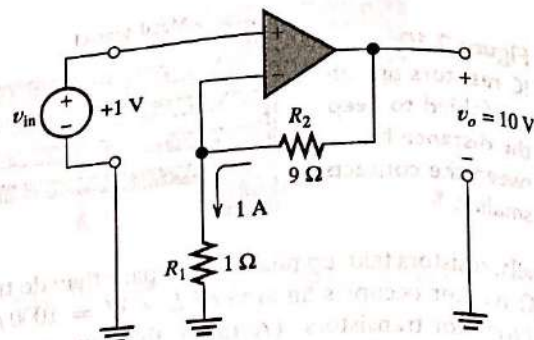
SOLUTION We use the noninverting amplifier configuration of Figure 2.11. The closed-loop gain is given by Equation 2.21. Thus, we have

$$A_v = 10 = 1 + \frac{R_2}{R_1}$$

Theoretically, any resistance values would provide the proper gain, provided that $R_2 = 9R_1$. However, very small resistances are not practical because the current through the resistances must be supplied by the output of the op amp and,

Figure 2.20

If low-value resistors are used, an impractically large current is required.



Very low resistances can result in currents that are too large.

Very large resistances tend to be unstable and lead to coupling of unwanted signals.

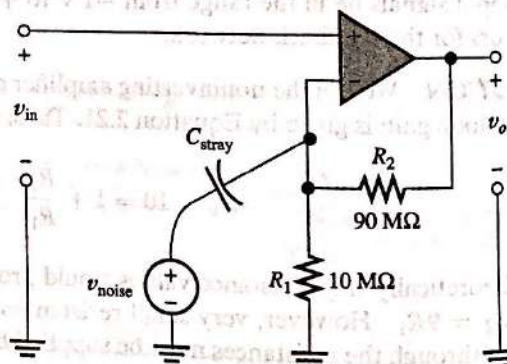
ultimately, by the power supply. For example, if $R_1 = 1\ \Omega$ and $R_2 = 9\ \Omega$, for an output voltage of 10 V, the op amp must supply 1 A of current. (See Figure 2.20.) Most op amps are not capable of such a large output current, and even if they were, the load on the power supply would be unwarranted. In the circuit at hand, we should keep $R_1 + R_2$ large enough so that the current is reasonable. For general design with power supplies operated from the ac power line, currents up to several milliamperes are usually acceptable. (In battery-operated equipment, we would try harder to reduce the current and avoid having to replace batteries frequently.)

Very large resistances, such as $R_1 = 10\ \text{M}\Omega$ and $R_2 = 90\ \text{M}\Omega$, also present problems. As we have seen, large integrated resistances consume excessive chip area. In discrete form, large resistances are unstable in value, particularly in a humid environment. Later, we will see that large resistances lead to problems due to an op-amp imperfection known as offset current. Furthermore, high-impedance circuits are prone to the injection of unwanted signals from nearby circuits through stray capacitive coupling. This is illustrated in Figure 2.21.

Assuming discrete resistors, resistance values between about $100\ \Omega$ and $1\ \text{M}\Omega$ are suitable for use in op-amp circuits. Because the statement of the problem calls for standard 5%-tolerance resistors (see Appendix A), we look for a pair of resistor values such that the ratio R_2/R_1 is 9. One possibility is $R_2 = 180\ \text{k}\Omega$ and $R_1 = 20\ \text{k}\Omega$. However, for many applications, we would find that $R_2 = 18\ \text{k}\Omega$ and $R_1 = 2\ \text{k}\Omega$ would work just as well. Of course, if 5%-tolerance resistors are used, we can expect unit-to-unit variations in the ratio R_2/R_1 of about $\pm 10\%$. This is because R_2 could be 5% low, while R_1 is 5% high, or vice versa. Thus, the

Figure 2.21

If very high value resistors are used, stray capacitance can couple unwanted signals into the circuit.



closed-loop gain of the amplifier (which is $A_v = 1 + R_2/R_1$) varies by about $\pm 9\%$.

If more precision is needed, 1%-tolerance resistors could be used. Another possibility would be an adjustable resistor to set the gain to the desired value. $\square$

Example 2.3 Amplifier Design

Suppose that we need an amplifier with input resistance of $500\text{ k}\Omega$ or greater and a voltage gain of -10 . The feedback resistors are to be implemented in integrated form and have values of $10\text{ k}\Omega$ or less to conserve chip area. Choose a suitable circuit configuration and specify the resistance values. Finally, estimate the resistor tolerances needed so that the gain magnitude is maintained within 5% of its nominal value.

SOLUTION Because a negative gain is required, we first consider using the inverting amplifier of Figure 2.4. To attain the desired input resistance, we would need $R_1 = 500\text{ k}\Omega$, and then to achieve the desired gain, we would need $R_2 = 10R_1 = 5\text{ M}\Omega$. These resistances greatly exceed the maximum value allowed.

A better approach uses two op amps, with the first one configured as a voltage follower and the second as an inverter with a gain of -10 . This is illustrated in Figure 2.22. Then the input impedance is very high (theoretically infinite for the voltage follower). The gain of the circuit is

$$A_v = -\frac{R_2}{R_1}$$

To achieve the desired gain, we need $R_2 = 10R_1$. A good choice of values would be $R_2 = 10\text{ k}\Omega$ and $R_1 = 1\text{ k}\Omega$. These values are within the maximum limit specified. Smaller resistances could be employed that would consume less chip area, but would result in higher power dissipation.

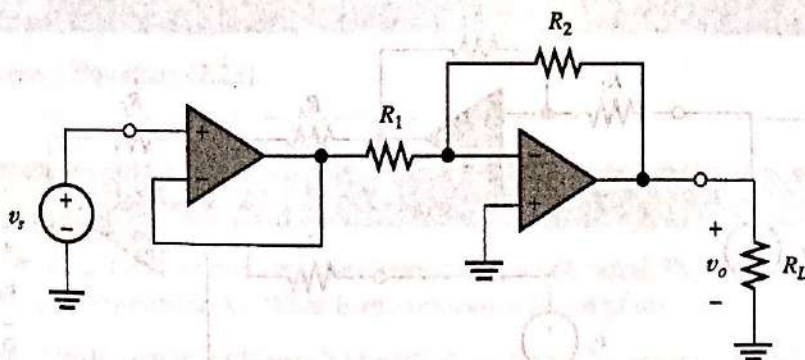


Figure 2.22 To attain large input resistance with moderate resistances for an inverting amplifier, we cascade a voltage follower with an inverter.

To achieve an accuracy of $\pm 5\%$ for the gain magnitude, we need to have a matching accuracy of $\pm 5\%$ for the resistance ratio, which is readily achieved in integrated circuits. The absolute tolerance typically would be $\pm 20\%$, but that is not a problem in this circuit because the gain depends on the resistance ratio.

Example 2.4 Summing-Amplifier Design

You need to be familiar with as many circuits as possible, so you can come up with the best circuit configuration for a given design problem.

Design an amplifier for which the output voltage is $v_o(t) = 5v_1(t) - 2v_2(t)$. Assume that ideal op amps and resistances of any nominal value up to $10\text{ k}\Omega$ are available.

SOLUTION The summer circuit of Figure 2.7 can be used to form the weighted sum of the input voltages given by

$$v_o = -(R_f/R_A)v_A - (R_f/R_B)v_B$$

in which the gains for both input signals are negative. However, the statement of the problem calls for a positive gain for v_1 and a negative gain for v_2 . Thus, we first pass v_1 through an inverting amplifier. The output of this inverter and v_2 are applied to the summer. The proposed circuit diagram is shown in Figure 2.23. It turns out that the output voltage of this circuit is given by

$$v_o = \frac{R_2 R_f}{R_1 R_A} v_1 - \frac{R_f}{R_B} v_2 \quad (2.23)$$

We must select values for the resistors so that the gain for the v_1 input is $+5$ and the gain for the v_2 input is -2 . Many combinations of resistor values can be used to meet these specifications. One possibility is

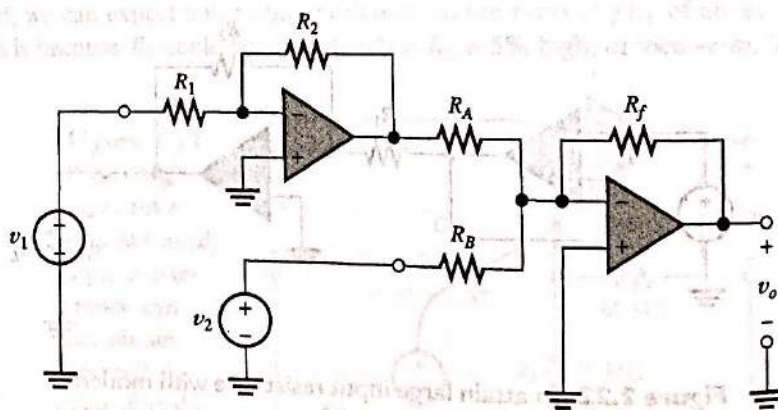


Figure 2.23 Amplifier designed in Example 2.4.

$$R_A = 1 \text{ k}\Omega$$

$$R_B = 1 \text{ k}\Omega$$

$$R_f = 2 \text{ k}\Omega$$

$$R_2 = 2.5 \text{ k}\Omega$$

$$R_1 = 1 \text{ k}\Omega$$

These are by no means the only values that could be used to meet the specifications. Usually, design problems have many "right" answers.

Usually, design problems have many "right" answers.

EXERCISE

2.7 Suppose that we are using a film with $R_{\square} = 300 \Omega/\square$ to design a $6\text{-k}\Omega$ resistor. What L/W ratio is required? If the minimum width allowed is $10 \mu\text{m}$, what area A does the resistor consume? Neglect the area consumed by the guard band required between the resistor and neighboring components.

Answer $L/W = 20$, $A = 2000 (\mu\text{m})^2$.

EXERCISE

2.8 A resistor using a film with $R_{\square} = 100 \Omega/\square$ has the layout illustrated in Figure 2.24. Determine the resistance. Count the corners as 0.56 square each and the end pads as 0.65 square each.

Answer $R = 1642 \Omega$.

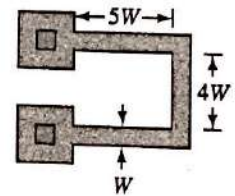


Figure 2.24 Resistor for Exercises 2.8.

EXERCISE

2.9 Derive Equation (2.23).

EXERCISE

2.10 Design a noninverting amplifier having a gain of 4, using 5%-tolerance discrete resistors. (See Appendix A.) What is the tolerance of the gain?

Answer Use the circuit of Figure 2.11 with $R_2 = 3R_1$. Many resistance values would work. One example is $R_2 = 30 \text{ k}\Omega$ and $R_1 = 10 \text{ k}\Omega$. The actual gain varies from $3.714 (-7.14\%)$ to $4.316 (+7.89\%)$.

2.6 OP-AMP IMPERFECTIONS IN THE LINEAR RANGE OF OPERATION

So far we have discussed ideal op amps. In the next few sections of this chapter, we consider the imperfections of real op amps and how to allow for these imperfections in circuit design.

The nonideal characteristics of real op amps fall into three categories:

1. Nonideal properties in the linear range of operation.
2. Nonlinear characteristics.
3. Dc offsets.

We discuss the imperfections for the linear range of operation in this section, including Bode plots of the frequency response of an op amp. (Bode-plot concepts are reviewed in Section 8.1.) In the next several sections, we consider nonlinear characteristics and dc offsets.

A typical integrated circuit op amp is composed of perhaps 30 transistors of several types, about 10 resistors, and one or two capacitors. Op-amp imperfections depend on their internal design, which we discuss in later chapters. For now, we confine our remarks to the external behavior of op amps.

Input Impedance and Output Impedance

An ideal op amp has infinite input impedance and zero output impedance. However, a real op amp has finite input impedance and nonzero output impedance. We will see later in the book that the open-loop input impedance of an op amp depends strongly on the type of transistors used in the input circuits. The open-loop input impedances of IC op amps having bipolar junction transistor (BJT) input stages are usually about $1\text{ M}\Omega$. Op amps having field effect transistor (JFET or MOS) input stages have much higher input impedances—as much as $10^{12}\ \Omega$. Open-loop output impedance is ordinarily between 1 and $100\ \Omega$ for an IC op amp, although it can be as high as several thousand ohms for a low-power op amp.

The closed-loop input and output impedances in a negative-feedback circuit can be markedly different from the open-loop impedances of the op amp. We can select the type of feedback to either increase or decrease the input or output impedance of the circuit. Usually, the open-loop input or output impedances of the op amps do not place serious limits on circuit performance.

Gain and Bandwidth Limitations

Ideal op amps have infinite open-loop gain magnitude and unlimited bandwidth. The gain of a real op amp is a function of frequency, becoming smaller in magnitude at high frequencies. At dc, the open-circuit differential voltage gain of a real op amp is typically between 10^4 and 10^6 .

Usually, the bandwidth of an IC op amp is intentionally limited by the designer. As discussed later in the book, this limitation is called **frequency compensation** and is required to avoid oscillation when feedback is used. Often, compensation requires a capacitor that consumes a substantial portion of the chip area of the op amp.

Categories of op-amp imperfections.

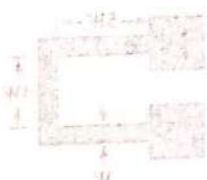


Figure 2.24 Resistor for Exercise 2.8.

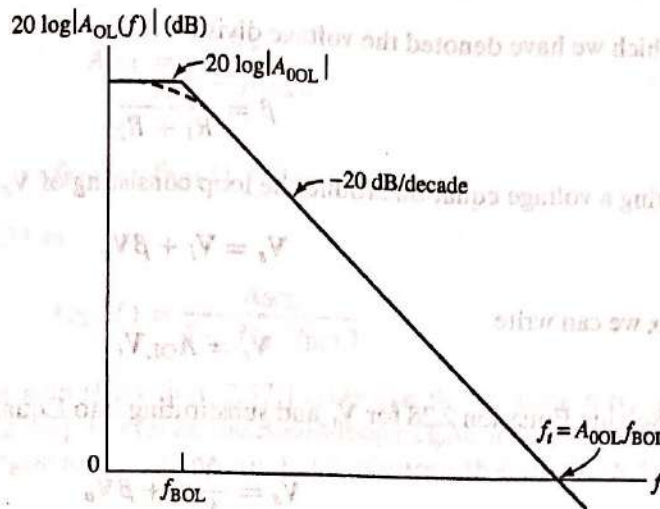


Figure 2.25
Bode plot of
open-loop gain for
a typical op amp.

Generally, in the useful frequency range, the open-loop gain has a single pole of significance called a **dominant pole**. The open-loop transfer function of a dominant-pole op amp is given by

$$A_{OL}(f) = \frac{A_{OL}}{1 + j(f/f_{BOL})} \quad (2.24)$$

where A_{OL} is the dc open-loop gain and f_{BOL} is the open-loop break frequency. In a Bode plot of $A_{OL}(f)$, the gain magnitude is approximately constant up to f_{BOL} . Above f_{BOL} , the gain magnitude rolls off at 20 dB/decade. (See Figure 2.25.)

Consider the noninverting amplifier shown in Figure 2.26. Because we are no longer assuming constant gain at all frequencies, we have denoted the voltages and current as phasors, for which we use boldface symbols. At this point, we assume that the op amp is ideal, except for finite gain that is a function of frequency. Thus, the input impedance of the op amp is assumed to be infinite and the input current I_i is zero.

The feedback network consisting of R_1 and R_2 acts as a voltage divider. The voltage across R_2 is given by

$$\frac{R_1}{R_1 + R_2} \times V_o = \beta V_o \quad (2.25)$$

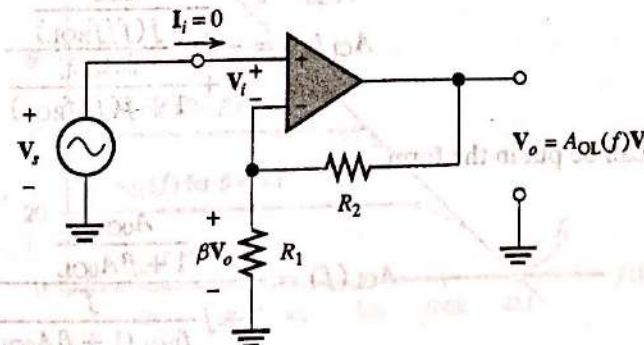


Figure 2.26
Noninverting
amplifier.

Key Equation: Open-loop gain
of a dominant-pole op amp.

in which we have denoted the voltage division ratio as

$$\beta = \frac{R_1}{R_1 + R_2} \quad (2.25)$$

Writing a voltage equation around the loop consisting of V_s , V_i and βV_o , we have

$$V_s = V_i + \beta V_o \quad (2.27)$$

Also, we can write

$$V_o = A_{OL} V_i \quad (2.28)$$

Solving Equation 2.28 for V_i and substituting into Equation 2.27, we have

$$V_s = \frac{V_o}{A_{OL}} + \beta V_o \quad (2.29)$$

Now we define the closed-loop gain as $A_{CL} = V_o/V_s$. Rearranging Equation 2.29, we obtain

$$A_{CL} = \frac{V_o}{V_s} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{1}{\beta + 1/A_{OL}} \quad (2.30)$$

Before we proceed, let us demonstrate that this expression for the closed-loop gain A_{CL} reduces to the expression derived earlier for the gain of the noninverting amplifier, assuming an ideal op amp. If we take the limit as the open-loop gain A_{OL} approaches infinity, we have

$$\lim_{A_{OL} \rightarrow \infty} A_{CL} = \frac{1}{\beta} \quad (2.31)$$

Then using Equation 2.26 to substitute for β , we obtain

$$\lim_{A_{OL} \rightarrow \infty} A_{CL} = 1 + \frac{R_2}{R_1} \quad (2.32)$$

which is the same as the expression for the gain given earlier in Equation 2.21 (except that we are now calling the closed-loop gain A_{CL} instead of A_v).

Now let us look at the closed-loop gain as a function of frequency. Using Equation 2.24 to substitute for A_{OL} in Equation 2.30, we have

$$A_{CL}(f) = \frac{\frac{A_{0OL}}{1 + j(f/f_{BOL})}}{1 + \frac{\beta A_{0OL}}{1 + j(f/f_{BOL})}} \quad (2.33)$$

This can be put in the form

$$A_{CL}(f) = \frac{\frac{A_{0OL}}{1 + \beta A_{0OL}}}{1 + j \frac{f}{f_{BOL}(1 + \beta A_{0OL})}} \quad (2.34)$$

Now, if we define

$$A_{0CL} = \frac{A_{0OL}}{1 + \beta A_{0OL}} \quad (2.35)$$

and

$$f_{BCL} = f_{BOL}(1 + \beta A_{0OL}) \quad (2.36)$$

we can express Equation 2.34 as

$$A_{CL}(f) = \frac{A_{0CL}}{1 + j(f/f_{BCL})} \quad (2.37)$$

Notice that the closed-loop gain [Equation (2.37)] takes exactly the same form as the open-loop gain [Equation (2.24)]. However, the closed-loop dc gain and break frequency have different values than those for the open loop. Let us illustrate this with the following example.

Example 2.5 Closed-Loop Gain Versus Frequency of a Noninverting Amplifier

A certain op amp has an open-loop dc gain of $A_{0OL} = 10^5$ and an open-loop bandwidth of $f_{BOL} = 40$ Hz. Prepare a Bode plot of the open-loop gain. Also, draw the Bode plots of the closed-loop gain for noninverting amplifiers with $\beta = 1$, $\beta = 0.1$, and $\beta = 0.01$.

SOLUTION Converting the open-loop dc gain to decibels, we have

$$A_{0OL} = 20 \log(10^5) = 100 \text{ dB}$$

With a single-pole function, the asymptote of the Bode plot is constant up to the break frequency of 40 Hz and then slopes downward at a rate of 20 dB per decade. The resulting open-loop Bode plot is shown in Figure 2.27.

Using Equations (2.35) and (2.36), we compute the closed-loop dc gains and bandwidths for the various values of β . The results are shown in Table 2.2.

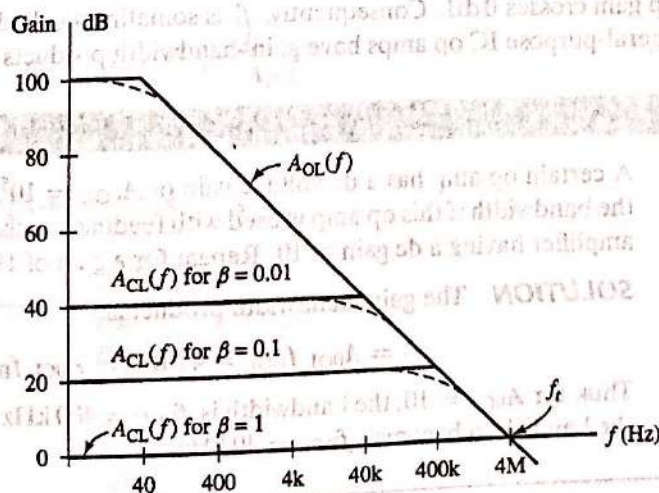


Figure 2.27
Bode plots for
Example 2.5.

These equations apply to the noninverting op-amp configuration.

Table 2.2. Closed-loop dc gain and bandwidth versus β .

β	A_{0CL}	A_{0CL} (dB)	f_{BCL}
		0	4 MHz
1	0.999990	20	400 kHz
0.1	9.9990	40	40 kHz
0.01	99.90		

The Bode plots of the closed-loop gain are shown in Figure 2.27. Notice that as β increases, the dc gain becomes lower and the bandwidth becomes wider. Notice also that the roll-off portions of all of the Bode plots are superimposed.

As shown in Table 2.2, the dc closed-loop gain for $\beta = 0.01$ is $A_{0CL} = 99.9$, whereas the theoretical value assuming an ideal op amp (i.e., $A_{0OL} = \infty$) is $A_{0CL} = 100$. Thus, the actual dc gain is 0.1% lower for this actual op amp than for an ideal op amp. Typically, the discrepancies between real and ideal op amps are small at low frequencies. At such frequencies, the inaccuracies associated with resistor tolerances are usually more significant. On the other hand, at higher frequencies, the discrepancies between real and ideal op amps are great. The gain of the real op amp rolls off, whereas the ideal op amp has infinite bandwidth.

If we take the products of the respective sides of Equations (2.35) and (2.36), we obtain

$$A_{0CL}f_{BCL} = A_{0OL}f_{BOL} \quad (2.38)$$

Thus, the product of the dc gain and bandwidth of the noninverting amplifier is a constant, independent of β . In general, negative feedback reduces the dc gain of an amplifier and extends its bandwidth.

We denote the **gain-bandwidth product** as

$$f_t = A_{0CL}f_{BCL} = A_{0OL}f_{BOL} \quad (2.39)$$

As indicated in Figure 2.27, f_t is also the frequency at which the Bode plot of the open-loop gain crosses 0 dB. Consequently, f_t is sometimes called the **unity-gain bandwidth**. General-purpose IC op amps have gain-bandwidth products of several megahertz.

Example 2.6 Calculation of Gain-Bandwidth Product

A certain op amp has a dc voltage gain of $A_{0OL} = 10^5$ and $f_{BOL} = 40$ Hz. Find the bandwidth if this op amp is used with feedback resistors to form a noninverting amplifier having a dc gain of 10. Repeat for a gain of 100.

SOLUTION The gain-bandwidth product is

$$f_t = A_{0OL}f_{BOL} = 4 \text{ MHz} = A_{0CL}f_{BCL}$$

Thus, for $A_{0CL} = 10$, the bandwidth is $f_{BCL} = 400$ kHz. For a gain of $A_{0CL} = 100$, the bandwidth becomes $f_{BCL} = 40$ kHz.

In general, negative feedback reduces the dc gain of an amplifier and extends its bandwidth.

The gains in this equation are ratios—not in decibels.

Closed-Loop Bandwidth for the Inverter

We can rearrange Equation (2.35) to obtain

$$1 + \beta A_{0OL} = \frac{A_{0OL}}{A_{0CL}} \quad (2.40)$$

Using Equation (2.40) to substitute for $(1 + \beta A_{0OL})$ in Equation (2.36), we have

$$f_{BCL} = f_{BOL} \frac{A_{0OL}}{A_{0CL}} \quad (2.41)$$

However, from Equation (2.39), we see that $f_t = f_{BOL} A_{0OL}$. Furthermore, to a high degree of accuracy, we have $A_{0CL} \cong 1 + R_2/R_1$. Thus, we get

$$f_{BCL} \cong \frac{f_t}{1 + R_2/R_1} \quad (2.42)$$

It turns out that Equation (2.42) applies for the inverting amplifier, as well as for the noninverting amplifier.

Example 2.7 Bandwidths of Inverting and Noninverting Amplifiers

A certain op amp has $f_t = 1$ MHz. Prepare a table showing the closed-loop bandwidth for amplifiers having closed-loop gains of 100, 10, 1, -1, -10, and -100.

SOLUTION For the noninverting amplifiers, we have $A_{0CL} = 1 + R_2/R_1$, and using Equation (2.39), we have

$$f_{BCL} = \frac{f_t}{A_{0CL}} \quad (2.43)$$

On the other hand, for inverting amplifiers, we have $A_{0CL} = -R_2/R_1$. Substituting this into Equation 2.42, we obtain

$$f_{BCL} = \frac{f_t}{1 - A_{0CL}} \quad (2.44)$$

Now substituting the given values into these equations, we obtain the results shown in Table 2.3.

Table 2.3. Closed-loop bandwidth versus gain.

Closed-loop gain	f_{BCL} (kHz)
-100	9.90
-10	90.9
-1	500
+1	1000
+10	100
+100	10

...for a given closed-loop gain magnitude, the inverting amplifier has a smaller bandwidth than the noninverting amplifier.

Notice that for a given closed-loop gain magnitude, the inverting amplifier has a smaller bandwidth than the noninverting amplifier. This is especially true when the gain magnitude is small. For a gain of unity, the inverting amplifier has half the bandwidth of the noninverting amplifier.

Some Popular Op Amps

Literally hundreds of IC op amps are available from dozens of manufacturers. The most enduring and well known is the $\mu A741$, which was introduced by Fairchild Semiconductor in 1966. Other manufacturers provide similar ICs, such as the LM741 (National Semiconductor) and AD741 (Analog Devices). Table 2.4 lists the key specifications for two popular op amps. (Some of these specifications are discussed later in the book.)

Table 2.4. Typical specifications for two popular op amps. The complete data sheets for these devices can be downloaded from the National Semiconductor Web site located at <http://www.national.com>.

Type	LM741	LF411
A_{OL}	2×10^5	2×10^5
f_t	1.5 MHz	4.0 MHz
SR	0.5 V/ μs	15 V/ μs
Input resistance	2 M Ω	10 ¹² Ω
Output resistance	50 Ω	50 Ω
V_{off}	1.0 mV	0.8 mV
I_B	80 nA	50 pA
I_{off}	20 nA	25 pA

EXERCISE

2.11 When a certain dominant-pole op amp is used in a noninverting amplifier configuration with a closed-loop dc gain of 10, the half-power bandwidth is 200 kHz. (a) If the dc open-loop gain is 10^6 , determine the open-loop bandwidth. (b) Determine the half-power bandwidth if the gain of the circuit is changed to 100.

Answer (a) $f_{BOL} = 2$ Hz; (b) 20 kHz.

EXERCISE

2.12 The nominal open-loop dc gain of an op amp is 10^6 . Suppose that this op amp is used in a noninverting amplifier with $\beta = 0.01$. (a) Determine the dc closed-loop gain, accurate to six significant figures. (b) If the open-loop gain decreases by 10%, by what percentage does the closed-loop dc gain change?

Answer (a) $A_{CL} = 99.9900$; (b) $1.11 \times 10^{-3}\%$.

EXERCISE

2.13 Repeat Exercise 2.12 for $\beta = 0.1$.

Answer (a) $A_{0CL} = 9.99990$; (b) $0.111 \times 10^{-3}\%$.

2.7 LARGE-SIGNAL OPERATION

Output Voltage Swing

There are several nonlinear modes of operation for real op amps. First, the output voltage has a maximum limit and a minimum limit. If an input signal is sufficiently large that the output would be driven beyond these limits, the output ceases to respond and **clipping** occurs. In other words, the amplifier **transfer characteristic**, which is the plot of v_o versus v_i , is nonlinear. This is illustrated in Figure 2.28.

...output voltage has a maximum limit and a minimum limit.

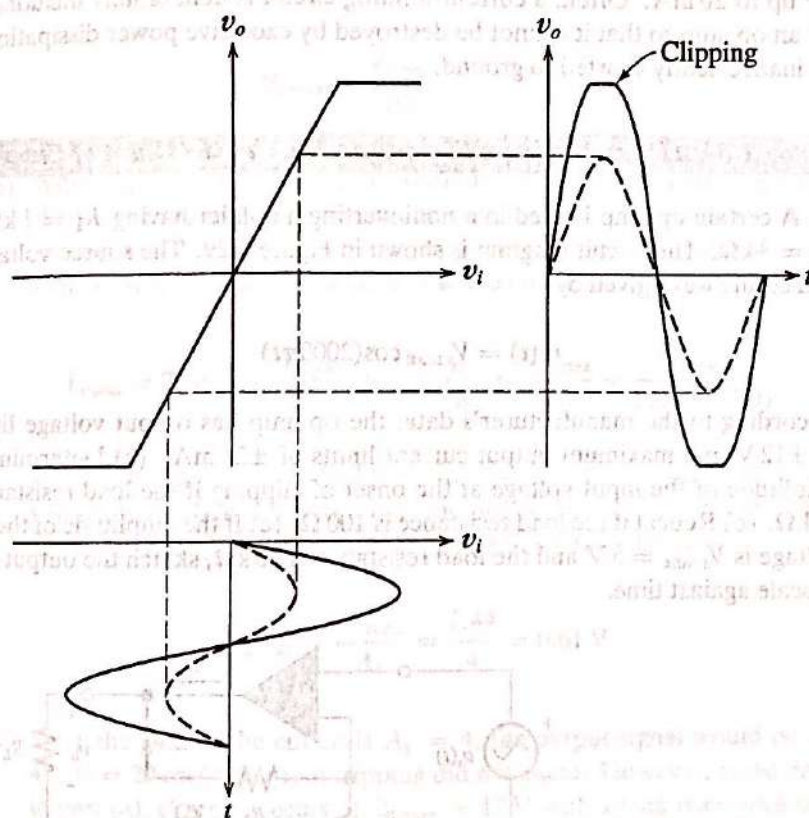


Figure 2.28 For a real op amp, clipping occurs if the output voltage reaches certain limits.

The range of allowed output voltages before clipping occurs depends on the type of op amp in use, on the load resistance, and on the values of the power-supply voltages. For example, with supply voltages of $+15\text{ V}$ and -15 V , the $\mu\text{A}741$ op amp is capable of producing output voltages in the range from approximately -14 V to $+14\text{ V}$. (These are typical limits for load resistances greater than $10\text{ k}\Omega$. The *guaranteed* output range for the $\mu\text{A}741$ is only from -12 V to $+12\text{ V}$. Smaller load resistances further restrict the range.) If smaller power-supply voltages are used, the linear range is reduced.

Some op amps, such as the LM324, are intended to be used with a single power-supply voltage. In that case, the range of allowed output voltages is not symmetrical around zero. For example, with a power-supply voltage of $+15\text{ V}$, the LM324 is limited to output voltages in the range from approximately 20 mV to 13.5 V .

Output Current Limits

Another op-amp limitation is the maximum current that an op amp can supply to a load.

Another op-amp limitation is the maximum current that an op amp can supply to a load. For the $\mu\text{A}741$, the limits are typically $\pm 25\text{ mA}$. If a small-value load resistance drew a current outside these limits, the output waveform would become clipped.

With a $+15\text{-V}$ supply, the typical LM324 can *source* (i.e., provide current flowing out of the op-amp output terminal) up to 30 mA or *sink* (i.e., draw current into the output terminal) up to 20 mA . Often, a current-limiting circuit is deliberately included in the design of an op amp so that it cannot be destroyed by excessive power dissipation if the output is inadvertently shorted to ground.

Example 2.8 Determination of Signal Amplitude at the Onset of Clipping

A certain op amp is used in a noninverting amplifier having $R_1 = 1\text{ k}\Omega$ and $R_2 = 3\text{ k}\Omega$. The circuit diagram is shown in Figure 2.29. The source voltage is 1-kHz sine wave given by

$$v_s(t) = V_{s\max} \cos(2000\pi t)$$

Clipping occurs when either the output voltage or the output current reaches its limit.

According to the manufacturer's data, the op amp has output voltage limits of $\pm 12\text{ V}$ and maximum output current limits of $\pm 25\text{ mA}$. (a) Determine the amplitude of the input voltage at the onset of clipping if the load resistance is $10\text{ k}\Omega$. (b) Repeat if the load resistance is $100\text{ }\Omega$. (c) If the amplitude of the source voltage is $V_{s\max} = 5\text{ V}$ and the load resistance is $10\text{ k}\Omega$, sketch the output voltage to scale against time.

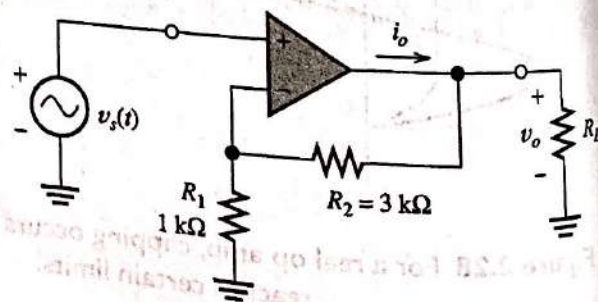


Figure 2.29
Circuit of
Example 2.8.

SOLUTION The closed-loop gain of the noninverting amplifier is

$$A_v = 1 + \frac{R_1}{R_2} = 4$$

Clipping starts when either the output voltage reaches 12 V or the output current reaches 20 mA.

- (a) With a relatively large load resistance, the output current is small, and we anticipate that clipping occurs when the output voltage limits are exceeded. To check this assumption, we compute the output current for an output voltage of 12 V. We have

$$I_{o\max} = \frac{V_{o\max}}{R_L} + \frac{V_{o\max}}{R_1 + R_2} = \frac{12}{10^4} + \frac{12}{3000 + 1000} = 4.2 \text{ mA}$$

which is within the current limits of the op amp. Thus, the circuit is at the onset of clipping for an input amplitude of

$$V_{s\max} = \frac{V_{o\max}}{A_v} = \frac{12}{4} = 3 \text{ V}$$

- (b) With a small load resistance, the output current is large, and we anticipate that clipping occurs when the op-amp output current exceeds 25 mA. To check this assumption, we compute the maximum output voltage for an output current of 25 mA. Writing a current equation at the output of the op amp, we obtain

$$I_{o\max} = 25 \text{ mA} = \frac{V_{o\max}}{R_L} + \frac{V_{o\max}}{R_1 + R_2} = \frac{V_{o\max}}{100} + \frac{V_{o\max}}{3000 + 1000}$$

Solving the equation, we find that $V_{o\max} = 2.44 \text{ V}$, which does not exceed the voltage limit of the op amp. Thus, clipping occurs because of the current limit. The onset of clipping corresponds to a peak source voltage of

$$V_{s\max} = \frac{V_{o\max}}{A_v} = \frac{2.44}{4} = 0.61 \text{ V}$$

- (c) Since the gain of the circuit is $A_v = 4$, the output signal would be $v_o(t) = 4v_s(t) = 20 \cos(2000\pi t)$ if clipping did not occur. However, as we determined in part (a), clipping occurs at $V_{o\max} = 12 \text{ V}$ with a load resistance of $10 \text{ k}\Omega$. Therefore, the output waveform is as shown in Figure 2.30. $\square$

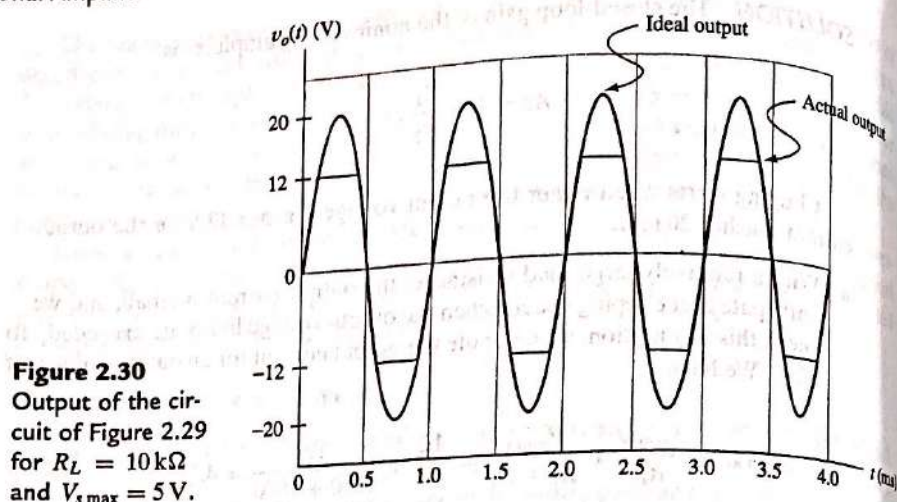


Figure 2.30
Output of the circuit of Figure 2.29 for $R_L = 10 \text{ k}\Omega$ and $V_{s \text{ max}} = 5 \text{ V}$.

EXERCISE

2.14 For the circuit of Example 2.8, determine the input amplitude at the onset of clipping for a load resistance of (a) $1 \text{ k}\Omega$ and (b) 200Ω .

Answer (a) $V_{s \text{ max}} = 3 \text{ V}$; (b) $V_{s \text{ max}} = 0.952 \text{ V}$.

Slew-Rate Limitation

The output voltage of an op amp cannot increase (or decrease) in magnitude at a rate exceeding the slew-rate limit.

Another nonlinear effect in actual op amps is that the magnitude of the rate of change of the output voltage is limited. This is called a **slew-rate limitation**. The output voltage cannot increase (or decrease) in magnitude at a rate exceeding this limit. In equation form, the slew-rate limit is

$$\left| \frac{dv_o}{dt} \right| \leq \text{SR} \quad (2.45)$$

For various types of IC op amps, the slew-rate limit ranges from $\text{SR} = 10^5 \text{ V/s}$ to $\text{SR} = 10^8 \text{ V/s}$. For the $\mu\text{A}741$ with $\pm 15\text{-V}$ supplies and $R_L > 2 \text{ k}\Omega$, the typical value is $5 \times 10^5 \text{ V/s}$ (which is often stated as $0.5 \text{ V}/\mu\text{s}$).

Slew-rate limiting can cause the output waveform of an actual op amp to be much different from that of an ideal op amp. For example, consider the noninverting amplifier shown in Figure 2.29. Suppose that the op amp has an slew-rate limit of $0.5 \text{ V}/\mu\text{s}$ and the input is a 50-kHz sine wave given by

$$\begin{aligned} v_s(t) &= 0 \quad t < 0 \\ &= 2.5 \sin(10^5 \pi t) \quad t \geq 0 \end{aligned}$$

The output voltage waveform is illustrated in Figure 2.31. Also plotted in the figure is four times the source voltage—which is the output, assuming an ideal op amp. At $t = 0$, the output voltage is zero. The ideal output increases at a rate exceeding the slew-rate limit of the op amp, so the op amp output increases at its maximum rate, which is $0.5 \text{ V}/\mu\text{s}$. At point A the actual output finally catches up with the ideal output, but by then the ideal output is decreasing at a rate that exceeds the slew-rate limit. Thus, at point A, the output of the op amp begins to decrease at its maximum possible rate. Notice that, because of slew-rate limiting, the actual op-amp output is a triangular waveform.

Full-Power Bandwidth

The **full-power bandwidth** of an op amp is the range of frequencies for which the op amp can produce an undistorted sinusoidal output with peak amplitude equal to the guaranteed maximum output voltage. Next we derive an expression for the full-power bandwidth in terms of the slew rate and peak amplitude. The output voltage is given by

$$v_o(t) = V_{o\max} \sin(\omega t)$$

Taking the derivative with respect to time, we obtain

$$\frac{dv_o(t)}{dt} = \omega V_{o\max} \cos(\omega t)$$

The maximum magnitude of the rate of change is $\omega V_{o\max} = 2\pi f V_{o\max}$. Setting this expression equal to the slew-rate limit, we have

$$2\pi f V_{o\max} = \text{SR}$$

Solving for frequency, we obtain

$$f_{\text{FP}} = \frac{\text{SR}}{2\pi V_{o\max}} \quad (2.46)$$

where we have denoted the full-power bandwidth as f_{FP} . An undistorted full-amplitude sinusoidal output waveform is possible only for frequencies less than f_{FP} .

The full-power bandwidth of an op amp is the range of frequencies for which the op amp can produce an undistorted sinusoidal output with peak amplitude equal to the guaranteed maximum output voltage.

Equation for full-power bandwidth in terms of slew rate and peak output voltage.

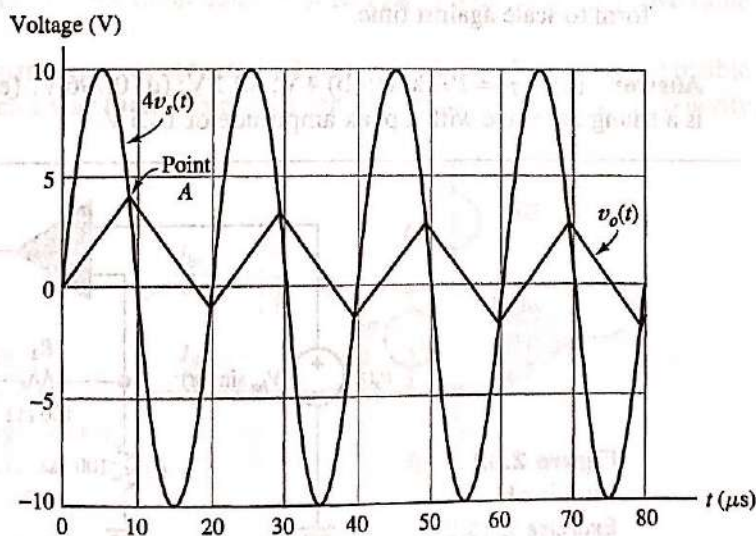


Figure 2.31
Output of the
circuit of Figure 2.29
for $R_L = 10 \text{ k}\Omega$
and $v_s(t) =$
 $2.5 \sin(10^5 \pi t)$.
Note the slew-rate
limiting.

Example 2.9 Determination of Full-Power Bandwidth

Find the full-power bandwidth of the $\mu A741$ op amp, given that the slew rate is $SR = 0.5 \text{ V}/\mu\text{s}$ and the guaranteed maximum output amplitude is $V_{o\text{max}} = 12 \text{ V}$.

SOLUTION We substitute the given data into Equation (2.46) to get

$$f_{\text{FP}} = \frac{SR}{2\pi V_{o\text{max}}} \cong 6.6 \text{ kHz}$$

Thus, we can obtain an undistorted 12-V-peak sinusoidal output from the $\mu A741$ only for frequencies less than 6.6 kHz.

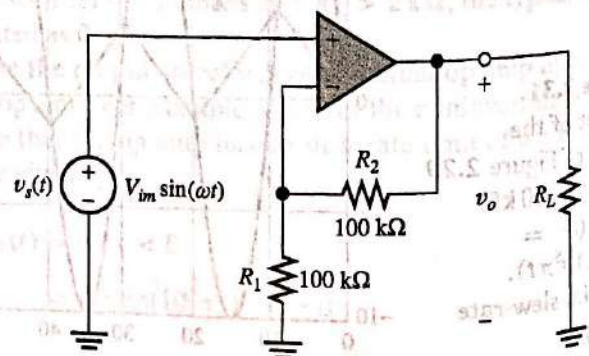
EXERCISE

2.15 A certain op amp has a maximum output voltage range from -4 to $+4 \text{ V}$. The output can source or sink a maximum current of 10 mA . The slew-rate limit is $SR = 5 \text{ V}/\mu\text{s}$. This op amp is used in the circuit of Figure 2.32. (Assume a sinusoidal input signal for all parts of this exercise.)

- Find the full-power bandwidth of the op amp.
- For a frequency of 1 kHz and $R_L = 1 \text{ k}\Omega$, what peak output voltage is possible without distortion?
- For a frequency of 1 kHz and $R_L = 100 \Omega$, what peak output voltage is possible without distortion?
- For a frequency of 1 MHz and $R_L = 1 \text{ k}\Omega$, what peak output voltage is possible without distortion?
- If $R_L = 1 \text{ k}\Omega$ and $v_s(t) = 5 \sin(2\pi 10^6 t)$, sketch the steady-state output waveform to scale against time.

Answer (a) $f_{\text{FP}} = 199 \text{ kHz}$; (b) 4 V ; (c) 1 V ; (d) 0.796 V . (e) The output waveform is a triangular wave with a peak amplitude of 1.25 V .

Figure 2.32
Circuit of
Exercise 2.15.



2.8 DC IMPERFECTIONS

Op amps have direct-coupled input circuits. Dc currents flow into (or out of) the input devices of the op amp through the elements that are connected to the input terminals, such as the signal source or feedback resistors. The dc current flowing into the noninverting input is denoted as I_{B+} , and the dc current flowing into the inverting input is I_{B-} . The average of the dc currents is called **bias current** and is denoted as I_B . Thus, we have

$$I_B = \frac{I_{B+} + I_{B-}}{2} \quad (2.47)$$

Nominally, the input circuits of op amps are symmetrical, and the bias currents flowing in the inverting and noninverting inputs are equal. However, in practice, the devices are not perfectly matched, and the bias currents are not equal. The difference between the bias currents is called the **offset current** and is denoted as I_{off} . Thus,

$$I_{off} = I_{B+} - I_{B-} \quad (2.48)$$

Another dc imperfection of op amps is that the output voltage may not be zero for zero input voltage. The op amp behaves as if a small dc source known as an **offset voltage** is in series with one of the input terminals.

The three dc imperfections can be modeled by placing dc sources at the input of the op amp as illustrated in Figure 2.33. The I_B sources model the bias current; the $I_{off}/2$ source models the offset current, and the V_{off} source models the offset voltage.

The bias current sources are equal in magnitude and are referenced in the same direction (which is away from the input terminals in Figure 2.33). In some op amps, the bias current can have a negative value, so the current sources point toward the input terminals. Usually, the direction of the bias current is predictable for a given type of op amp. For example, we will see later that if the input terminals of an op amp are the base terminals of *nnp* BJTs, the bias current I_B is positive (assuming the reference directions illustrated in Figure 2.33). On the other hand, *pnp* BJTs would result in a negative value for I_B .

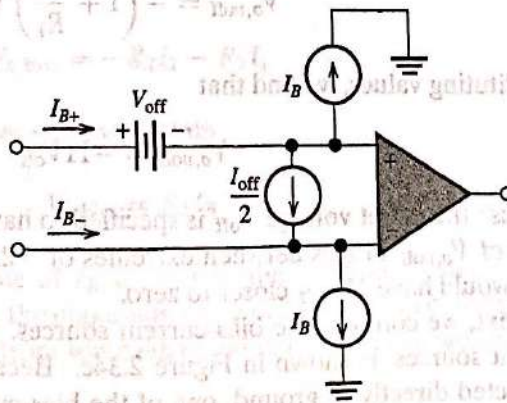
Because the bias-current sources are matched in magnitude and direction, it is possible to design circuits in such a way that their effects cancel. On the other hand, the polarity

Dc imperfections can be modeled by placing dc sources at the input of the op amp as shown in Figure 2.33.

The three dc imperfections of real op amps are

1. input bias current,
2. input offset current, and
3. input offset voltage.

Figure 2.33
Current sources and a voltage source model the dc imperfections of an op amp.



The effect of bias current, offset current, and offset voltage on inverting or noninverting amplifiers is to add a (usually undesirable) dc voltage to the intended output signal.

First compute the output voltage due to the input offset voltage source.

Second, compute the output voltage caused by the bias-current sources.

of the offset voltage and direction of the offset current are unpredictable—varying from unit to unit. For example, if the offset voltage of a given type of op amp is specified as a maximum of 2 mV, the value of V_{off} can range between -2 and $+2$ mV from unit to unit. Usually, most units have offset values close to zero, and only a few have values close to the maximum specification. A typical specification for the maximum offset voltage magnitude for IC op amps is several millivolts.

Bias currents are on the order of 100 nA for op amps with BJT inputs. Bias currents are much lower for op amps with junction field effect transistor (JFET) inputs—a typical specification is 100 pA at 25°C for a device with JFET inputs. Op amps with metal–oxide–semiconductor (MOS) transistor input circuits have even lower bias currents. Offset current specifications commonly range from 20 to 50% of the bias current.

The effect of bias current, offset current, and offset voltage on inverting or noninverting amplifiers is to add a (usually undesirable) dc voltage to the intended output signal. We can analyze these effects by considering the sources shown in Figure 2.33 and assuming an otherwise ideal op amp.

Example 2.10 Worst-Case DC Output Voltage of an Inverting Amplifier

Find the worst-case dc output voltage of the inverting amplifier shown in Figure 2.34a, assuming that $v_{\text{in}} = 0$. The maximum bias current of the op amp is 100 nA, the maximum offset current magnitude is 40 nA, and the maximum offset voltage magnitude is 2 mV.

SOLUTION Our approach is to calculate the output voltage due to each of the dc sources acting individually. Then, using superposition, we can find the worst-case output by adding the outputs due to the various sources.

First, we consider the offset voltage. The circuit including the offset voltage source is illustrated in Figure 2.34b. The offset voltage source can be placed in series with either input. We have elected to place it in series with the noninverting input. Then the circuit takes the form of a noninverting amplifier (i.e., notice that although it is drawn differently, the circuit of Figure 2.34b is electrically equivalent to the noninverting amplifier of Figure 2.11). Thus, the output voltage is the gain of the noninverting amplifier times the offset voltage:

$$V_{o,\text{voff}} = -\left(1 + \frac{R_2}{R_1}\right) V_{\text{off}}$$

Substituting values, we find that

$$V_{o,\text{voff}} = -11V_{\text{off}}$$

Because the offset voltage V_{off} is specified to have a maximum value of 2 mV, the value of $V_{o,\text{voff}}$ ranges between extremes of -22 and $+22$ mV. However, most units would have $V_{o,\text{voff}}$ closer to zero.

Next, we consider the bias-current sources. The circuit, including the bias-current sources, is shown in Figure 2.34c. Because the noninverting input is connected directly to ground, one of the bias-current sources is short circuited

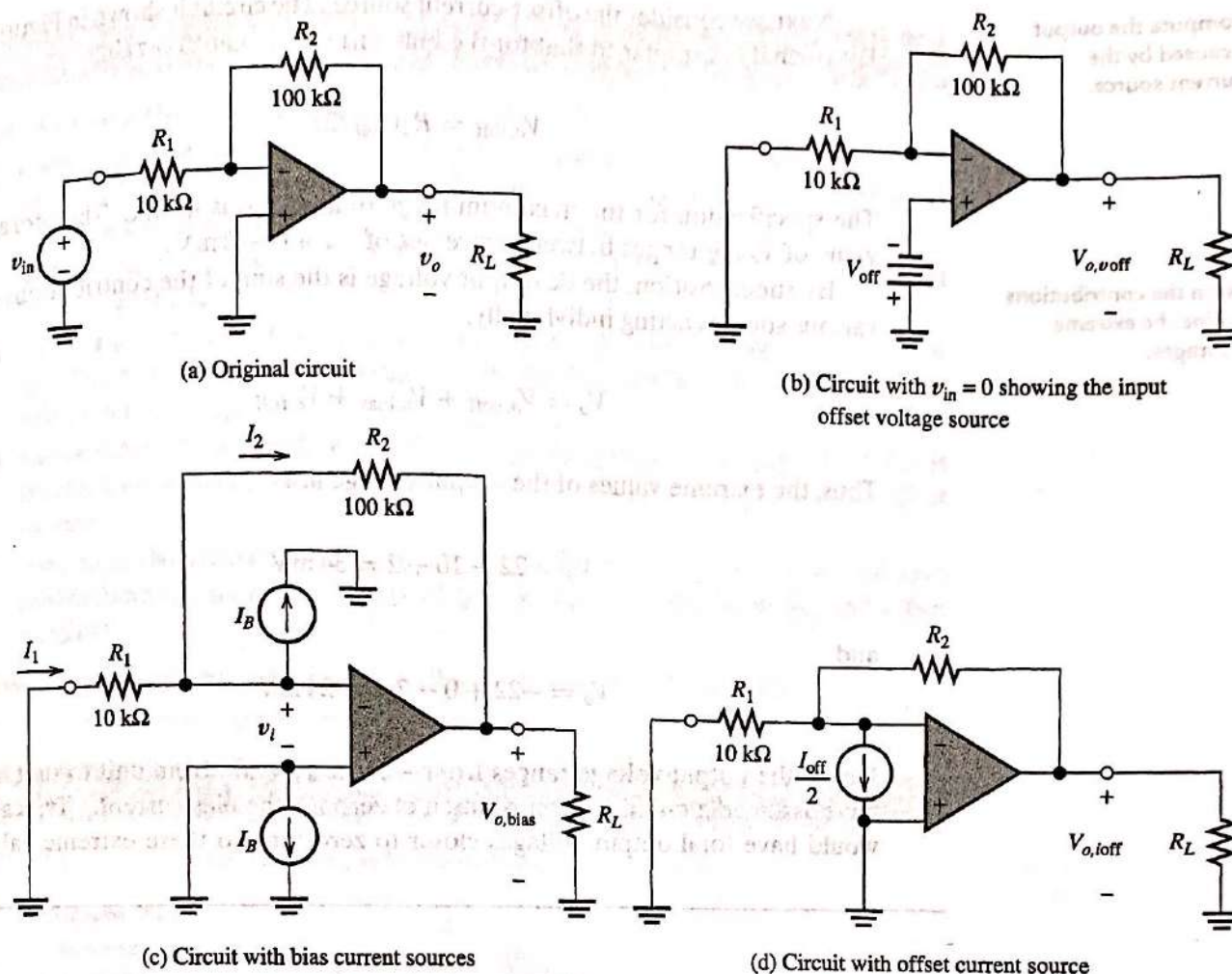


Figure 2.34 Circuit of Example 2.10.

and has no effect. Since we assume an ideal op amp (aside from the dc sources), the summing-point constraint applies, and $v_i = 0$. Thus, the current I_1 is zero. Applying Kirchhoff's current law, we have $I_2 = -I_B$. Writing a voltage equation from the output through R_2 and R_1 , we have

$$V_{o,bias} = -R_2 I_2 - R_1 I_1$$

Substituting $I_1 = 0$ and $I_2 = -I_B$, we obtain

$$V_{o,bias} = R_2 I_B$$

Because the maximum value of I_B is 100 nA, the maximum value of $V_{o,bias}$ is 10 mV. As is often the case, the maximum value of I_B is specified, but the minimum is not. Thus, $V_{o,bias}$ ranges from some small indeterminate voltage (perhaps a few millivolts) up to 10 mV.

Third, compute the output voltage caused by the offset-current source.

Finally, sum the contributions to determine the extreme output voltages.

Next, we consider the offset-current source. The circuit is shown in Figure 2.34d. By an analysis similar to that for the bias current, we can show that

$$V_{o,ioff} = R_2(I_{off}/2)$$

The specification for the maximum magnitude of I_{off} is 40 nA. Therefore, the value of $V_{o,ioff}$ ranges between extremes of -2 and $+2$ mV.

By superposition, the dc output voltage is the sum of the contributions of the various sources acting individually:

$$V_o = V_{o,voff} + V_{o,bias} + V_{o,ioff}$$

Thus, the extreme values of the output voltage are

$$V_o = 22 + 10 + 2 = 34 \text{ mV}$$

and

$$V_o = -22 + 0 - 2 = -24 \text{ mV}$$

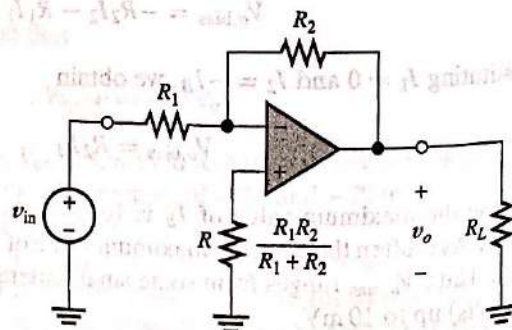
Hence the output voltage ranges from -24 to $+34$ mV from unit to unit. (We have assumed a minimum contribution of zero for the bias current.) Typical units would have total output voltages closer to zero than to these extreme values.

Adding a resistor R in series with the noninverting op-amp input as shown in Figure 2.35 ... results in cancellation of the effects of the I_B sources.

Cancellation of the Effects of Bias Currents

As mentioned earlier, it is possible to design circuits in which the effects of the two bias-current sources cancel. For example, consider the inverting amplifier configuration. Adding a resistor R in series with the noninverting op-amp input as shown in Figure 2.35 does not affect the gain of the amplifier, but results in cancellation of the effects of the I_B sources. Notice that the value of R is equal to the parallel combination of R_1 and R_2 .

Figure 2.35
Adding the resistor R to the inverting amplifier circuit causes the effects of bias currents to cancel.



EXERCISE

2.16 Consider the amplifier illustrated in Figure 2.35.

- Assume an ideal op amp, and derive an expression for the voltage gain v_o/v_{in} . Notice that the result is the same as Equation (2.5), which was derived for the inverting amplifier without the bias-current-compensating resistor R .
- Redraw the circuit with $v_{in} = 0$, but include the bias-current sources. Show that the output voltage is zero.
- Assume that $R_1 = 10\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, and the maximum magnitude of V_{off} is specified to be 3 mV . Find the range of output voltages resulting from the offset voltage source V_{off} .
- Assume that $R_1 = 10\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, and the maximum magnitude of I_{off} is specified to be 40 nA . Find the range of output voltages resulting from the offset current.
- Assuming the values given in parts (c) and (d), what range of output voltages results from the combined action of the bias current, offset voltage, and offset current?

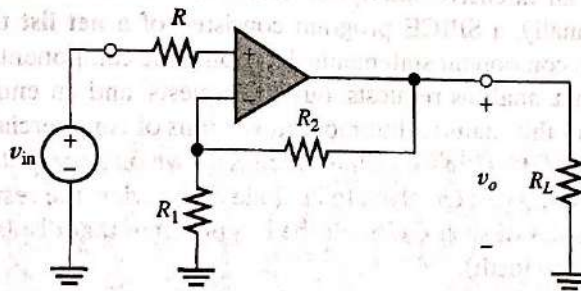
Answer (a) $v_o/v_{in} = -R_2/R_1$; (c) $\pm 33\text{ mV}$; (d) $\pm 4\text{ mV}$; (e) $\pm 37\text{ mV}$.

EXERCISE

2.17 Consider the noninverting amplifier shown in Figure 2.36.

Figure 2.36

Noninverting amplifier, including resistor R to balance the effects of the bias currents. See Exercise 2.17.



- Derive an expression for the voltage gain v_o/v_{in} . Does the gain depend on the value of R ? Explain.
- Derive an expression for R in terms of the other resistor values, so that the output voltage due to the bias currents is zero.

Answer

- $v_o/v_{in} = 1 + R_2/R_1$. The gain is independent of R , because the current through R is zero (assuming an ideal op amp).
- $R = R_1 || R_2$. (We use this notation to indicate the parallel combination of R_1 and R_2 .)

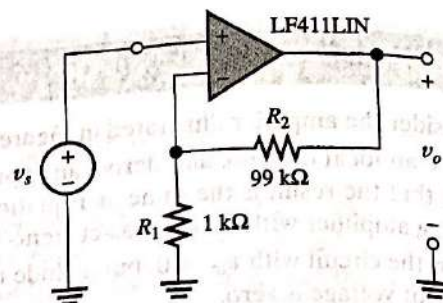


Figure 2.37
Noninverting amplifier.

2.9 COMPUTER-AIDED ANALYSIS OF OP-AMP CIRCUITS

Computers are indispensable in the design of complex integrated circuits. An important design tool is SPICE, which is an acronym for “Simulation Program with Integrated Circuit Emphasis.” The original program was developed at the University of California at Berkeley and released into the public domain. Several commercial versions are currently available. Possibly you have encountered some version of SPICE in your introductory circuits courses.

In this book, we illustrate computer-aided analysis of electronic circuits by using the free evaluation versions of *Schematics*, *PSPice*, and *Probe* from OrCAD. We also supply schematic files on the website, so that you can modify the circuits and experiment with the simulations. As newer versions of the software become available, we will place updated circuit files on our Web site. We do not have space in this book to give a complete discussion of these programs. A number of books are listed in the bibliography that will give you an extensive description of this software if needed.

Originally, a SPICE program consisted of a **net list** that included the title of the program, component statements describing the components and circuit topology, model statements, analysis requests, output requests, and an end statement. SPICE can still be used in this manner, but modern versions of commercial software use **graphical user interfaces** (GUIs), in which the circuit is drawn on a computer screen and menus are used to select the type of analysis to be done and to view the results. *Schematics* and *Capture* are examples of such GUIs. *Probe* is a program that displays results (waveforms, Bode plots, and so forth).

Bode Plots Using AC Analysis

Next, we use SPICE to find the Bode plot of the voltage gain for the noninverting amplifier shown in Figure 2.37. We have used *Schematics* to draw this circuit. The circuit file is named Fig2.37 and can be found on the website. After loading the software and starting *Schematics*, you can load the file by using the **file/open** command.

We want to observe the Bode plot of the closed-loop gain of this circuit, so we specify an ac sweep analysis of the circuit. We use the **analysis/setup** command to display the menu shown in Figure 2.38. We click the left mouse button on **AC Sweep**, which brings up the window shown in Figure 2.39. For a Bode plot, we select **Decade** as the AC Sweep Type.

Schematic files for the circuits simulated in this book can be downloaded from our Web site, www.prenhall.com/hambley

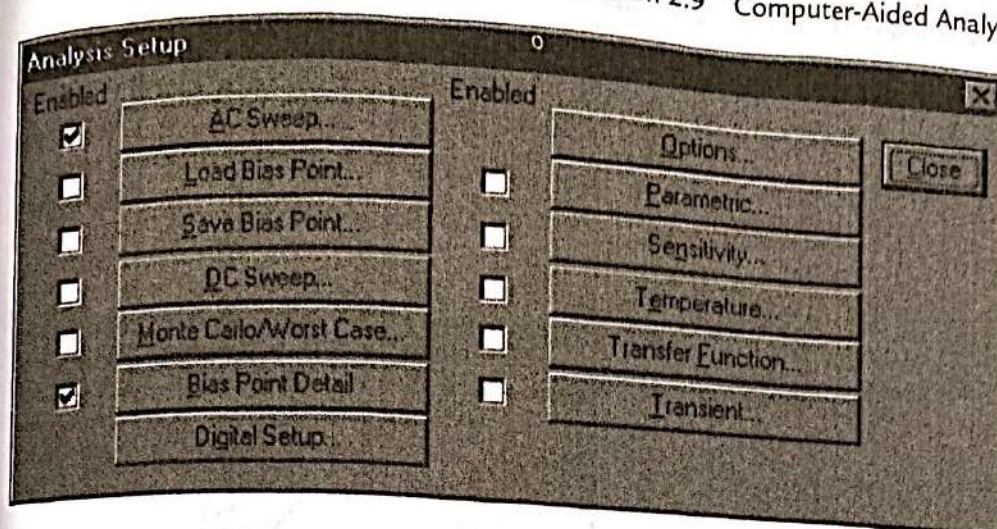


Figure 2.38 Analysis setup window.

Now we must select the starting and ending frequencies for the analysis. Looking at the circuit shown in Figure 2.37, we see that we have a noninverting amplifier. We expect the dc closed-loop gain to be

$$A_{0CL} = 1 + \frac{R_2}{R_1} = 100$$

which is equivalent to 40 dB. The unity-gain bandwidth of the LF411 is approximately $f_t = 4$ MHz, and we expect the closed-loop half-power frequency to be

$$f_{BCL} = \frac{f_t}{A_{0CL}} = 40 \text{ kHz}$$

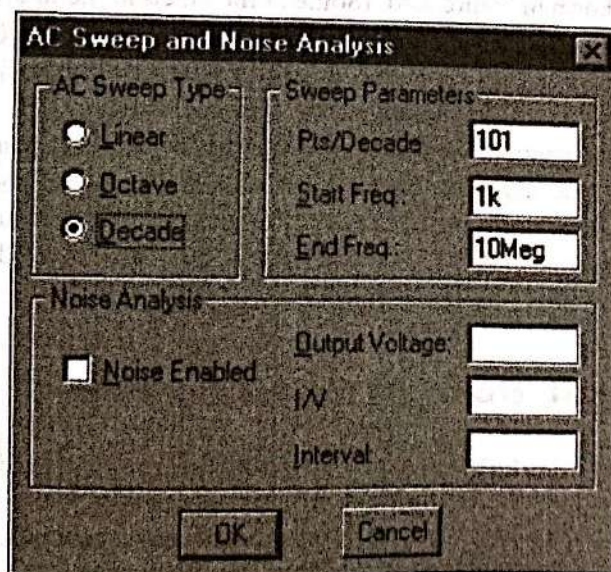


Figure 2.39
Ac sweep window.

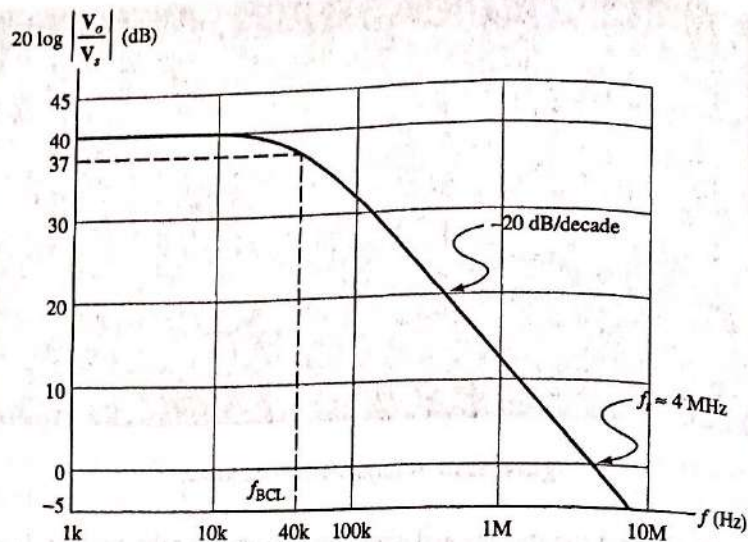


Figure 2.40 Bode plot of the gain magnitude for the circuit of Figure 2.37.

Thus, we have selected the starting frequency as 1 kHz and the ending frequency as 10 MHz, because this range will display the key features of the Bode plot. After making these selections, we close the AC Sweep window and the Analysis Setup window.

Next, we use the **analysis/simulate** commands to invoke a PSpice analysis of the circuit. After PSpice finishes the analysis, Probe starts. We then request a plot of $20 \log |V_o|$, in which V_o is the phasor for the op-amp output voltage. This plot is the gain V_o/V_i in decibels, because we selected a source signal having unity amplitude. The resulting Bode plot is shown in Figure 2.40. (Some of the labels in the figure were added later.)

As expected, we see that the closed-loop dc gain is 40 dB, the closed-loop break frequency is $f_{BCL} = 40 \text{ kHz}$, the unity-gain bandwidth is $f_t = 4 \text{ MHz}$, and the slope of the rolloff is -20 dB/decade .

For convenience in the preceding example, we used an input voltage of 1 V, resulting in an output of 100 V. However, the LF411 op amp is not capable of producing such a large output. PSpice uses a linear model for nonlinear devices in ac analysis, and we must keep in mind that the voltage magnitudes encountered in an ac analysis may not be realistic.

...keep in mind that the voltage magnitudes encountered in an ac analysis may not be realistic.

Linear Macromodel for the Op Amp

Macromodels are subcircuits that are convenient for representing the external behavior of op amps in SPICE programs. A macromodel does not faithfully represent the internal structure of an op amp. One of the advantages of a macromodel is that it is simpler and leads to faster simulation than with a detailed model of the actual internal circuit.

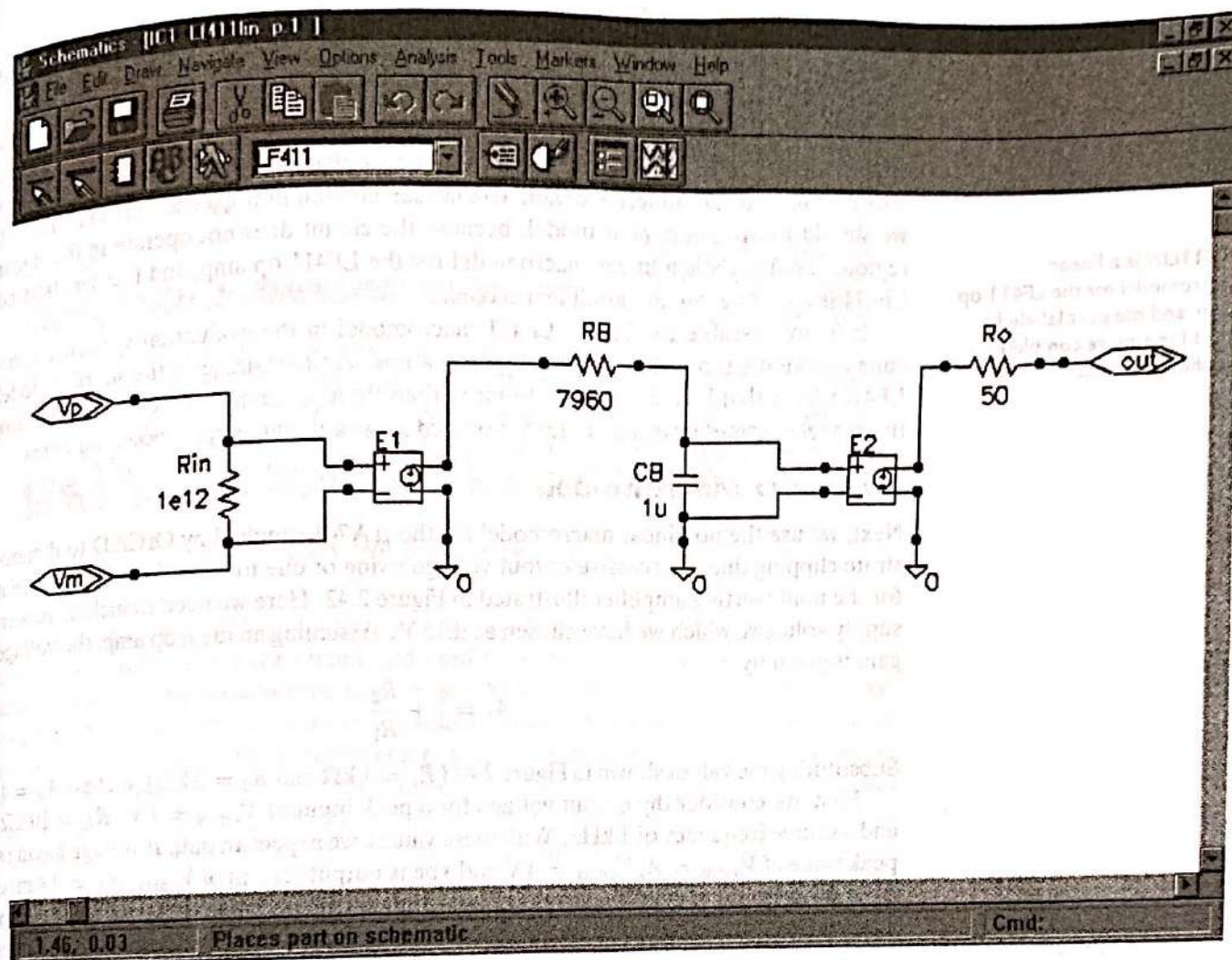


Figure 2.41 Linear macromodel for the internally compensated op amp.

For example, if we return to the circuit of Figure 2.37 and double click the left button of the mouse while the cursor is on the op-amp symbol, we can see the subcircuit macromodel that we have used for the LF411. The subcircuit is shown in Figure 2.41. The resistance R_{in} models the input resistance of the op amp, and R_o models the output resistance. The resistance R_B and capacitance C_B form a low-pass filter that models the open-loop frequency response. The open-loop break frequency is given by

$$f_{BOL} = \frac{1}{2\pi R_B C_B} \quad (2.49)$$

In choosing values of R_B and C_B to use in the macromodel, either C_B or R_B is selected arbitrarily. Then, assuming that f_{BOL} is known for the op amp to be modeled, Equation (2.49) is used to compute the other value. It is not necessary to select practical values for either R_B or C_B . Element E_1 is a voltage-controlled voltage source, having a gain constant of unity. E_2 is a voltage-controlled voltage source, having a gain constant equal

LF411LIN is a linear macromodel for the LF411 op amp, and the part labeled LF411 is a more complete nonlinear model.

to the dc open-loop gain of the op amp A_{OL} . Usually, values for f_{BOL} , A_{OL} , R_{in} , and R_o can be determined from data given by the manufacturer.

This linear macromodel must be used with caution—it provides realistic results only if the circuit operation remains in the linear range of the op amp. The more complex macromodels provided by device and software manufacturers take the nonlinear effects into account. For example, if we wanted to model the Schmitt trigger circuit of Figure 2.10, we should use the nonlinear model, because the circuit does not operate in the linear region. LF411LIN is a linear macromodel for the LF411 op amp, and the part labeled LF411 is a more complete nonlinear model.

It is not possible to use the LF411 macromodel in the evaluation version for circuits containing more than two or three op amps. An advantage of the simpler model LF411LIN is that linear circuits with more than three op amps can be analyzed. Also, the model parameters can be readily modified for simulating other types of op amps.

Nonlinear Macromodels

Next, we use the nonlinear macromodel for the $\mu A741$ supplied by OrCAD to demonstrate clipping due to excessive output voltage swing or due to excessive output current for the noninverting amplifier illustrated in Figure 2.42. Here we need to include power-supply voltages, which we have chosen as ± 15 V. Assuming an ideal op amp, the voltage gain is given by

$$A_v = 1 + \frac{R_2}{R_1}$$

Substituting the values shown in Figure 2.42 ($R_1 = 1 \text{ k}\Omega$ and $R_2 = 3 \text{ k}\Omega$), we find $A_v = 4$.

First, we consider the output voltage for a peak input of $V_{s \max} = 1 \text{ V}$, $R_L = 10 \text{ k}\Omega$, and a source frequency of 1 kHz. With these values, we expect an output voltage having a peak value of $V_{o \max} = A_v V_{s \max} = 4 \text{ V}$ and a peak output current of $V_{o \max} / R_L = 0.4 \text{ mA}$. Both the peak current and peak voltage are within the linear range of the $\mu A741$ op amp. Thus, we expect the output to be an undistorted sine wave. We must perform a transient

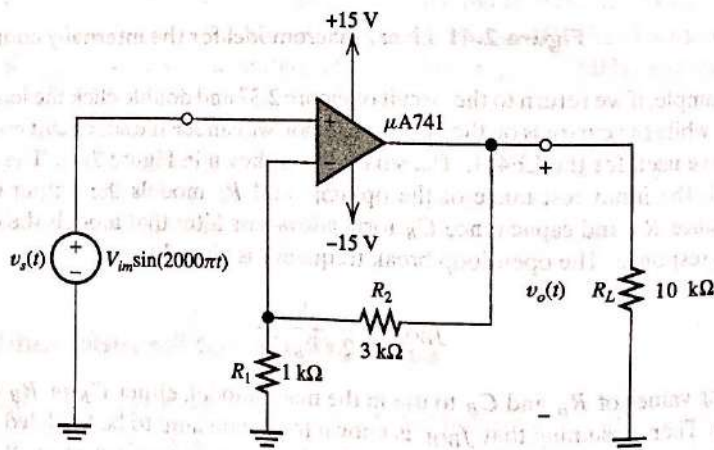


Figure 2.42 Noninverting amplifier used to demonstrate nonlinear effects.

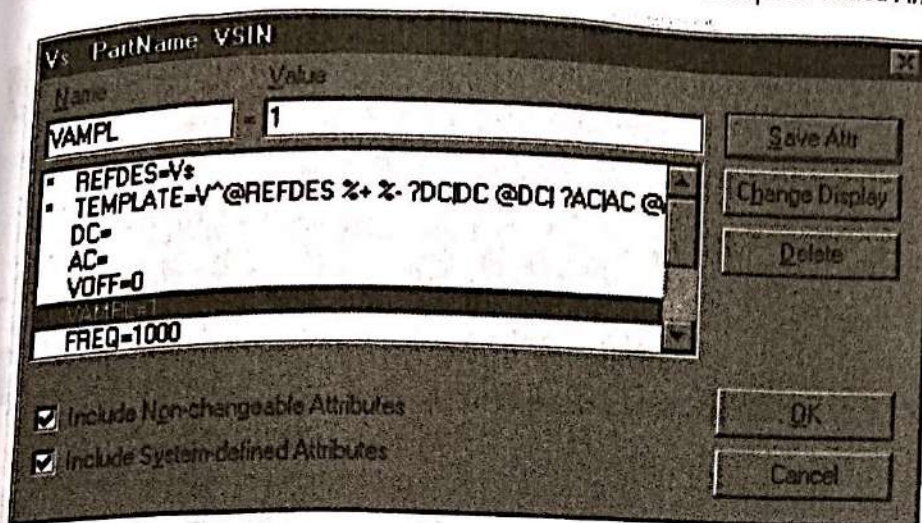


Figure 2.43 Window for the source $v_s(t)$.

analysis to demonstrate the nonlinear properties of the op amp. (In an ac analysis, a linear model is found for the circuit and used by PSpice, so nonlinear effects are not seen.) To set up the input source $v_s(t) = \sin(2000\pi t)$, we use the mouse and double click the left button with the cursor on the source symbol. This brings up the menu shown in Figure 2.43. Because we do not intend to perform a dc analysis or an ac analysis, we do not need to give values for the attributes "DC=" or "AC=". However, we must set the source attributes that are used in transient analysis. The attribute "VOFF" is the dc component of the source, "VAMPL" is the peak amplitude, and "FREQ" is the frequency. Thus, we set VOFF = 0, VAMPL = 1, and FREQ = 1000. Remember to click the **Save Attr** button with the mouse after entering a value for each attribute; otherwise the values are not saved.

Next, we use the **analysis/setup/transient** commands to bring up the transient-analysis setup window, shown in Figure 2.44. We have selected a final time of 4 ms, so the simulation will show a few (namely, four) cycles of the 1-kHz signal. If you run this program and use Probe to examine the output waveform, you will observe that the output signal is an undistorted sine wave with a 4-V peak, just as is expected from the analysis assuming an ideal op amp.

Now we return to the schematic. Double click the left button of your mouse with the cursor on the input source, and increase the input amplitude to VAMPL = 5 V. For an ideal op amp, this would result in a peak output of $V_{o\max} = 20$ V. However, the $\mu A741$ clips at a peak output of approximately 14 V. Changing the peak value of the input in the PSpice program given earlier results in the output voltage waveform shown in Figure 2.45. Notice the clipping of the waveform.

Next, we reduce the peak input amplitude to 1 V and also reduce the load resistance to $R_L = 50 \Omega$. For an ideal op amp, we would expect a peak output voltage of $V_{o\max} = 4$ V and a peak load current of $V_{o\max}/R_L = 80$ mA. However, the output current of the $\mu A741$ is limited to 40 mA. (The model simulates a $\mu A741$ with the *maximum* specification of the output current limit. However, the *typical* output current limit is

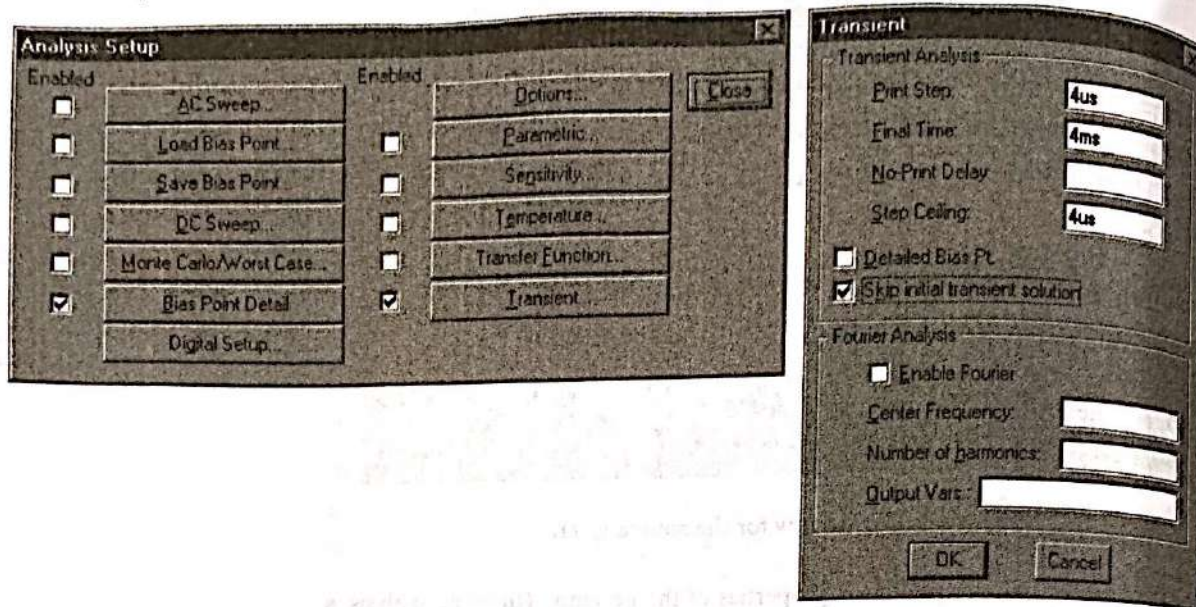


Figure 2.44 Analysis setup windows.

25 mA for the $\mu A741$.) Therefore, clipping occurs due to current limiting. Simulating the circuit and using Probe to examine the output voltage reveals clipping with a peak output voltage of $40 \text{ mA} \times R_L = 2 \text{ V}$.

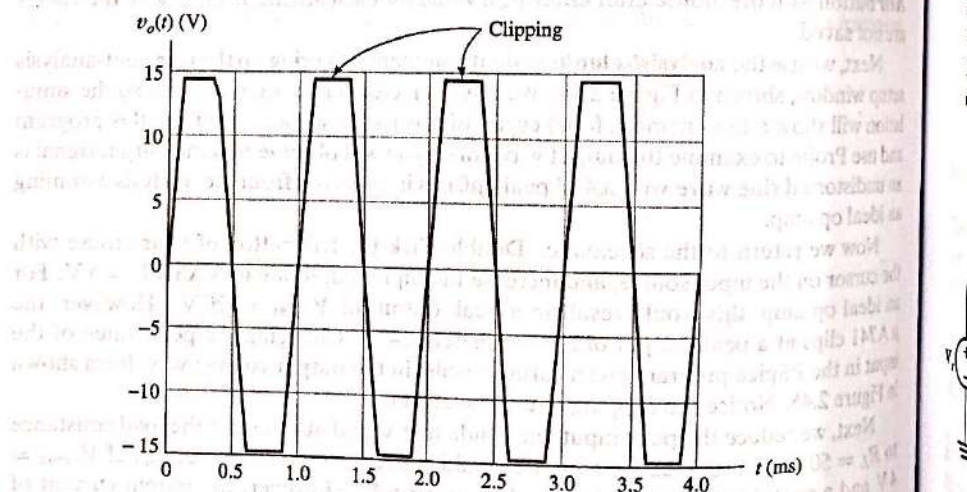


Figure 2.45 Output of the circuit of Figure 2.42 for $R_L = 10 \text{ k}\Omega$ and $V_{im} = 5 \text{ V}$.

EXERCISE

2.18 Show that the transfer function $A(f) = V_o/V_i$ of the macromodel illustrated in Figure 2.41(a) is given by Equation (2.24). Assume that the input source V_i is connected across the input terminals and that the load is an open circuit. Assume also that f_{BOL} is related to R_B and C_B by Equation (2.49).

EXERCISE

2.19 Draw a simple macromodel similar to Figure 2.41(a), including values of all circuit elements, for an op amp that has an input resistance of $10\text{ M}\Omega$, an output resistance of $100\ \Omega$, a dc voltage gain of 90 dB , and a gain-bandwidth product of 15 MHz . Assume that $R_B = 1\text{ k}\Omega$.

Answer The circuit diagram for the macromodel is shown in Figure 2.41(a). $R_{\text{in}} = 10\text{ M}\Omega$, $R_o = 100\ \Omega$, the product of the gains of the voltage-controlled sources must equal $A_{\text{OOL}} = 3.16 \times 10^4$, and $C_B = 0.336\ \mu\text{F}$.

EXERCISE

2.20 Use the op-amp model LF411LIN to obtain Bode plots of the voltage gain magnitude for the amplifiers shown in Figure 2.46. Find the 3-dB bandwidth of each amplifier. Compute the gain-bandwidth product for each circuit. Which circuit has the best performance with respect to this product? [Hint: In Schematics, cut the LF411LIN block from Figure 2.37 (stored in the file Fig2_37) and paste it into your circuits.]

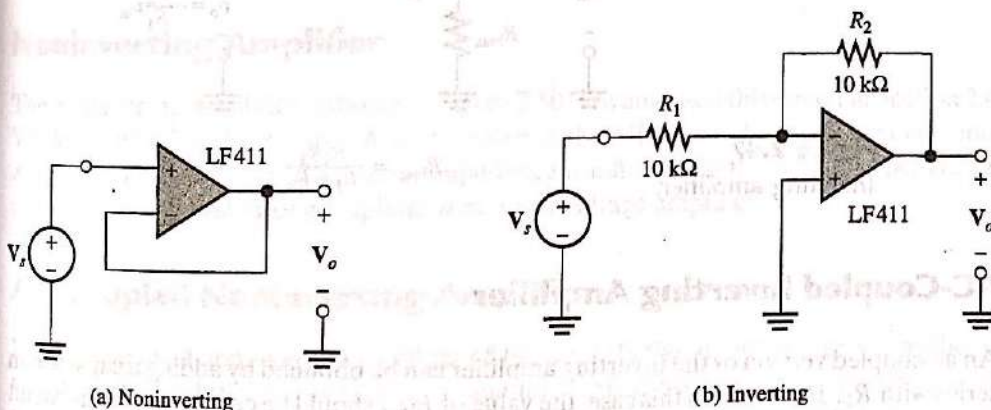


Figure 2.46 Unity-gain amplifiers.

Answer The circuit file can be found on the website. Its name is Exer2.20. (a) From the SPICE results, we find that $A_{0CL} = 1$, $f_{BCL} = 4$ MHz, and the gain-bandwidth product = 4 MHz. (b) $|A_{0CL}| = 1$, $f_{BCL} = 2$ MHz, and the gain-bandwidth product = 2 MHz. As we saw earlier, the noninverting circuit performs best with respect to the gain-bandwidth product.

2.10 A COLLECTION OF AMPLIFIER CIRCUITS

In this section, we present a collection of useful amplifier circuits that use op amps with resistive feedback networks. In many cases, properties of the circuits are stated without proof. However, the circuits can be analyzed using the summing-point constraint, as we have learned to do earlier in this chapter.

Inverting Amplifier

Refer to this section when you need ideas to start on a design problem.

We first met the inverting amplifier in Section 2.3. The circuit diagram of an improved version of the circuit is shown in Figure 2.47. The resistor R_{bias} is included so that the effects of bias current cancel, as discussed in Section 2.8. Assuming an ideal op amp, the input impedance of the circuit is equal to R_1 , and the output impedance is zero.

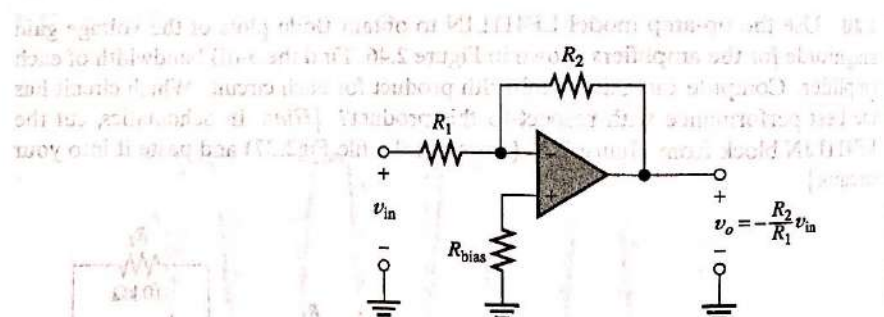


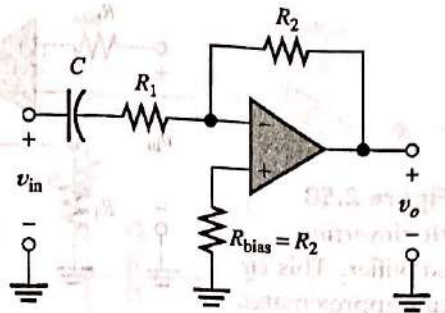
Figure 2.47
Inverting amplifier.

$$R_{bias} = \frac{R_1 R_2}{R_1 + R_2}$$

AC-Coupled Inverting Amplifier

An ac-coupled version of the inverting amplifier can be obtained by adding a capacitor in series with R_1 . However, in this case, the value of R_{bias} should be equal to R_2 . This circuit is shown in Figure 2.48. The circuit is useful if the input signal contains an unwanted dc component.

Figure 2.48
Ac-coupled invert-
ing amplifier.



The ac coupled inverter may be useful when the signal contains an unwanted dc component.

Summing Amplifier

The summing amplifier is illustrated in Figure 2.49. A simpler version of this circuit was analyzed, assuming an ideal op amp, in Exercise 2.1. Here the resistor R_{bias} is included to balance the effects of the input bias currents. Assuming an ideal op amp, the input impedance for the v_A source is R_A , and the input impedance for the v_B source is R_B . The output impedance is zero.

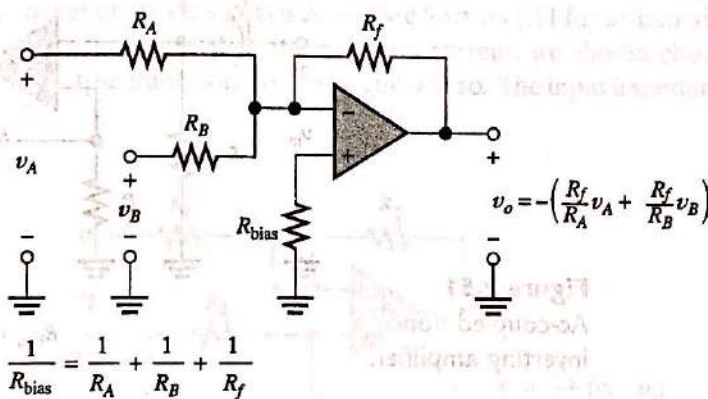


Figure 2.49
Summing amplifier.

Noninverting Amplifier

The noninverting amplifier is shown in Figure 2.50. We analyzed this circuit in Section 2.4. We have included the resistor R_{bias} to balance the effects of the input bias currents. Assuming an ideal op amp, the input impedance is infinite and the output impedance is zero. Thus, the noninverting amplifier is an ideal voltage amplifier.

AC-Coupled Noninverting Amplifier

In the dc-coupled noninverting amplifier of Figure 2.50, the input bias current of the op amp flows through the signal source. Sometimes this is not desirable. In other cases, the signal source can contain a large dc component that must be eliminated, so that the amplifier is not overdriven. Then the ac-coupled amplifier shown in Figure 2.51 is useful.

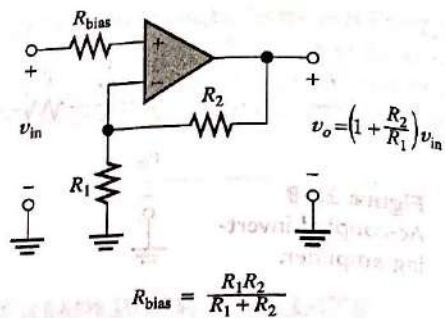


Figure 2.50
Noninverting
amplifier. This cir-
cuit approximates
an ideal voltage
amplifier.

It is important to notice that the resistor R_{bias} is required to provide a path for the dc-bias current. If R_{bias} is omitted, the bias current charges the coupling capacitor until the op amp is driven out of its active range. Assuming an ideal op amp and operation in the midband frequency range, the voltage gain is $1 + R_2/R_1$, the input impedance is R_{bias} , and the output impedance is zero.

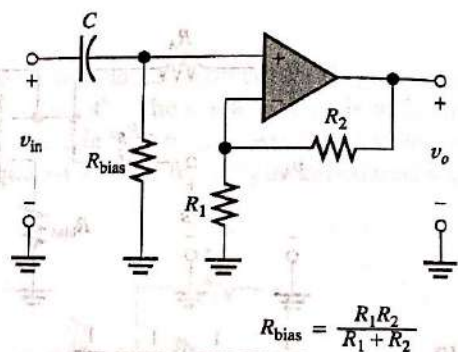


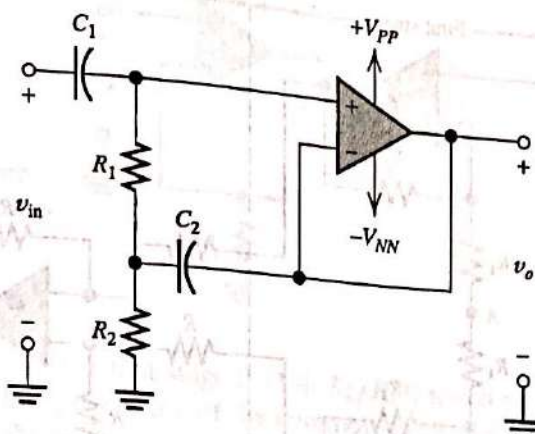
Figure 2.51
Ac-coupled non-
inverting amplifier.

Bootstrap AC-Coupled Voltage Follower

One of the disadvantages of the circuit shown in Figure 2.51 is that the ac input impedance is reduced (to R_{bias}) by the necessity to provide a dc path for the bias current. An ac-coupled voltage follower having much higher input impedance (infinite for an ideal op amp) is shown in Figure 2.52. For frequencies at which the capacitors appear as short circuits, the resistor R_1 appears to be connected from the input terminal to the output terminal of the amplifier. Notice that because the amplifier gain is unity, the output voltage equals the input voltage. Thus, there is zero signal voltage across R_1 . Accordingly, no signal current flows through R_1 , and the input impedance is very high.

The name *bootstrap* is used for the circuit because it reminded someone (the inventor, perhaps) of pulling oneself up by the bootstraps. Assuming that the capacitors are short circuits, the voltage at the bottom end of R_1 is "pulled up" to equal the input voltage of the amplifier.

Figure 2.52
Ac-coupled voltage follower with bootstrapped bias resistors.

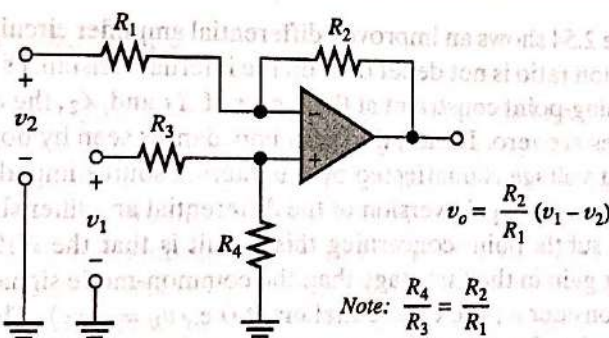


This bootstrap circuit achieves very high input impedance combined with ac coupling.

Differential Amplifier

Figure 2.53 shows a differential amplifier. Assuming an ideal op amp and letting $R_4/R_3 = R_2/R_1$, we find that the output voltage is a constant times the differential input signal ($v_1 - v_2$). The gain for the common-mode signal is zero. (See Section 1.11 for a discussion of common-mode signals.) To minimize the effects of bias current, we should choose $R_2 = R_4$ and $R_1 = R_3$. The output impedance of the circuit is zero. The input impedance for the v_1 source is $R_3 + R_4$.

Figure 2.53
Differential amplifier.



$$v_o = \frac{R_2}{R_1} (v_1 - v_2)$$

Note: $\frac{R_4}{R_3} = \frac{R_2}{R_1}$

A current that depends on v_1 flows back through the feedback network (R_1 and R_2) into the input source v_2 . Thus, as seen by the v_2 source, the circuit does not appear to be passive. Hence, the concept of input impedance does not apply for the v_2 source (unless v_1 is zero).

In some applications, the signal sources contain internal impedances, and the desired signal is the difference between the internal source voltages. Then we could design the circuit by including the internal source resistances of v_2 and v_1 as part of R_1 and R_3 , respectively. However, to obtain very high common-mode rejection, it is necessary to match closely the ratios of the resistances. This can be troublesome if the source impedances are not small enough to be neglected and are not predictable.

This circuit is very useful when the source contains a large unwanted common-mode component.

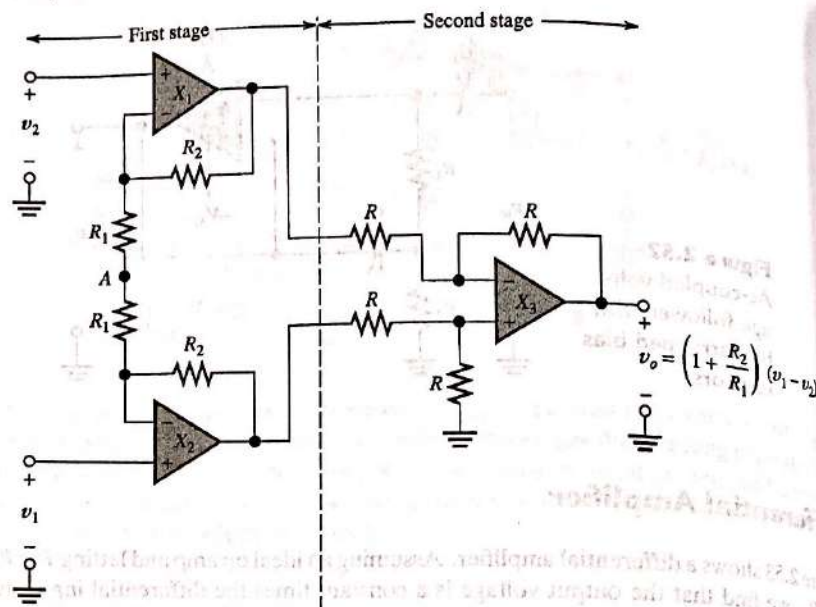


Figure 2.54 Instrumentation-quality differential amplifier.

Instrumentation-Quality Differential Amplifier

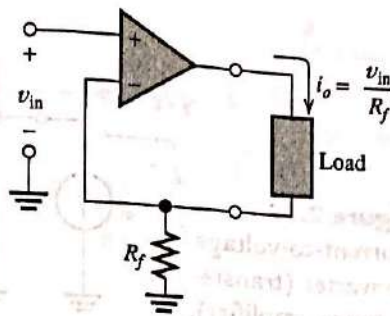
Figure 2.54 shows an improved differential amplifier circuit for which the common-mode rejection ratio is not dependent on the internal resistances of the sources. Because of the summing-point constraint at the inputs of X_1 and X_2 , the currents drawn from the signal sources are zero. Hence, the input impedances seen by both sources are infinite, and the output voltage is unaffected by the internal source impedances. Notice that the second stage is a unity-gain version of the differential amplifier shown in Figure 2.53.

A subtle point concerning this circuit is that the differential-mode signal incurs a higher gain in the first stage than the common-mode signal does. To illustrate this point, first consider a pure differential input (i.e., $v_1 = -v_2$). Then, because the circuit is symmetrical, point A remains at zero voltage. Hence, in the analysis for a purely differential input signal, point A can be considered to be grounded. In this case, the input amplifiers X_1 and X_2 are configured as noninverting amplifiers having gains of $(1 + R_2/R_1)$. The differential gain of the second stage is unity. Thus, the overall gain for the differential signal is $(1 + R_2/R_1)$.

Now consider a pure common-mode signal (i.e., $v_1 = v_2 = v_{cm}$). Because of the summing-point constraint, the voltages between the input terminals of X_1 or X_2 are zero. Therefore, the voltages at the inverting input terminals of X_1 and X_2 are both equal to v_{cm} . Hence, the voltage across the series-connected R_1 resistors is zero, and no current flows through them. Consequently, no current flows through the R_2 resistors. Thus, the output voltages of X_1 and X_2 are equal to v_{cm} , and we have shown that the first-stage gain is unity for the common-mode signal.

...the differential-mode signal incurs a higher gain in the first stage than the common-mode signal does.

Figure 2.55
Voltage-to-current
converter (transcon-
ductance ampli-
fier).



However, the differential gain of the first stage is $(1 + R_2/R_1)$, which can be much larger than unity, thereby achieving a reduction of the common-mode signal amplitude relative to the differential signal. (Notice that if point A were actually grounded, the gain for the common-mode signal would be the same as for the differential signal.)

In practice, the series combination of the two R_1 resistors is implemented by a single resistor because it is not necessary to have access to point A. Thus, matching of component values for R_1 is not required. Furthermore, close matching of the R_2 resistors is not required to achieve a higher differential gain than the common-mode gain in the first stage. Because the first stage reduces the relative amplitude of the common-mode signal, matching of the resistors in the second stage is not as critical.

While it is more complex, the differential amplifier of Figure 2.54 performs better than that of Figure 2.53. Specifically, the common-mode rejection ratio is independent of the internal source resistances, the input impedance seen by both sources is infinite, and resistor matching is not as critical.

While it is more complex, the differential amplifier of Figure 2.54 performs better than that of Figure 2.53.

Voltage-to-Current Converters

A circuit that forces a current through the load that is proportional to the input voltage is shown in Figure 2.55. In this circuit, the load is said to be *floating*, because neither end is connected to ground. Assuming an ideal op amp, the input impedance and output impedance are infinite. In other words, the circuit is an ideal transconductance amplifier.

Often, the load must have one end connected to ground. Then the **Howland circuit** shown in Figure 2.56 is useful. A drawback of this circuit is that the resistor ratios must be carefully matched for the load current to be independent of the load impedance.

Figure 2.56
Voltage-to-current
converter with
grounded load
(Howland circuit).

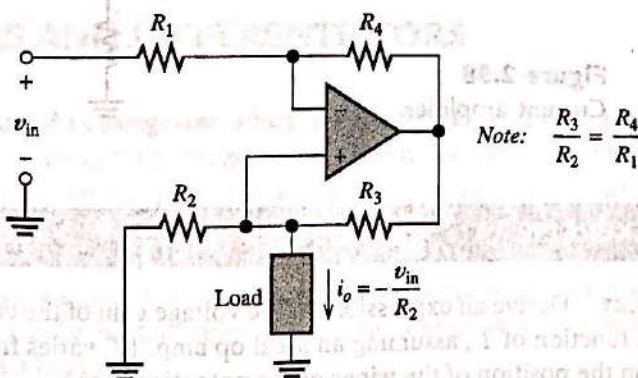
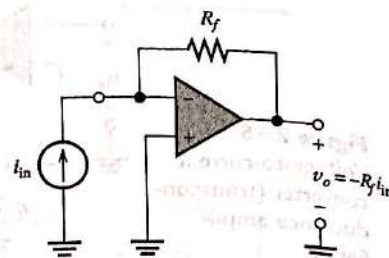


Figure 2.57
Current-to-voltage
converter (transre-
sistance amplifier).



Assuming an ideal op amp and matched resistors, the circuit has infinite output impedance. However, the input impedance is finite and depends on the load impedance.

Current-to-Voltage Converter

A circuit that produces an output voltage proportional to the input current is illustrated in Figure 2.57. Because of the summing-point constraint, the voltage across the input source is forced to zero. Therefore, the input impedance of the circuit is zero. Furthermore, the output voltage is independent of the load. Thus, the output impedance is zero. With an ideal op amp, the circuit is an ideal transresistance amplifier.

Current Amplifiers

The circuit shown in Figure 2.58 has the characteristics of an ideal current amplifier: zero input impedance and infinite output impedance. Notice that the load is floating. A current amplifier having a grounded load can be obtained by cascading a current-to-voltage converter with the Howland circuit of Figure 2.56.

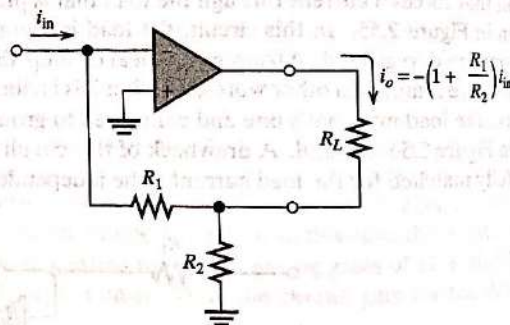
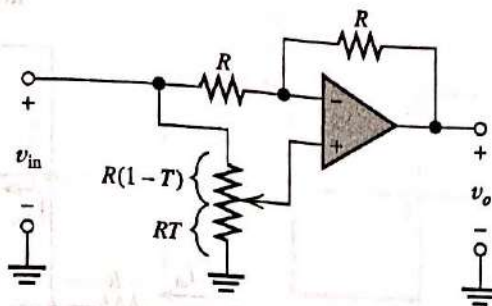


Figure 2.58
Current amplifier.

EXERCISE

2.21 Derive an expression for the voltage gain of the circuit shown in Figure 2.59 as a function of T , assuming an ideal op amp. (T varies from zero to unity, depending on the position of the wiper of the potentiometer.)

Figure 2.59
Variable-gain amplifier. See Exercise 2.21.



This is a nice trick to know about when the application calls for gain that can be varied through zero.

Answer $A_v = 2T - 1$. Notice that the gain varies from -1 through 0 to $+1$ as the potentiometer is rotated.

EXERCISE

2.22 Assume an ideal op amp, and use the summing-point constraint to verify the expression for the output current in the voltage-to-current converter of Figure 2.55. Also, find the input and output resistances of the circuit.

Answer $R_{in} = \infty$, $R_o = \infty$.

EXERCISE

2.23 Repeat Exercise 2.22 for the Howland circuit shown in Figure 2.56. In finding the input resistance, assume that the load is a resistance R_L .

Answer $R_{in} = (R_1 R_2) / (R_2 + R_L)$, $R_o = \infty$.

2.11 INTEGRATORS AND DIFFERENTIATORS

Figure 2.60 shows the diagram of an **integrator**, which is a circuit that produces an output voltage proportional to the running time integral of the input voltage. The integrator circuit is often useful in instrumentation applications. For example, consider a signal from an accelerometer that is proportional to the acceleration of a piston in an automobile engine. By integrating the acceleration signal, we obtain a signal proportional to the velocity of the piston. Another integration yields a signal proportional to the position of the piston. These signals can be used to study the design of engines or to control an automobile's ignition and fuel injection.

The integrator is useful in control systems and waveshapers.

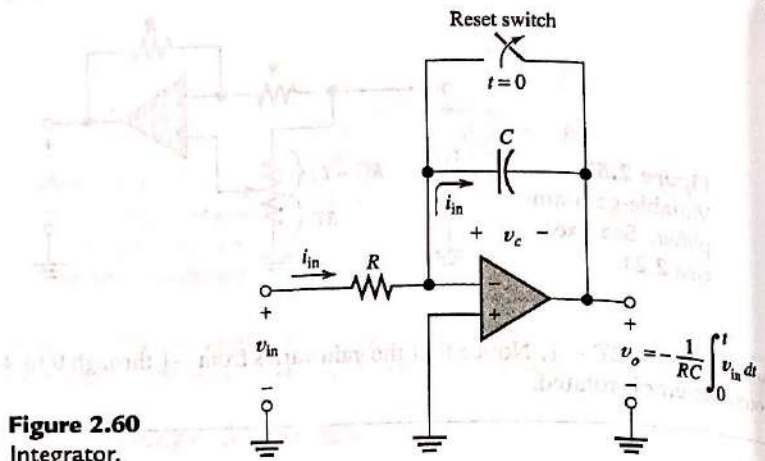


Figure 2.60 Integrator.

In Figure 2.60, negative feedback occurs through the capacitor. Thus, assuming an ideal op amp, the voltage at the inverting op-amp input is zero. The input current is given by

$$i_{in}(t) = \frac{v_{in}(t)}{R} \quad (2.50)$$

The current flowing into the input terminal of the (ideal) op amp is zero. Therefore, the input current i_{in} flows through the capacitor. We assume that the reset switch is opened at $t = 0$. Hence, the capacitor voltage is zero at $t = 0$. The voltage across the capacitor is

$$v_c(t) = \frac{1}{C} \int_0^t i_{in}(x) dx \quad (2.51)$$

in which x is a "dummy" variable of integration.

Writing a voltage equation from the output terminal across the capacitor and then to ground across the op-amp input terminals, we obtain

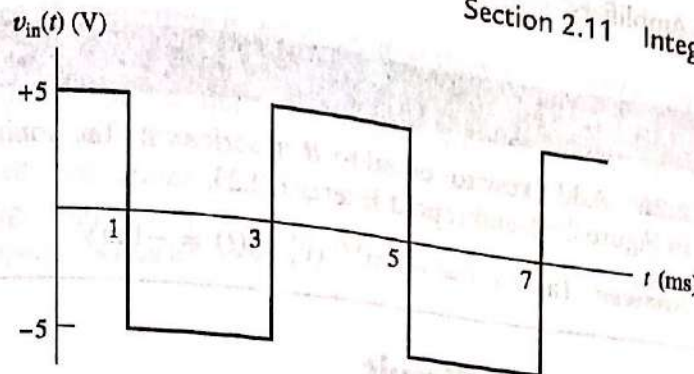
$$v_o(t) = -v_c(t) \quad (2.52)$$

Using Equation (2.50) to substitute for i_{in} in Equation 2.51 and the result to substitute for $v_c(t)$ in Equation (2.52), we have

$$v_o(t) = -\frac{1}{RC} \int_0^t v_{in}(x) dx \quad (2.53)$$

Thus, the output voltage is $-1/RC$ times the running integral of the input voltage. (The term *running integral* implies that the upper limit of integration is the time variable.) If an integrator with a positive gain constant is desired, we can cascade the integrator with an inverting amplifier. The magnitude of the gain constant can be adjusted by the choice of R and C .

Figure 2.61
Square-wave
input signal for
Exercise 2.24.



Of course, in selecting a capacitor, we always want to use as small a value as possible to minimize cost, volume, and mass. However, for a given gain constant $1/RC$, smaller C leads to larger R and smaller values of i_{in} . Therefore, the bias current of the op amp becomes more significant as the capacitance becomes smaller. As usual, we try to design for the best compromise.

EXERCISE

2.24 Consider the integrator of Figure 2.60 with the square-wave input signal shown in Figure 2.61. (a) If $R = 10\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$, and the op amp is ideal, sketch the output waveform to scale. (b) If $R = 10\text{ k}\Omega$, what value of C is required for the peak-to-peak output amplitude to be 2 V ?

Answer (a) See Figure 2.62; (b) $C = 0.5\text{ }\mu\text{F}$.

This exercise illustrates a wave shaping application of the integrator.

EXERCISE

2.25 Consider the circuit of Figure 2.60 with $v_{in} = 0$, $R = 10\text{ k}\Omega$, and $C = 0.01\text{ }\mu\text{F}$. As indicated in the figure, the reset switch opens at $t = 0$. The op amp is ideal, except for a bias current of $I_B = 100\text{ nA}$. [Assume that the bias currents flow into (rather than out of) the op-amp input terminals.] (a) Find an expression for the output voltage of the circuit as a function of time. (b) Repeat for $C = 1\text{ }\mu\text{F}$.

Answer (a) $v_o(t) = 10t$; (b) $v_o(t) = 0.1t$.

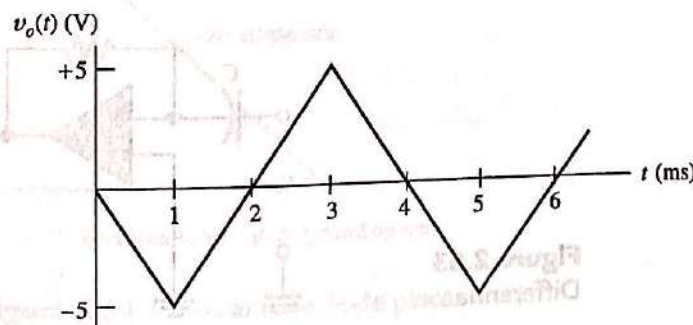


Figure 2.62
Answer for Exer-
cise 2.24a.

EXERCISE

2.26 Add a resistor equal to R in series with the noninverting input of the op amp in Figure 2.60, and repeat Exercise 2.25.

Answer (a) $v_o(t) = -1 \text{ mV}$; (b) $v_o(t) = -1 \text{ mV}$.

Differentiator Circuit

Figure 2.63 shows a **differentiator** which produces an output voltage proportional to the time derivative of the input voltage. By an analysis similar to that used for the integrator, we can show that the circuit produces an output voltage given by

$$v_o(t) = -RC \frac{dv_{in}}{dt} \quad (2.54)$$

EXERCISE

2.27 Derive Equation (2.54).

Frequency Response

If we consider a sinusoidal steady-state analysis of the integrator circuit, we find that the transfer function is given by

$$\frac{V_o}{V_{in}}(f) = -\frac{1}{j2\pi f RC} \quad (2.55)$$

For the differentiator, the transfer function is

$$\frac{V_o}{V_{in}}(f) = -j2\pi f RC \quad (2.56)$$

Bode plots of the magnitude of the transfer functions of the integrator and of the differentiator are illustrated in Figures 2.64a and b, respectively. Notice that the gain of the integrator crosses 0 dB at $f = 1/(2\pi RC)$ and has a slope of -20 dB/decade . The differentiator gain also crosses 0 dB at $f = 1/(2\pi RC)$, but displays a $+20 \text{ dB/decade}$ slope. Also shown, in Figure 2.64c, is the open-loop voltage gain of a typical op amp.

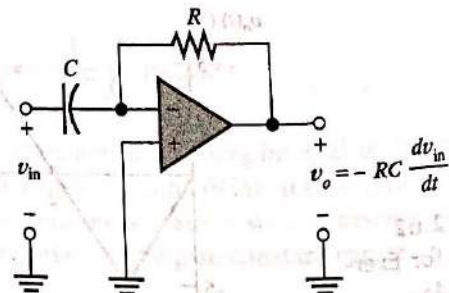


Figure 2.63
Differentiator.

Usually, the performance of integrators is closer to ideal than is the performance of differentiators, because the gain of the ideal integrator becomes low at higher frequencies, for which the open-loop gain of the op amp declines. On the other hand, the ideal differentiator has high gain at high frequencies, but that is not possible for real op amps. In other words, the bandwidth limitations of the op amp cause the gain of both circuits to be lower than ideal at high frequencies. Because the gain of the integrator is low at high frequencies, the discrepancy is less noticeable.

...the performance of integrators is closer to ideal than is the performance of differentiators.

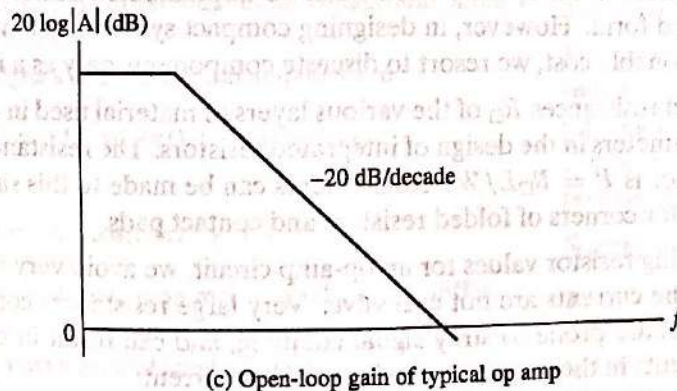
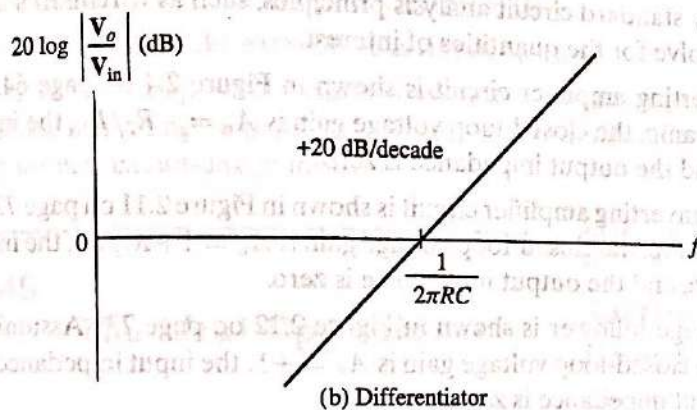
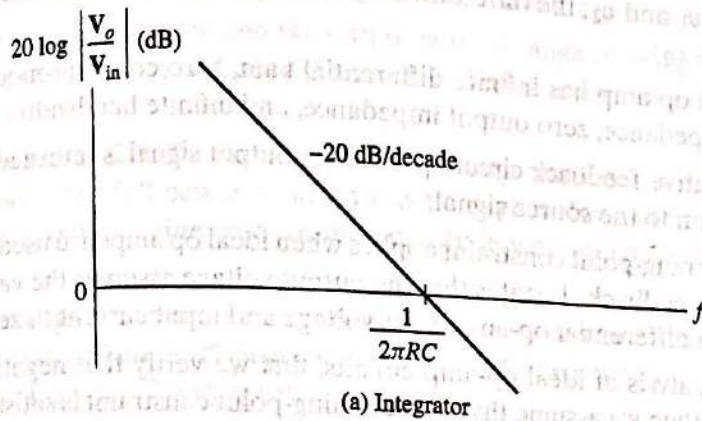


Figure 2.64 Comparative Bode plots.

The differentiator has high gain at high frequencies, which tends to accentuate high-frequency noise.

Another reason for avoiding differentiators is that high-frequency noise is often contained in the input signal. The differentiator has high gain at high frequencies, which tends to accentuate the noise.

SUMMARY

- A differential amplifier has two input terminals. If the input voltages to the terminals are v_1 and v_2 , the differential signal is $v_1 - v_2$, and the common-mode signal is $\frac{1}{2}(v_1 + v_2)$.
- An ideal op amp has infinite differential gain, zero common-mode gain, infinite input impedance, zero output impedance, and infinite bandwidth.
- In a negative-feedback circuit, part of the output signal is returned to the input in opposition to the source signal.
- The summing-point constraint applies when ideal op amps are used in circuits with negative feedback. It states that the output voltage assumes the value required to drive the differential op-amp input voltage and input current to zero.
- In the analysis of ideal op-amp circuits, first we verify that negative feedback is present, then we assume that the summing-point constraint is satisfied, and finally we apply standard circuit analysis principles, such as Kirchhoff's laws and Ohm's law, to solve for the quantities of interest.
- The inverting amplifier circuit is shown in Figure 2.4 on page 64. Assuming an ideal op amp, the closed-loop voltage gain is $A_v = -R_2/R_1$, the input impedance is R_1 , and the output impedance is zero.
- The noninverting amplifier circuit is shown in Figure 2.11 on page 72. Assuming an ideal op amp, the closed-loop voltage gain is $A_v = 1 + R_2/R_1$, the input impedance is infinite, and the output impedance is zero.
- The voltage follower is shown in Figure 2.12 on page 73. Assuming an ideal op amp, the closed-loop voltage gain is $A_v = +1$, the input impedance is infinite, and the output impedance is zero.
- The resistors in an op-amp circuit can be implemented either in discrete or in integrated form. However, in designing compact systems with high functionality and reasonable cost, we resort to discrete components only as a last resort.
- The sheet resistances $R_{\square}$ of the various layers of material used in an IC are important parameters in the design of integrated resistors. The resistance of a rectangular resistor is $R = R_{\square}L/W$. Refinements can be made to this simple formula to account for corners of folded resistors and contact pads.
- In choosing resistor values for an op-amp circuit, we avoid very small resistance so that the currents are not excessive. Very large resistances consume excessive chip area, are prone to stray signal coupling, and can result in objectionable components in the output due to input offset current.
- Real op amps have finite input impedance, nonzero output impedance, finite open-loop dc gain, and finite bandwidth.

- The open-loop frequency response of general-purpose op amps is limited to avoid instability. Such op amps often have a dominant pole.
- The closed-loop bandwidth of either the inverting amplifier or the noninverting amplifier is given by $f_{BCL} = f_t / (1 + R_2/R_1)$. For the same gain magnitude, noninverting amplifiers have wider bandwidth than inverting amplifiers.
- For the noninverting amplifier, the product of the closed-loop dc gain and the bandwidth is constant. Thus, an important parameter of a real op amp is its gain-bandwidth product, which is also called the unity-gain bandwidth. General-purpose op amps have unity gain bandwidths of a few megahertz.
- The output voltage range and the output current range of an op amp are limited. The output waveform is clipped if it reaches (and tends to exceed) either of these limits.
- The slew-rate limit is the maximum rate of change possible for the output voltage magnitude. The full-power bandwidth is the highest frequency for which the op amp can produce a sine wave of full amplitude without exceeding the slew-rate limit.
- Real op amps suffer from dc imperfections known as input offset voltage, input bias current, and input offset current. These effects can be modeled by the sources shown in Figure 2.33 on page 95.
- SPICE is a useful tool in the design of electronic circuits.
- Macromodels simulate the external behavior of op amps.
- Many practical op-amp circuits can be designed. A small collection is discussed in Section 2.10 starting on page 108. Expert circuit designers are always on the lookout for new circuit-design ideas.

PROBLEMS

Section 2.1: The Ideal Operational Amplifier

- 2.1. A differential amplifier has input voltages v_1 and v_2 . Give the definitions of the differential input voltage and of the common-mode input voltage.
- 2.2. The input signals to a differential amplifier are

$$v_1(t) = 0.1 \cos(20\pi t) + 20 \sin(120\pi t)$$

and

$$v_2(t) = -0.1 \cos(20\pi t) + 20 \sin(120\pi t)$$

Find expressions for the common-mode signal and the differential signal.

- 2.3. List the characteristics of ideal op amps.
- 2.4. Assuming that two pins are needed for power-supply connections, what is the practical limit on the number of op

amps in a 14-pin package? Assume that we need to be able to access the input and output terminals of all op amps.

Section 2.2: The Summing-Point Constraint

- 2.5. Define the term *summing-point constraint*. Does it apply if positive feedback is present?
- 2.6. List the steps in the analysis of an ideal op-amp circuit.
- 2.7. List and briefly discuss one or two situations in which negative feedback is useful in daily life or in mechanical systems.
- 2.8. In a positive-feedback situation, signals can grow larger and larger. List and briefly discuss one or two examples of positive feedback in areas other than electronic circuits.

Section 2.3: The Inverting Amplifier

- 2.9. Draw the circuit diagram of the basic inverting-amplifier configuration. Give an expression for the voltage gain of the circuit in terms of the resistors, assuming an ideal op amp. Give expressions for the input impedance and output impedance of the circuit.

2.10. Each of the circuits shown in Figure P2.10 employs negative feedback. Assume that the op amps are ideal, and use the summing-point constraint. Analyze the circuits to find the value of v_o for each circuit.

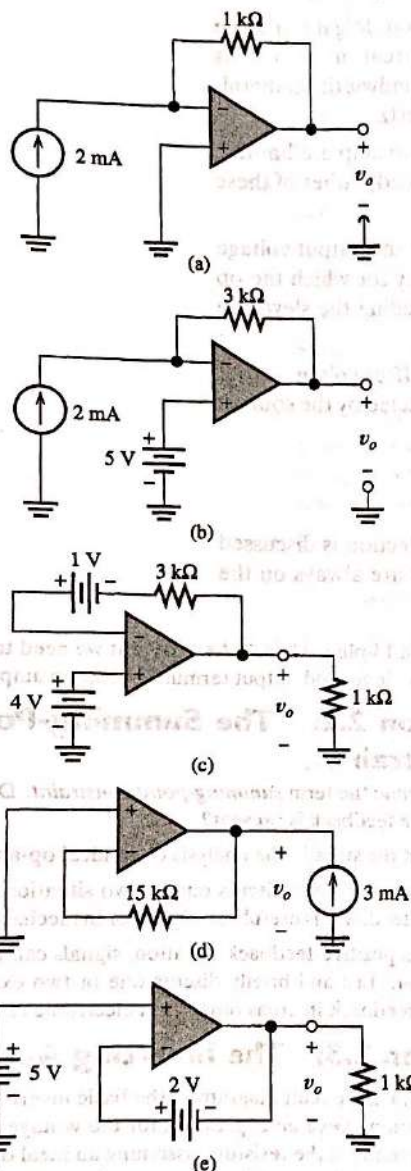


Figure P2.10

2.11. A certain op amp has an open-loop gain of $A_{OL} = 10^4$. The op amp is used in an inverting amplifier as illustrated in Figure 2.4 with $R_2 = 10 \text{ k}\Omega$ and $R_1 = 1 \text{ k}\Omega$. The output voltage lies in the range from -12 V to $+12 \text{ V}$. What is the range of v_x ? What is the approximate range of v_{in} (assuming an ideal op amp)? Is v_x negligible compared with v_{in} ? Is the summing-point constraint assumption justified in this case?

2.12. In this problem, we investigate a subject known as the **Miller effect**. Consider the situation shown in Figure P2.12 in which an impedance Z_f is connected between the input of an amplifier and the output terminal. (a) Show that the input impedance is $Z_{in} = Z_f / (1 - A_v)$. (b) Suppose that the input and $A_v = -10^5$. Compute the value of Z_{in} . (c) Suppose that $Z_f = 10 \text{ k}\Omega$ and $A_v = +2$. Comment. (d) Suppose that Z_f consists of a 1-pF capacitance and that $A_v = -100$. What equivalent capacitance is seen looking into the input terminals?

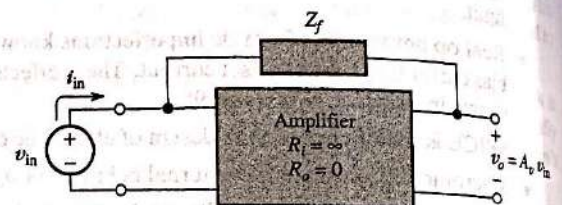


Figure P2.12

2.13. Derive an expression for the input impedance of the inverting amplifier, assuming a finite value of A_{OL} . Assume that the input impedance of the op amp is infinite and that the output impedance of the op amp is zero. Evaluate the expression you came up with for $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, and $A_{OL} = 10^4$. What is the input impedance, assuming infinite A_{OL} ? Compute the percentage difference between the two answers.

2.14. Determine the closed-loop voltage gain of the circuit shown in Figure P2.14, assuming an ideal op amp. All of the resistors are equal in value.

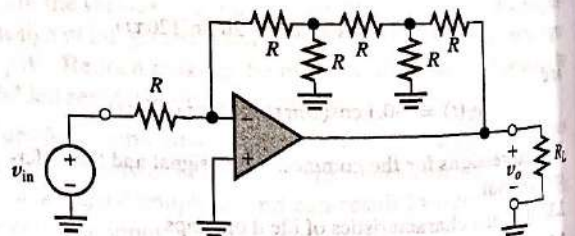


Figure P2.14

2.15. Suppose that the resistors R_1 and R_2 used in an inverting amplifier have tolerances of $\pm 1\%$. What is the tolerance of the gain?

2.16. Use the equivalent circuit of the op amp shown in Figure 2.2 to derive an expression for the closed-loop voltage gain of the inverter illustrated in Figure 2.4. Evaluate your expression for $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, and $A_{OL} = 10^4$. Repeat for $A_{OL} = 10^5$ and in the limit as A_{OL} approaches infinity.

2.17. Draw the circuit diagram of an inverting amplifier with $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$, and $v_{in} = 1 \text{ V}$. Show the current in each branch of the circuit and explain how Kirchhoff's current law is satisfied.

2.18. The circuit shown in Figure P2.18 employs negative feedback. Use the summing-point constraint (for both op amps) to derive expressions for the voltage gains $A_1 = v_{o1}/v_{in}$ and $A_2 = v_{o2}/v_{in}$.

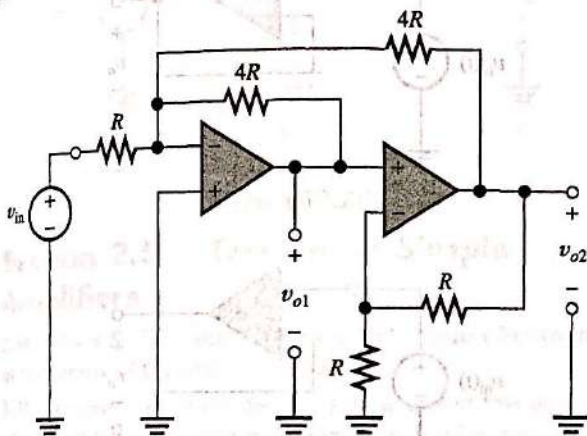


Figure P2.18

Section 2.4: The Noninverting Amplifier

2.19. Draw the circuit diagram of the noninverting-amplifier. Give an expression for the voltage gain of the circuit in terms of the resistances, assuming an ideal op amp. Give expressions for the input impedance and output impedance of the circuit.

2.20. What is a voltage follower? Draw the circuit diagram.

2.21. How can an amplifier like the voltage follower be useful? Why not just connect the source to the load, thereby achieving a voltage gain of unity without the need for an op amp?

2.22. Analyze the ideal op-amp circuit shown in Figure P2.22 to find an expression for v_o in terms of v_A , v_B , and the resistor values.

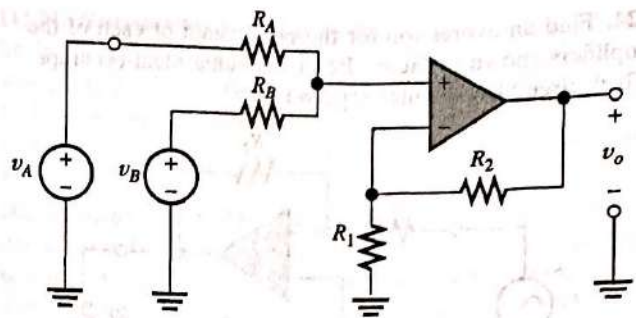
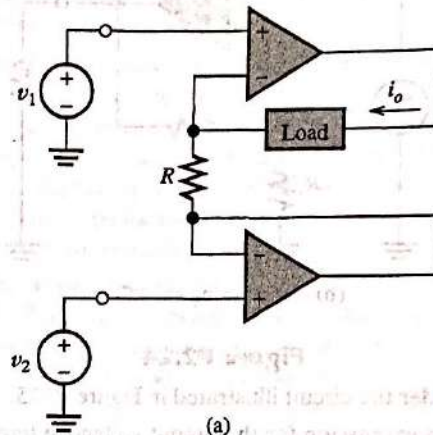
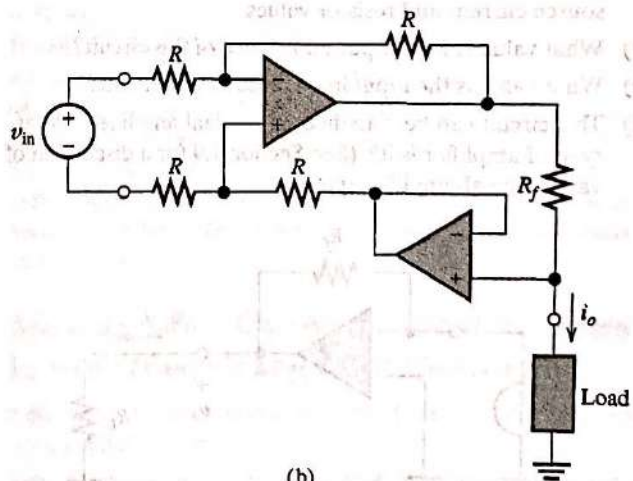


Figure P2.22

2.23. Analyze each of the ideal op-amp circuits shown in Figure P2.23 to find expressions for i_o . What is the value of the output resistance (seen by the load) for each of these circuits? Why?



(a)



(b)

Figure P2.23 Voltage-to-current converter circuits.

2.24. Find an expression for the power gain of each of the amplifiers shown in Figure P2.24. Assume ideal op amps. Which circuit has the higher power gain?

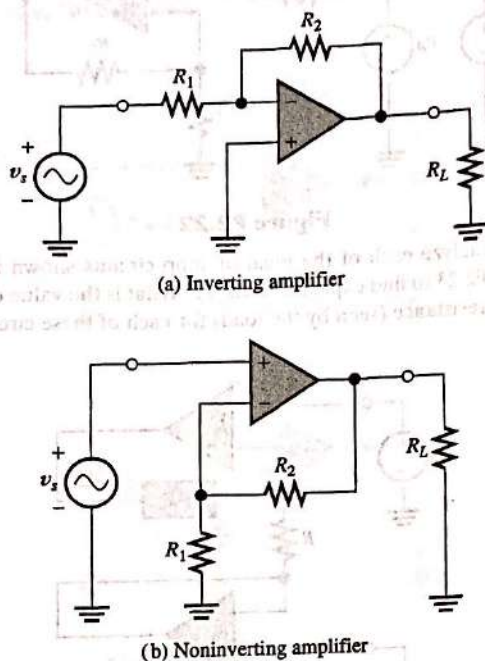


Figure P2.24

- 2.25. Consider the circuit illustrated in Figure P2.25.
- Find an expression for the output voltage in terms of the source current and resistor values.
 - What value is the output impedance of this circuit?
 - What value is the input impedance of this circuit?
 - This circuit can be classified as an ideal amplifier. What type of amplifier is it? (See Section 1.9 for a discussion of various ideal-amplifier types.)

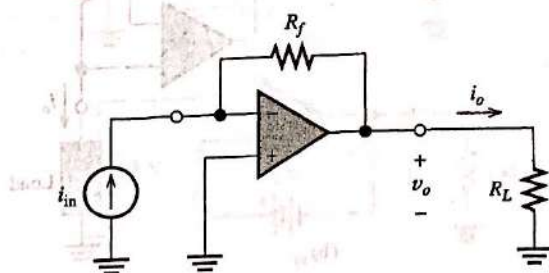


Figure P2.25

2.26. Suppose that we design an inverting amplifier using 5% tolerance resistors and an ideal op amp. The nominal amplifier gain is -2 . What is the minimum and maximum gain that is possible, assuming that the resistor values are within the stated tolerance? What is the percentage tolerance of the gain?

2.27. Repeat Problem 2.26 for a noninverting amplifier having a nominal voltage gain of $+2$.

2.28. Consider the circuits shown in Figures P2.28a and b. One of the circuits has negative feedback and the other has positive feedback. Assume that the op amps are ideal, except that the output voltage is limited to extremes of ± 5 V. For the input voltage waveform shown in Figure P2.28c, plot the output voltage $v_o(t)$ to scale against time. You may wish to use SPICE (see Section 2.9) to verify your answers.

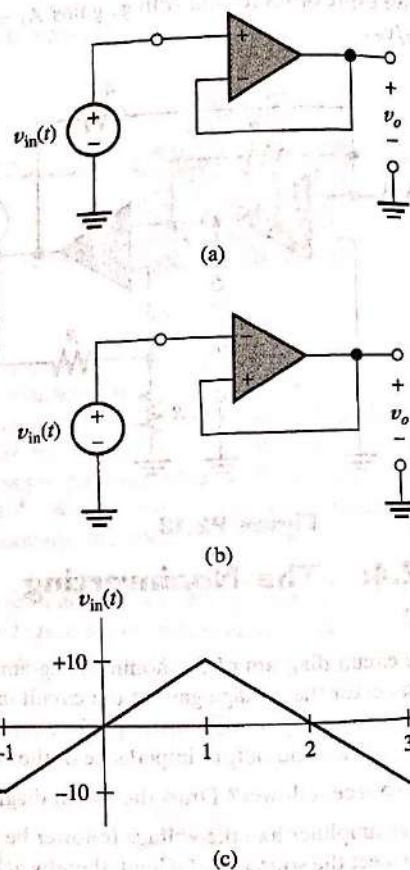


Figure P2.28

2.29. Repeat Problem 2.28 for the circuits of Figures P2.29a and b. (The input voltage waveform is shown in Figure P2.28c.)

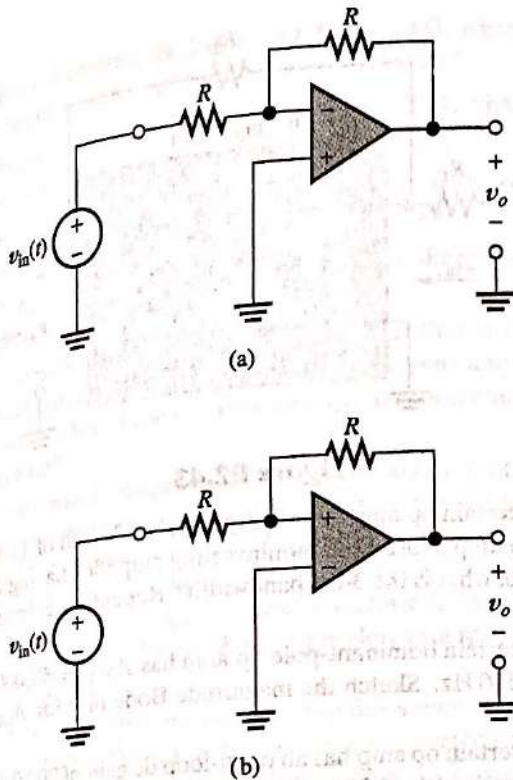


Figure P2.29

Section 2.5: Design of Simple Amplifiers

2.30. Why is $R_{\square}$ for resistors in integrated circuits often outside of the control of the circuit designer?

2.31. Suppose that we are designing an amplifier that uses an op amp. What problems are associated with using very small feedback resistances? With very large feedback resistances?

2.32. Suppose that $R_{\square} = 200 \Omega/\square$ for a certain film. Find the new value of $R_{\square}$ if the thickness of the film is doubled. Justify your answer.

D2.33. Film-resistor design. Design a $10\text{-k}\Omega$ resistor similar to Figure 2.19. (That is, draw the layout of the resistor, showing its dimensions.) The material has $R_{\square} = 200 \Omega/\square$. Use dog-bone contact pads (counting for 0.65 of a square each). Count corners as 0.56 of a square each. Lay out the resistor so that the region it occupies is approximately square. The minimum width of the resistor is $W = 10 \mu\text{m}$, and the minimum spacing between sides of the resistor is $W_{\text{space}} = 5 \mu\text{m}$. Strive for minimum area. 1. Choose the minimum width to reduce the area consumed. 2. Determine the total length required. 3. Determine the area consumed by the resistor including the guard strips. 4. Fold the resistor to fit into an approximately square region. 5. Compute the resistance of your layout and adjust one of its dimensions to achieve $10 \text{ k}\Omega$ exactly.

D2.34. Noninverting amplifier design. Design an amplifier having a nominal input impedance of $10 \text{ k}\Omega$ and a nominal voltage gain of $+10$. Use 5%-tolerance discrete resistors. 1. Design a noninverting amplifier with a gain of ten. 2. Place a $10\text{-k}\Omega$ resistor in parallel with the input terminals to achieve the desired input impedance.

D2.35. Inverting amplifier design. Design an amplifier with one op amp having a nominal gain of -100 . Use no resistors smaller than $1 \text{ k}\Omega$. Strive to minimize the total resistance used. Consider the circuit configuration shown in Figure 2.6.

D2.36. Design for minimum chip area. Suppose that an op amp consumes a chip area equivalent to a $10\text{-k}\Omega$ resistor. Design an amplifier having a gain magnitude of 100. Use no resistances smaller than $1 \text{ k}\Omega$. Strive for minimum chip area. Multiple op amps are allowed. Assume that the area consumed by a resistor is proportional to its resistance. One approach is to cascade several noninverting amplifier stages. Another approach is to use the circuit of Figure 2.15 which was analyzed in Exercise 2.6.

D2.37. Modified summing amplifier design. Design a circuit for which the output voltage is $v_o = A_1 v_1 + A_2 v_2$. The voltages v_1 and v_2 are input voltages. Design the circuit to achieve $A_1 = 5$ and $A_2 = -10$. Use 5%-tolerance discrete resistors. There is no restriction on input impedances. One approach is to use the circuit configuration of Figure 2.23. Another approach is to modify the differential amplifier of Figure 2.53.

D2.38. Modified summing amplifier design. Repeat Problem D2.37 if the input impedances are required to be as large as possible (ideally, open circuits). An easy approach is to add voltage followers at the inputs of the circuit designed for Problem 2.37. However, another approach is to use two op amps. To achieve high input impedances, we should apply the input signals to the noninverting input terminals.

D2.39. High input impedance inverter design. A certain signal source has an internal resistance that fluctuates between limits of $1 \text{ k}\Omega$ and $1 \text{ M}\Omega$. Design an amplifier that produces an amplified version of the internal source voltage. Use standard 5%-tolerance discrete resistors. The voltage gain should be -20 with a tolerance of $\pm 15\%$ or better. Very high input impedance is needed. Consider a voltage follower or noninverting amplifier cascaded with an inverter.

Section 2.6: Op-Amp Imperfections in the Linear Range of Operation

2.40. List the imperfections of a real op amp in the linear range of operation.

2.41. Consider the noninverting-amplifier configuration for an op amp having a dominant pole. How are the dc gain and bandwidth related?

2.42. The objective of this problem is to investigate the effects of finite gain, finite input impedance, and nonzero output impedance of the op amp on the voltage follower. Consider the circuit, including the op-amp model, shown in Figure P2.42.

- Derive an expression for the circuit voltage gain v_o/v_s . Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, and $R_o = 25\ \Omega$. Compare this result with the circuit gain assuming an ideal op amp.
- Derive an expression for the circuit input impedance $Z_{in} = v_s/i_s$. Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, and $R_o = 25\ \Omega$. Compare this result to the input impedance with an ideal op amp.
- Derive an expression for the circuit output impedance Z_o . Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, and $R_o = 25\ \Omega$. Compare this result with the output impedance of the circuit assuming an ideal op amp.

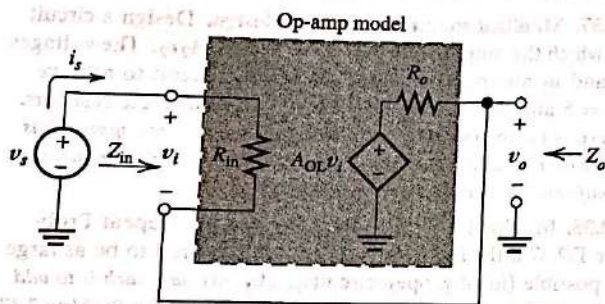


Figure P2.42

2.43. The objective of this problem is to investigate the effects of finite gain, finite input impedance, and nonzero output impedance of the op amp on the inverting amplifier. Consider the circuit, including the op-amp model, shown in Figure P2.43.

- Derive an expression for the circuit voltage gain v_o/v_s . Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, $R_o = 25\ \Omega$, $R_1 = 1\text{ k}\Omega$, and $R_2 = 10\text{ k}\Omega$. Compare this result to the gain with an ideal op amp.
- Derive an expression for the circuit input impedance $Z_{in} = v_s/i_s$. Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, $R_o = 25\ \Omega$, $R_1 = 1\text{ k}\Omega$, and $R_2 = 10\text{ k}\Omega$. Compare this result with the input impedance for an ideal op amp.
- Derive an expression for the circuit output impedance Z_o . Evaluate your expression for $A_{OL} = 10^5$, $R_{in} = 1\text{ M}\Omega$, $R_o = 25\ \Omega$, $R_1 = 1\text{ k}\Omega$, and $R_2 = 10\text{ k}\Omega$. Compare this result with the output impedance with an ideal op amp.

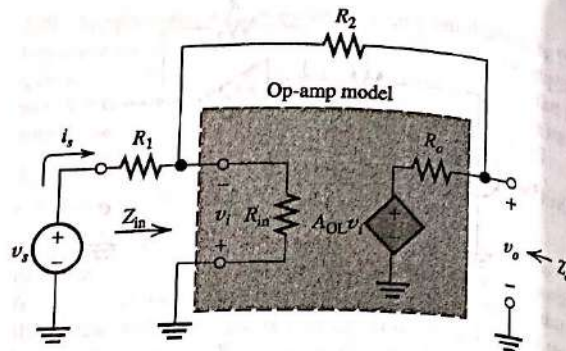


Figure P2.43

2.44. A certain op amp has a unity-gain bandwidth of 15 MHz. If this op amp is used in a noninverting amplifier having a dc gain of 10, what is the 3-dB bandwidth? Repeat for a dc gain of 100.

2.45. A certain dominant-pole op amp has $A_{OL} = 50,000$ and $f_{BOL} = 100\text{ Hz}$. Sketch the magnitude Bode plot for A_{OL} to scale.

2.46. A certain op amp has an open-loop dc gain of 200,000 and a 3-dB bandwidth of 5 Hz. Find the magnitude and phase of the open-loop gain at a frequency of (a) 100 Hz, (b) 1000 Hz, and (c) 1 MHz.

2.47. Consider two alternatives for designing an amplifier having a dc gain of 100. The first alternative is to use a single noninverting stage with a gain of 100. The second alternative is to cascade two noninverting stages, each having a gain of 10. Op amps with a gain bandwidth product of 10^6 are to be used. Write an expression for the gain as a function of frequency for each alternative. Find the 3-dB bandwidth for each alternative.

2.48. A certain internally compensated (dominant-pole) op amp has a dc gain of 200,000 and a 3-dB bandwidth of 5 Hz. Sketch the Bode plot of the magnitude of the open-loop gain to scale. If this op amp is used in a noninverting amplifier having a closed-loop dc gain of 100, sketch the Bode plot of the magnitude of the closed-loop gain to scale. Repeat for a closed-loop dc gain of 10.

Section 2.7: Large-Signal Operation

2.49. Define the terms *slew-rate limitation* and *full-power bandwidth*.

2.50. A certain op amp has a maximum output voltage range from -10 V to $+10\text{ V}$. The output can source or sink a maximum current of 20 mA. The slew-rate limit is $\text{SR} = 10\text{ V}/\mu\text{s}$. This op amp is used in the circuit of Figure 2.32.

- Find the full-power bandwidth of the op amp.

- (b) For a frequency of 1 kHz and $R_L = 1 \text{ k}\Omega$, what peak output voltage is possible without distortion?
- (c) For a frequency of 1 kHz and $R_L = 100 \Omega$, what peak output voltage is possible without distortion?
- (d) For a frequency of 1 MHz and $R_L = 1 \text{ k}\Omega$, what peak output voltage is possible without distortion?
- (e) If $R_L = 1 \text{ k}\Omega$ and $v_s(t) = 5 \sin(2\pi 10^6 t)$, sketch the output waveform to scale against time.

2.51. Suppose we want to design an amplifier that can produce a 100-kHz sine-wave output voltage having a peak amplitude of 5 V. What is the minimum slew-rate specification allowed for the op amp?

2.52. One way to measure the slew-rate limitation of an op amp is to apply a sine wave (or square wave) as the input to an amplifier and then increase the frequency until the output waveform becomes triangular. Suppose that a 1-MHz input signal produces a triangular output waveform having a peak-to-peak amplitude of 4 V. What is the slew-rate specification of the op amp?

2.53. A certain dominant-pole op amp has a unity-gain bandwidth of 5 MHz. This op amp is used in a noninverting amplifier having a dc gain of 100. If the input voltage $v_{in}(t)$ is the step function illustrated in Figure P2.53, sketch the output waveform to scale, assuming that neither clipping nor slew-rate limiting occurs. If the slew-rate limit of the op amp is $1 \text{ V}/\mu\text{s}$, what is the largest step amplitude V_m that can be applied to the input if slew-rate limiting is to be avoided?

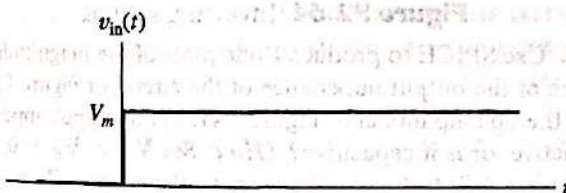


Figure P2.53

2.54. An op amp has a maximum output voltage range from -10 to $+10 \text{ V}$. The output can source or sink 25 mA . The slew-rate limit is $1 \text{ V}/\mu\text{s}$. The op amp is used in the amplifier shown in Figure P2.54.

- (a) Find the full-power bandwidth of the op amp.
- (b) For a frequency of 5 kHz and $R_L = 100 \Omega$, what peak output voltage is possible without distortion?
- (c) For a frequency of 5 kHz and $R_L = 10 \text{ k}\Omega$, what peak output voltage is possible without distortion?
- (d) For a frequency of 100 kHz and $R_L = 10 \text{ k}\Omega$, what peak output voltage is possible without distortion?

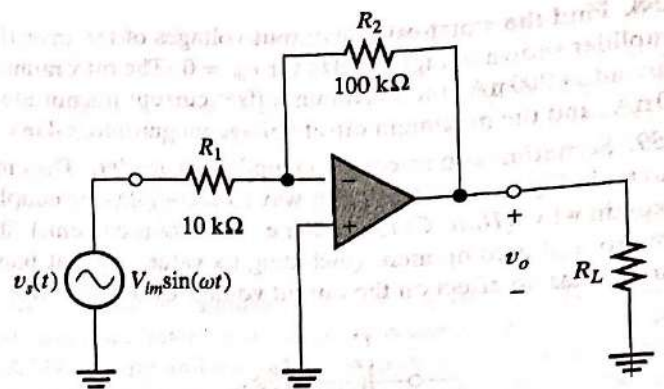


Figure P2.54

2.55. Consider the bridge amplifier illustrated in Figure P2.55. (a) Assuming ideal op amps, derive an expression for the voltage gain v_o/v_s . (b) If $v_s(t) = 3 \sin \omega t$, sketch $v_1(t)$, $v_2(t)$, and $v_o(t)$ to scale against time. (c) If the op amps are supplied from $\pm 15 \text{ V}$ and clip at an output voltage of $\pm 14 \text{ V}$, what is the peak value of $v_o(t)$ just at the threshold of clipping? (Comment: This circuit can be useful if a peak output voltage greater than the magnitude of the supply voltages is required.)

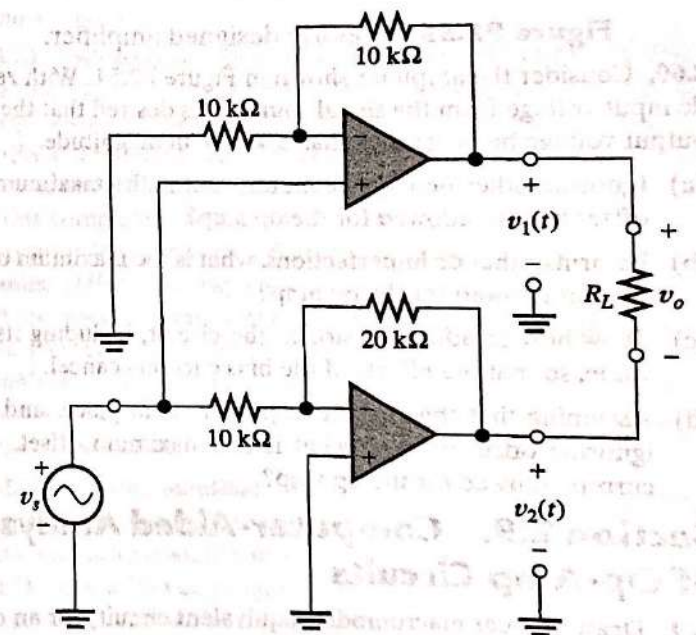


Figure P2.55 Bridge amplifier.

Section 2.8: DC Imperfections

2.56. Draw the circuit symbol for an op amp, adding sources to account for dc imperfections.

2.57. What is the main advantage of a FET-input op amp compared with a BJT-input op amp?

2.58. Find the worst-case dc output voltages of the inverting amplifier shown in Figure 2.34a for $v_{in} = 0$. The maximum bias current is 200 nA, the maximum offset current magnitude is 50 nA, and the maximum offset voltage magnitude is 4 mV.

2.59. Sometimes an ac-coupled amplifier is needed. The circuit shown in Figure P2.59 is a poor way to accomplish ac coupling. Explain why. (Hint: Consider the effect of bias current.) Show how to add a component (including its value) so that bias current has no effect on the output voltage of this circuit.

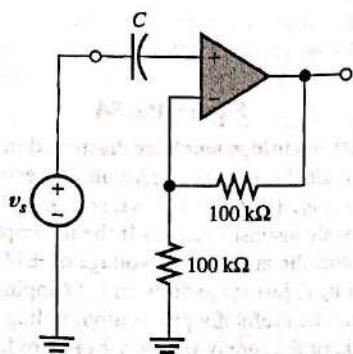


Figure P2.59 A poorly designed amplifier.

2.60. Consider the amplifier shown in Figure P2.54. With zero dc input voltage from the signal source, it is desired that the dc output voltage be no greater than 100 mV in magnitude.

- Ignoring other dc imperfections, what is the maximum offset voltage allowed for the op amp?
- Ignoring other dc imperfections, what is the maximum bias current allowed for the op amp?
- Show how to add a resistor to the circuit, including its value, so that the effects of the bias currents cancel.
- Assuming that the resistor of part (c) is in place, and ignoring offset voltage, what is the maximum offset current allowed for the op amp?

Section 2.9: Computer-Aided Analysis of Op-Amp Circuits

2.61. Draw a linear macromodel (equivalent circuit) for an op amp having a dominant pole.

2.62. What is a macromodel in a SPICE analysis? How is it useful?

2.63. The data sheet for a certain op amp gives an open-loop dc voltage gain of 80 dB, an input resistance of 100 kΩ, an output resistance of 50 Ω, and a unity-gain bandwidth of 10⁶ Hz. Draw a linear macromodel for the op amp, including numerical values for all components.

2.64. Consider the inverting summer circuit shown in Figure P2.64. The output voltage is given by

$$V_o = A_A V_A + A_B V_B$$

Use the op-amp model shown in Figure 2.41(a), together with SPICE programs, to generate magnitude Bode plots of the voltage gains A_A and A_B . (Hint: Set $V_B = 0$ when finding A_A , and set $V_A = 0$ when finding A_B .) How do the 3-dB bandwidths of the two gains compare? Find the gain-bandwidth product for A_A . Repeat for A_B . (Hint: An easy way to set up this op-amp model is to cut the op-amp symbol from the file named Fig2.37 and paste it into your circuit.)

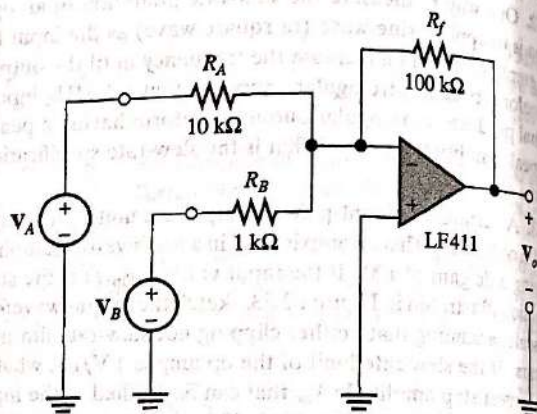


Figure P2.64 Inverting summer.

2.65. Use SPICE to produce Bode plots of the magnitude and phase of the output impedance of the circuit of Figure P2.64. Use the op amp model of Figure 2.41. Is the output impedance inductive, or is it capacitive? (Hint: Set $V_A = V_B = 0$, and connect a 1-A test current source to the output. Then the output impedance equals the voltage at the output terminal. Also, an easy way to set up this op-amp model is to cut the op-amp symbol from the file named Fig2.37 and paste it into your circuit.)

2.66. Use SPICE to obtain a Bode plot of the voltage gain V_o/V_{in} of the circuit of Figure 2.52. Use the op-amp model for the $\mu A741$ supplied with PSpice. Assume power-supply voltages of +15 V and -15 V. Select a frequency range for the analysis from 1 Hz to 10 kHz. The component values are

- $R_1 = 100 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $R_{bias} = 200 \text{ k}\Omega$, $C_1 = 0.1 \mu\text{F}$, and $C_2 = 0.1 \mu\text{F}$.
- $R_1 = 190 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_{bias} = 200 \text{ k}\Omega$, $C_1 = 0.01 \mu\text{F}$, and $C_2 = 1 \mu\text{F}$.
- Compare and comment on the results of parts (a) and (b).

2.67. Use SPICE to analyze the inverting amplifier shown in Figure P2.67. Use power-supply voltages of ± 15 V. Obtain a magnitude Bode plot of the voltage gain V_o/V_s . Estimate the range of frequencies for which the summing-point constraint is valid. (For purposes of this problem, define the valid range to be that for which the voltage magnitude at the inverting input is less than 1% of the magnitude of v_s .) Obtain plots of the magnitude and phase of the input impedance versus frequency. Finally, obtain a plot of the magnitude of the output impedance versus frequency. Compare the results with those of the ideal-op-amp analysis.

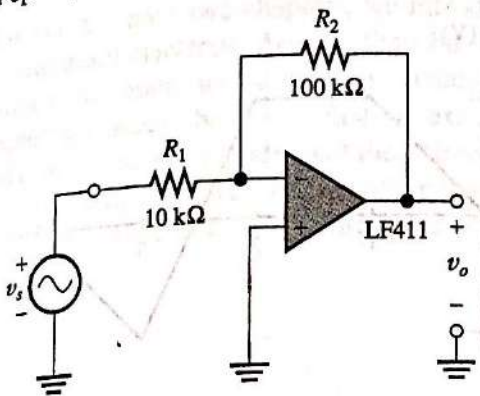


Figure P2.67

Section 2.10: A Collection of Amplifier Circuits.

2.68. Including resistors to cause the effects of bias current to cancel (where appropriate), draw the circuit diagrams of (a) a dc-coupled inverting amplifier; (b) an ac-coupled inverting amplifier; (c) a two-input summing amplifier; (d) a dc-coupled noninverting amplifier; (e) an ac-coupled noninverting amplifier; (f) a single-op-amp differential amplifier; (g) a voltage-to-current converter with floating load; (h) a current-to-voltage converter; (i) a current amplifier.

D2.69. Ac-coupled inverter design. Design an ac-coupled inverting amplifier. In the midband region, the input impedance magnitude should be at least $10\text{ k}\Omega$. The 3-dB bandwidth should extend from 100 Hz (or less) to 10 kHz (or more). At 1 kHz, the gain magnitude should be $10 \pm 5\%$. Include one or more resistors to minimize the effect of bias current. Use a SPICE program (or programs) to verify that your design meets the specifications given. Add a coupling capacitor to an inverter as shown in Figure 2.48. To achieve the desired accuracy, either use 1%-tolerance resistors or use an adjustable resistor.

D2.70. Ac-coupled noninverting amplifier. Repeat Problem D2.69 for an ac-coupled noninverting amplifier. Add a coupling capacitor and a resistor at the input of a noninverting amplifier

as shown in Figure 2.51. To achieve the desired accuracy, either use 1%-tolerance resistors or use an adjustable resistor.

D2.71. High-input-impedance ac-coupled noninverting amplifier. Repeat Problem D2.69 for an ac-coupled noninverting amplifier having an input impedance of at least $20\text{ M}\Omega$ at a frequency of 1 kHz. Use a circuit configuration similar to Figure 2.52. To achieve the desired accuracy, either use 1%-tolerance resistors or use an adjustable resistor.

D2.72. Differential amplifier. Design a single-op-amp differential amplifier having a nominal differential gain of 10. Use a $\mu\text{A}741$ op amp and standard 1%-tolerance resistors. Power supply voltages of $+15\text{ V}$ and -15 V are available. Write a PSpice program to plot the differential-mode gain magnitude (for a differential mode signal $v_1 = -v_2$) against frequency for the range from 100 Hz to 1 MHz. Use a Monte Carlo analysis with as many runs as your computer can accomplish in a reasonable time. Repeat the program for the common-mode gain ($v_1 = v_2$). What is the approximate worst-case common-mode rejection ratio (CMRR) at $f = 1\text{ kHz}$? The circuit configuration is shown in Figure 2.53. In the PSpice simulation, after drawing the circuit, double click the left mouse button with the cursor on each resistor and enter tolerance = 1%. Then use the analysis/setup/Monte Carlo menu to set up the analysis.

D2.73. Instrumentation-quality differential amplifier. Repeat Problem D2.72 using the LF411 and the instrumentation-quality circuit shown in Figure 2.54. (In this case, you will need to use the linear model for the LF411 illustrated in Figure 2.41, because the evaluation version of PSpice will not accommodate a circuit of this complexity with the full nonlinear macromodel for the op amp.) If you have worked Problem P2.72, compare the results. (Hint: An easy way to set up this op-amp model is to cut the op-amp symbol from the file named Fig2.37 and paste it into your circuit.) In the PSpice simulation, after drawing the circuit, double click the left mouse button with the cursor on each resistor and enter tolerance = 1%. Then use the analysis/setup/Monte Carlo menu to set up the analysis.

D2.74. Current amplifier. Design a current amplifier having a nominal gain magnitude of $3 \pm 5\%$ using discrete components. The load is a resistance of unknown value between $500\text{ }\Omega$ and $1\text{ k}\Omega$. Use a PSpice program to verify the design for a 1-kHz, 2-mA-peak sinusoidal input current. Use the circuit configuration shown in Figure 2.58.

Section 2.11: Integrators and Differentiators.

2.75. Sketch the output voltage of the circuit shown in Figure P2.75 to scale against time. Sometimes an integrator circuit is used as an (approximate) pulse counter. Suppose that the output voltage is -10 V . How many input pulses have been

applied? (Assume that the pulses have an amplitude of 5 V and a duration of 2 ms, as shown in the figure.)

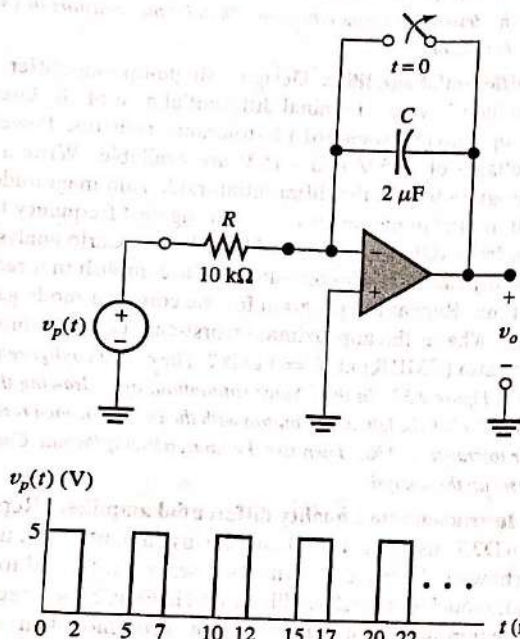


Figure P2.75

2.76. Sketch the output voltage of the ideal-op-amp circuit shown in Figure P2.76 to scale against time.

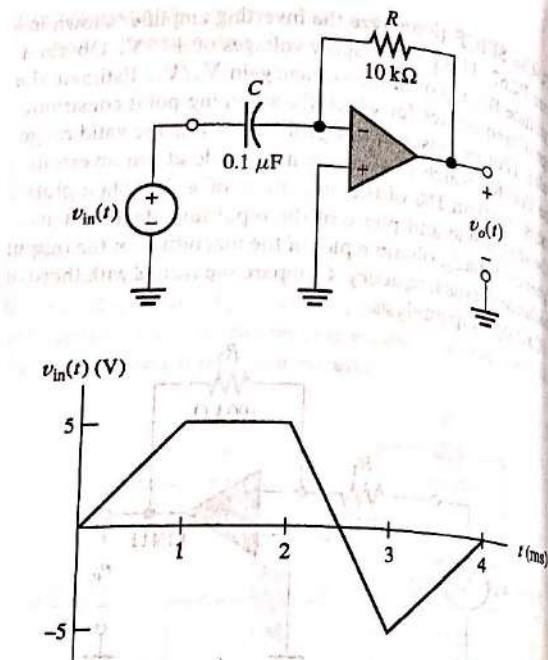


Figure P2.76

D2.77. Differentiator design. The displacement of a robot arm in a given direction is represented by a voltage signal $v_m(t)$. One volt corresponds to a displacement of 10 cm from the reference position. Design a circuit that produces a voltage $v_1(t)$ which is proportional to the velocity of the robot arm such that 1 m/s corresponds to 1 V. Design an additional circuit that produces a voltage v_2 which is proportional to the acceleration of the robot arm such that 1 m/s^2 corresponds to 1 V. Velocity is the derivative of displacement, thus we need a differentiator. Similarly acceleration is the derivative of velocity.

Diodes and Diode Circuits

In this and the next two chapters, we introduce the most important electronic devices, their basic circuit applications, and many useful analysis techniques. In this chapter, we discuss the diode. First, we examine the external characteristics of diodes and their circuit applications. Then, in the last three sections of the chapter, we discuss the internal operation of semiconductor diodes.

3

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3.1 DIODE CHARACTERISTICS

The diode is a very important electronic device that has two terminals: the **anode** and the **cathode**. The circuit symbol for a diode is shown in Figure 3.1a, and the diode volt-ampere characteristic is displayed in Figure 3.1b. As shown in Figure 3.1a, the voltage v_D across the diode is referenced as positive at the anode and negative at the cathode. Similarly, the diode current i_D is referenced as positive from anode to cathode.

Notice in the characteristic that if the voltage v_D across the diode is positive, relatively large amounts of current flow for small voltages. This condition is called **forward bias**. Thus, current flows easily through the diode in the direction of the arrowhead of the circuit symbol.

On the other hand, for moderately negative values of v_D , the current i_D is very small. This is called the **reverse-bias** region, as shown on the diode characteristic. If a sufficiently large reverse-bias voltage is applied to the diode, its operation enters the **reverse-breakdown** region of the characteristic, and currents of large magnitude flow. Provided that the power dissipated in the diode does not raise its temperature too high, reverse-breakdown operation is not destructive to the device. In fact, we will see that diodes are often deliberately operated in the reverse-breakdown region.

Small-Signal Diodes

Various materials and structures are used to fabricate diodes. For now, we confine our discussion to small-signal silicon diodes commonly found in low- and medium-power

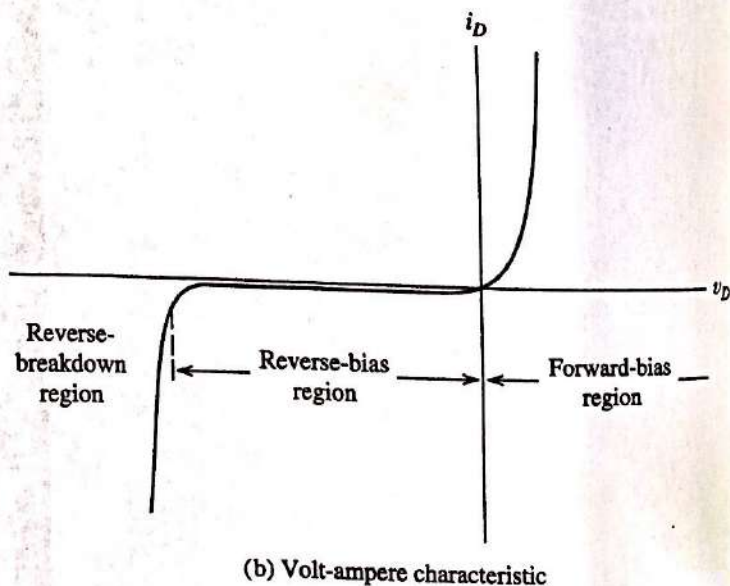
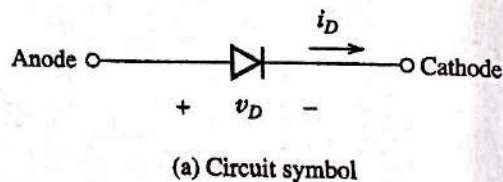


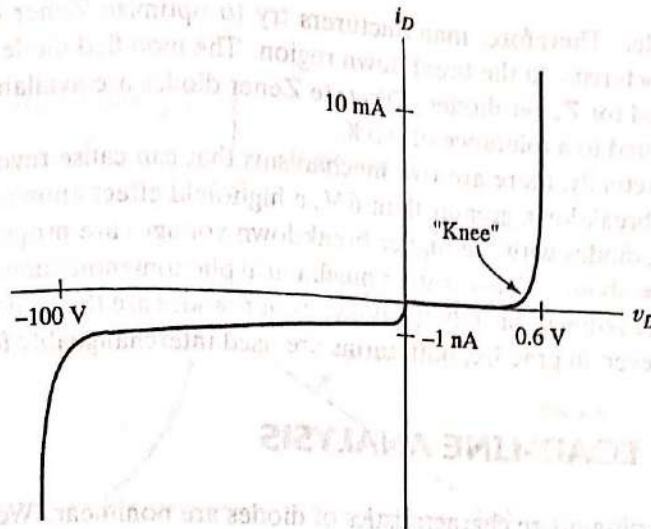
Figure 3.1
Semiconductor diode.

... current flows easily through the diode in the direction of the arrowhead.

... for moderately negative values of v_D , the current i_D is very small.

If a sufficiently large reverse-bias voltage is applied to the diode, ... currents of large magnitude flow.

Figure 3.2
Volt-ampere characteristic for a typical small-signal silicon diode at a temperature of 300 K. Notice the changes of scale.



electronic circuits. One such discrete diode is the 1N4148, which is available from several manufacturers. Integrated-circuit diodes have characteristics that are similar to small-signal discrete diodes.

The characteristic curve of a typical small-signal silicon diode operated at a temperature of 300 K is illustrated in Figure 3.2. Notice that the voltage and current scales for the forward-bias region are different than for the reverse-bias region. This helps to clearly display the details of the characteristic, because the current magnitudes are much smaller, and the voltage magnitudes much larger, in the reverse-bias region than in the forward-bias region.

In the forward-bias region, small-signal silicon diodes conduct very little current (much less than 1 mA), until a forward voltage of 0.6 to 0.7 V is applied (assuming that the diode is at a temperature of about 300 K). Then the current increases very rapidly as the voltage is increased further. We say that the forward characteristic displays a *knee* in the forward-bias characteristic at about 0.6 V. As the temperature increases, the knee voltage decreases by about 2 mV/K.

In the reverse-bias region, for small-signal silicon diodes at room temperature, a typical current is about 1 nA. As the temperature increases, the reverse current increases in magnitude. A rule of thumb is that the reverse current doubles for each 10-K increase in temperature.

When reverse breakdown is reached, the current increases in magnitude very rapidly. The voltage for which this occurs is called the **breakdown voltage**. For example, the breakdown voltage of the diode characteristic illustrated in Figure 3.2 is approximately -100 V. Breakdown voltages range from several volts to several hundred volts. Some applications call for diodes that operate in the forward-bias and nonconducting reverse-bias regions without entering the breakdown region. Diodes intended for these applications have a specification for the minimum magnitude of the breakdown voltage.

Zener Diodes

Diodes that are intended to operate in the breakdown region are called **Zener diodes**. Zener diodes are used in applications for which a constant voltage in breakdown is de-

As the temperature increases, the knee voltage decreases by about 2 mV/K.

A rule of thumb is that the reverse current doubles for each 10-K increase in temperature.

Zener diodes are used in applications for which a constant voltage in breakdown is desirable.



Figure 3.3 Zener diode symbol.

Graphical methods provide one approach to analyzing circuits containing nonlinear elements.

Load-line Equation.

sirable. Therefore, manufacturers try to optimize Zener diodes for a nearly vertical characteristic in the breakdown region. The modified diode symbol shown in Figure 3.3 is used for Zener diodes. Discrete Zener diodes are available with breakdown voltages specified to a tolerance of $\pm 5\%$.

Actually, there are two mechanisms that can cause reverse breakdown. For diodes with breakdown greater than 6 V, a high-field effect known as **avalanche** is responsible. Thus, diodes with the higher breakdown voltages are properly called **avalanche diodes**. Below about 6 V, a quantum mechanical phenomenon known as **tunneling** is responsible for breakdown. Strictly speaking, Zener diodes are those in the lower breakdown range. However, in practice, both terms are used interchangeably for all breakdown diodes.

3.2 LOAD-LINE ANALYSIS

The volt-ampere characteristics of diodes are nonlinear. We will see in the next several chapters that characteristics of other electronic devices are also nonlinear. Because of this nonlinearity, many of the techniques you have learned in basic circuit theory courses for dealing with linear circuits do not apply to circuits involving diodes. In fact, much of your study of electronics will be concerned with techniques for analyzing circuits containing nonlinear elements.

Graphical methods provide one approach to analyzing these kinds of circuits. For example, consider the circuit shown in Figure 3.4. Applying Kirchhoff's voltage law, we can write

$$V_{SS} = Ri_D + v_D \quad (3.1)$$

We assume that the values of V_{SS} and R are known and that we wish to find i_D and v_D . Thus, Equation (3.1) has two unknowns, and another relationship between i_D and v_D is needed to find a solution. The needed relationship is available in graphical form in Figure 3.5, which shows the volt-ampere characteristic of the diode.

We can obtain the solution by plotting Equation (3.1) on the same set of axes used for the diode characteristic. Because this equation is linear, it plots as a straight line that can be drawn if two points satisfying the equation are located. A simple method for locating these points is to assume that $i_D = 0$. Then Equation (3.1) yields $v_D = V_{SS}$. This pair of values is shown as point A in Figure 3.5. A second point results if we assume that $v_D = 0$, in which case the equation yields $i_D = V_{SS}/R$. This pair of values is shown as point B in Figure 3.5. Then, connecting points A and B results in the plot, which is called the **load line**. The **operating point** is the intersection of the load line and the diode characteristic. The operating point represents the simultaneous solution of Equation (3.1) and the diode characteristic.

Figure 3.4
Circuit for load-line analysis.

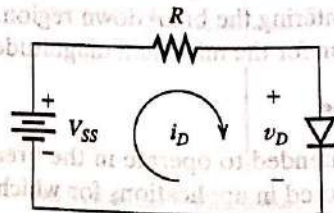
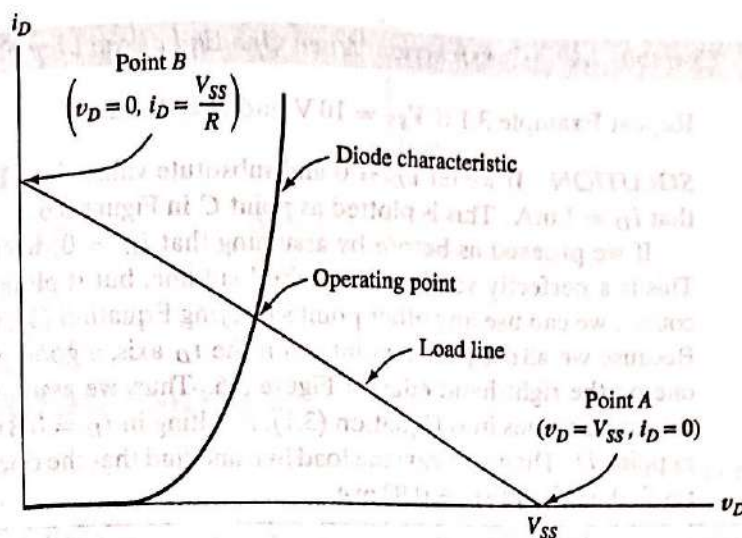


Figure 3.5
Load-line analysis of the circuit of Figure 3.4.



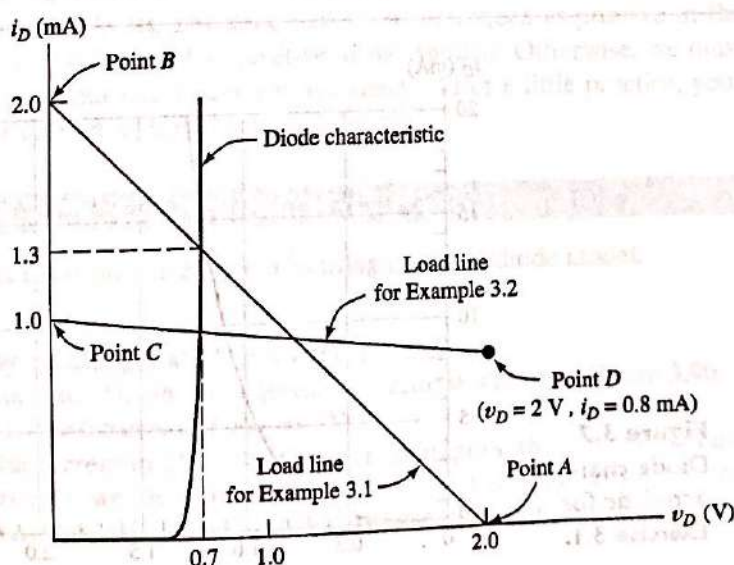
Example 3.1 Load-Line Construction for a Diode Circuit

If the circuit of Figure 3.4 has $V_{SS} = 2\text{ V}$, $R = 1\text{ k}\Omega$, and a diode with the characteristic shown in Figure 3.6, find the diode voltage and current at the operating point.

SOLUTION First, we locate the ends of the load line. Substituting $v_D = 0$ and the values given for V_{SS} and R into Equation (3.1) yields $i_D = 2\text{ mA}$. These values are plotted as point B in Figure 3.6. Substitution of $i_D = 0$ and $V_{SS} = 2\text{ V}$ results in $v_D = 2\text{ V}$. These values are plotted as point A in the figure. Constructing the load line results in an operating point of $v_D \cong 0.7\text{ V}$ and $i_D \cong 1.3\text{ mA}$, as shown in the figure. $\square$

Locate two points on the load line, then draw a straight line through them.

Figure 3.6
Load-line analysis for Examples 3.1 and 3.2.



Example 3.2 Construction When One End of the Line Falls Outside the Plot

Repeat Example 3.1 if $V_{SS} = 10\text{ V}$ and $R = 10\text{ k}\Omega$.

SOLUTION If we let $v_D = 0$ and substitute values into Equation (3.1), we find that $i_D = 1\text{ mA}$. This is plotted as point *C* in Figure 3.6.

If we proceed as before by assuming that $i_D = 0$, we find that $v_D = 10\text{ V}$. This is a perfectly valid point on the load line, but it plots far off the page. Of course, we can use any other point satisfying Equation (3.1) to locate the load line. Because we already have point *C* on the i_D axis, a good point to use would be one on the right-hand edge of Figure 3.6. Thus, we assume that $v_D = 2\text{ V}$ and substitute values into Equation (3.1), resulting in $i_D = 0.8\text{ mA}$. These values plot as point *D*. Then we draw the load line and find that the operating-point values are $v_D \cong 0.68\text{ V}$ and $i_D \cong 0.93\text{ mA}$.

EXERCISE

3.1 Find the operating point for the circuit of Figure 3.4 if the diode characteristic is shown in Figure 3.7 and

- (a) $V_{SS} = 2\text{ V}$ and $R = 100\ \Omega$;
- (b) $V_{SS} = 15\text{ V}$ and $R = 1\text{ k}\Omega$;
- (c) $V_{SS} = 1.0\text{ V}$ and $R = 20\ \Omega$.

Answer

- (a) $v_D \cong 1.08\text{ V}$, $i_D \cong 9.2\text{ mA}$;
- (b) $v_D \cong 1.18\text{ V}$, $i_D \cong 13.8\text{ mA}$;
- (c) $v_D \cong 0.91\text{ V}$, $i_D \cong 4.5\text{ mA}$.

Figure 3.7
Diode characteristic for Exercise 3.1.

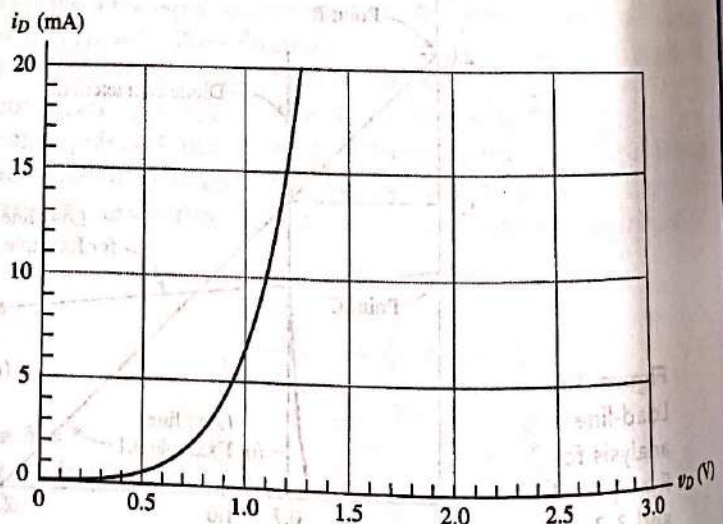
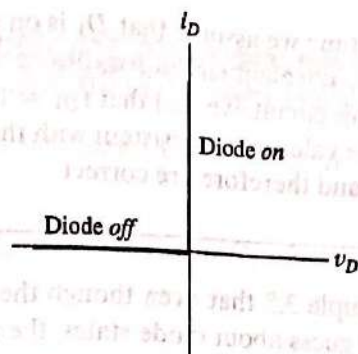


Figure 3.8
Ideal-diode
volt-ampere
characteristic.



3.3 THE IDEAL-DIODE MODEL

While load-line analysis of diode circuits provides insight and accurate results, we need simpler models in order to rapidly analyze circuits containing multiple diodes. One very useful model is the **ideal-diode model**, which is a perfect conductor with zero voltage drop in the forward direction. In the reverse direction, the ideal diode is an open circuit. We use the ideal-diode assumption if our judgment tells us that the forward diode voltage drop and reverse current are negligible or if we want a basic understanding, rather than an exact analysis, of a circuit. The volt-ampere characteristic for the ideal diode is illustrated in Figure 3.8. If i_D is positive, then v_D is zero, and we say that the diode is in the *on* state. On the other hand, if v_D is negative, then i_D is zero, and we say that the diode is in the *off* state.

Assumed States for Analysis of Ideal-Diode Circuits

When analyzing a circuit containing ideal diodes, we may not know in advance which diodes are on and which are off. Thus, we are forced to make considered guesses. Then we analyze the circuit to find the currents in the diodes assumed to be on and the voltages across the diodes assumed to be off. If i_D is positive for the diodes assumed to be on, and if v_D is negative for the diodes assumed to be off, our assumptions are correct and we have solved the circuit. (We are assuming that i_D is referenced as positive in the forward direction and v_D is referenced as positive at the anode.) Otherwise, we must make another assumption about the diodes and try again. After a little practice, your first guess will usually be correct, at least for simple circuits.

Example 3.3 Circuit Solution by Assumed Diode States

Analyze the circuit illustrated in Figure 3.9a using the ideal-diode model.

SOLUTION

- Step 1: We start by assuming that D_1 is off and D_2 is on.
 Step 2: With D_1 off and D_2 on, the equivalent circuit is shown in Figure 3.9b. Solving results in $i_{D2} = 0.5 \text{ mA}$ and $v_{D1} = 7 \text{ V}$.
 Step 3: Because the current in D_2 is positive, our assumption that D_2 is on seems to be correct. However, we also have $v_{D1} = +7 \text{ V}$, which is not consistent with the assumption that D_1 is off. Therefore, we must return to step 1 and try another assumption.

We use the ideal-diode assumption if our judgment tells us that the forward diode voltage drop and reverse current are negligible or if we want a basic understanding, rather than an exact analysis, of a circuit.

- Step 1: Assume a set of states for the diodes.
 Step 2: Solve the circuit to find i_D for diodes assumed to be on and v_D for diodes assumed to be off.
 Step 3: Check to see if i_D is positive for all diodes assumed to be on and if v_D is negative for all diodes assumed to be off. If so the solution is complete; otherwise return to step 1.

... we cannot decide on the state of a particular diode until we have found a combination of states that works for all of the diodes in the circuit.

Step 1: This time we assume that D_1 is on and D_2 is off.

Step 2: The equivalent circuit for these assumptions is illustrated in Figure 3.9c.

By solving this circuit, we find that $i_{D1} = 1 \text{ mA}$ and $v_{D2} = -3 \text{ V}$.

Step 3: These values are consistent with the assumptions about the diodes (D_1 on and D_2 off) and therefore are correct.

Notice in Example 3.3 that even though the current flows in the forward direction of D_2 for our first guess about diode states, the correct solution is that D_2 is off. Thus, in general, we cannot decide on the state of a particular diode until we have found a combination of states that works for all of the diodes in the circuit.

For a circuit containing n diodes, there are 2^n possible states. Thus, an exhaustive search eventually yields the solution.

EXERCISE

3.2 Show that the condition D_1 off and D_2 off is not valid for the circuit of Figure 3.9a.

EXERCISE

3.3 Show that the condition D_1 on and D_2 on is not valid for the circuit of Figure 3.9a.

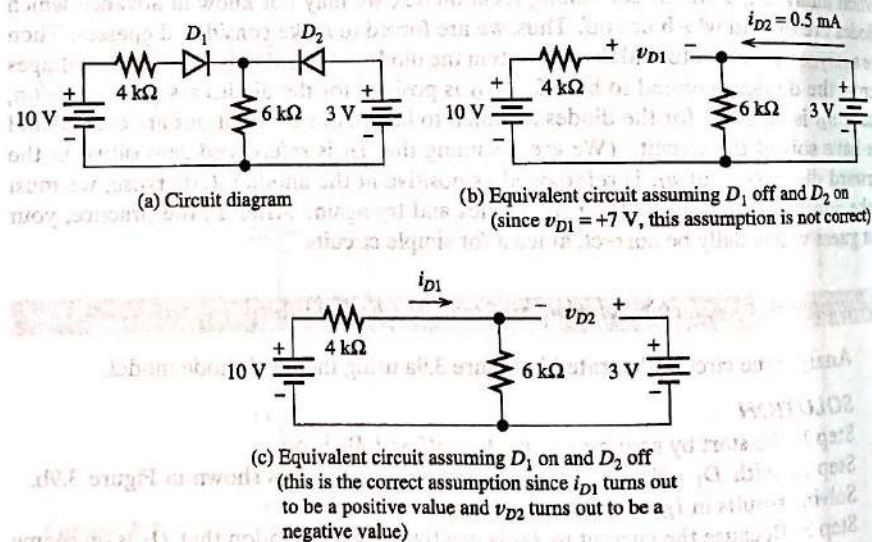


Figure 3.9 Analysis of a diode circuit using the ideal-diode model. See Example 3.3.

EXERCISE

3.4 Determine the diode states for the circuits shown in Figure 3.10. Assume ideal diodes.

Answer (a) D_1 is on; (b) D_2 is off; (c) D_3 is off and D_4 is on.

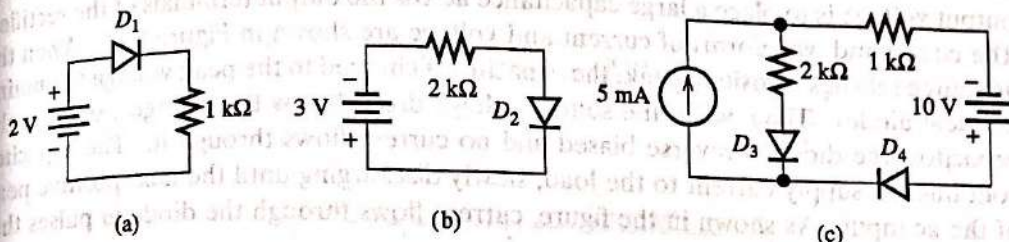


Figure 3.10 Circuits for Exercise 3.4.

3.4 RECTIFIER CIRCUITS

Now that we have introduced the diode and two methods for analyzing diode circuits, we consider some practical circuits. First, we examine several types of **rectifiers** that convert ac power into dc power. Rectifiers form the basis for electronic power supplies and battery-charging circuits. Rectifiers also are used in signal processing (e.g., to demodulate a radio signal) and in the precision conversion of an ac voltage to dc in an electronic voltmeter.

Half-Wave Rectifier Circuits

A **half-wave rectifier** with a sinusoidal source and resistive load is shown in Figure 3.11. When the source voltage $v_s(t)$ is positive, the diode is in the forward-bias region. Then if an ideal diode is assumed, the source voltage appears across the load. For a typical real

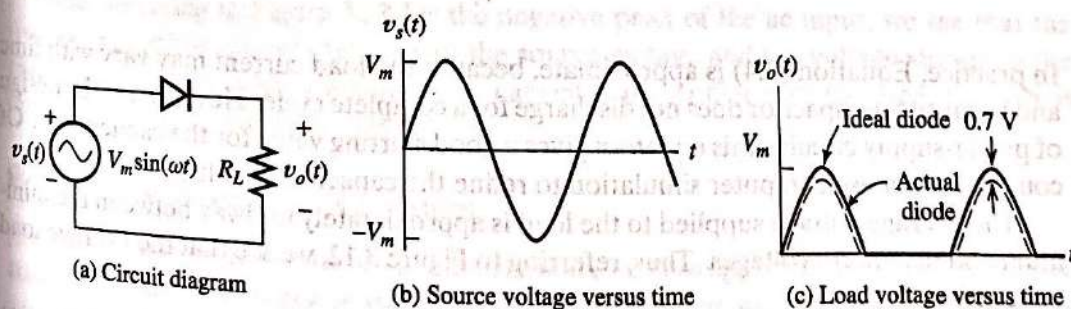


Figure 3.11 Half-wave rectifier with resistive load.

diode, the output voltage is less than the source voltage by an amount equal to the drop across the diode, which is about 0.7 V for silicon diodes at room temperature. If the source voltage is negative, the diode is reverse biased and no current flows through the load. Even for typical real diodes, only a very small reverse current flows. Thus, only the positive half-cycles of the source voltage appear across the load.

Half-Wave Rectifier with Smoothing Capacitor

Often, we want to convert an ac voltage into a nearly constant dc voltage that is to be used as a power supply for electronic circuits. One approach to smoothing the output voltage is to place a large capacitance across the output terminals of the rectifier. The circuit and waveforms of current and voltage are shown in Figure 3.12. When the ac source reaches a positive peak, the capacitor is charged to the peak voltage (assuming an ideal diode). Then, when the source voltage drops below the voltage stored on the capacitor, the diode is reverse biased and no current flows through it. The capacitor continues to supply current to the load, slowly discharging until the next positive peak of the ac input. As shown in the figure, current flows through the diode in pulses that recharge the capacitor.

Because of the charge-and-discharge cycle, the load voltage contains a small ac component called **ripple**. Usually, it is desirable to minimize ripple, so we choose the largest capacitance value that is practical. In this case, the capacitor discharges for nearly the entire cycle, and the charge removed from the capacitor during one discharge cycle is

$$Q \cong I_L T \quad (3.2)$$

where I_L is the average load current and T is the period of the ac voltage. Since the charge removed from the capacitor is the product of the change in voltage and the capacitance, we can also write

$$Q = V_r C \quad (3.3)$$

where V_r is the peak-to-peak ripple voltage and C is the capacitance. Equating the right-hand sides of Equations (3.2) and (3.3) allows us to solve for C :

$$C = \frac{I_L T}{V_r} \quad (3.4)$$

In practice, Equation (3.4) is approximate, because the load current may vary with time and because the capacitor does not discharge for a complete cycle. However, in the design of power-supply circuits, this equation gives a good starting value for the capacitance. Of course, we can use computer simulation to refine the capacitance value.

The average voltage supplied to the load is approximately midway between the minimum and maximum voltages. Thus, referring to Figure 3.12, we see that the average load voltage is

$$V_L \cong V_m - \frac{V_r}{2} \quad (3.5)$$

Equation for estimating the filter capacitance needed in a half-wave rectifier.

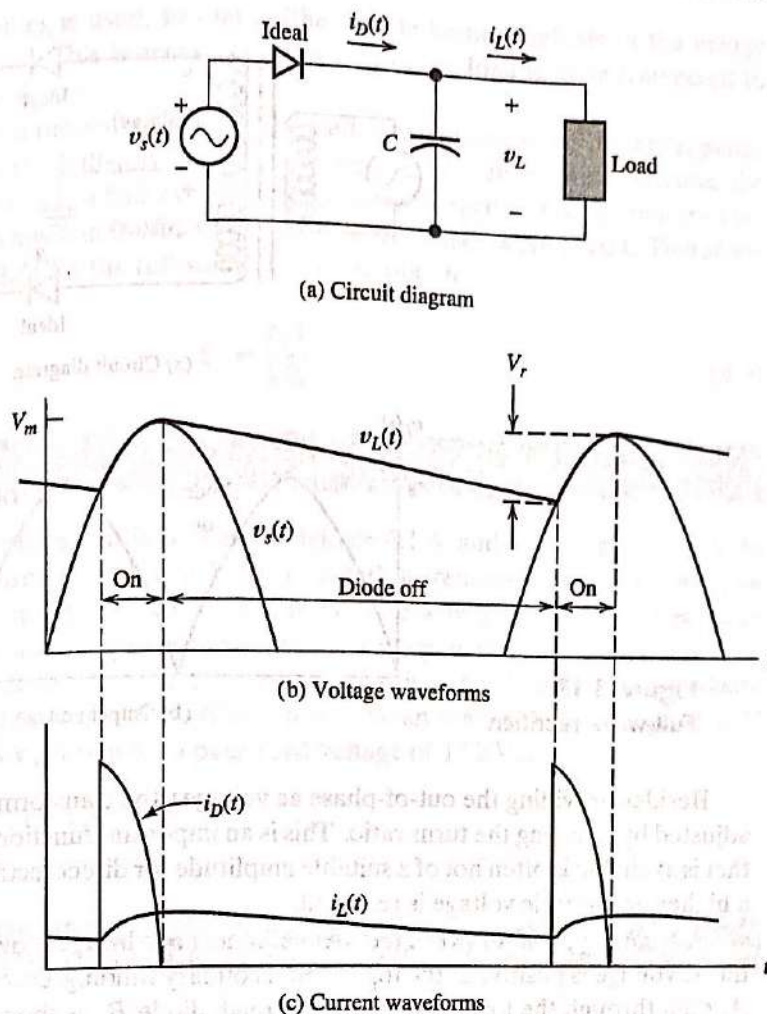


Figure 3.12
Half-wave rectifier with smoothing capacitor.

Peak Inverse Voltage

An important aspect of rectifier circuits is the **peak inverse voltage (PIV)** across the diodes. Of course, the breakdown specification of the diodes should be greater in magnitude than the PIV. For example, in the half-wave circuit with a resistive load, shown in Figure 3.11, the PIV is V_m .

Now, referring to Figure 3.12 for the negative peak of the ac input, we see that the reverse bias of the diode is the sum of the source voltage and the voltage stored on the capacitor. Thus by adding a smoothing capacitor in parallel with the load, the PIV is increased to (approximately) $2V_m$.

Full-Wave Rectifier Circuits

Several **full-wave rectifier** circuits are in common use. One approach uses a center-tapped transformer and two diodes, as shown in Figure 3.13. This circuit consists of two half-wave rectifiers with out-of-phase source voltages and a common load. The diodes conduct on alternate half cycles.

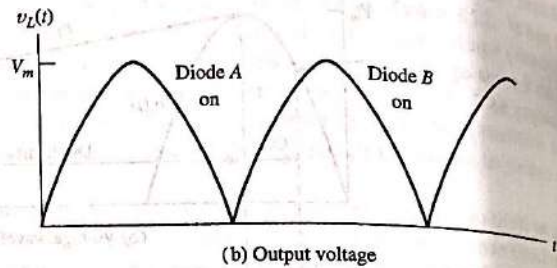
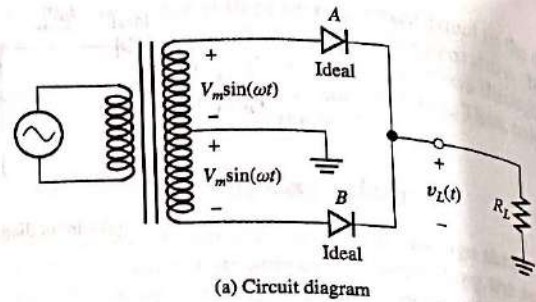


Figure 3.13
Full-wave rectifier.

A transformer allows the input of the rectifier to be selected by the designer. Furthermore, a transformer isolates the load from the ac power line.

Besides providing the out-of-phase ac voltages, the transformer also allows V_m to be adjusted by selecting the turns ratio. This is an important function because the ac voltage that is available is often not of a suitable amplitude for direct rectification—usually either a higher or lower dc voltage is required.

A second type of full-wave rectifier uses the **diode bridge** shown in Figure 3.14. When the ac voltage is positive at the top of the secondary winding, current flows through diode *A*, then through the load, and returns through diode *B*, as shown in the figure. For the opposite polarity, current flows through diodes *D* and *C*. Notice that in either case, current flows in the same direction through the load.

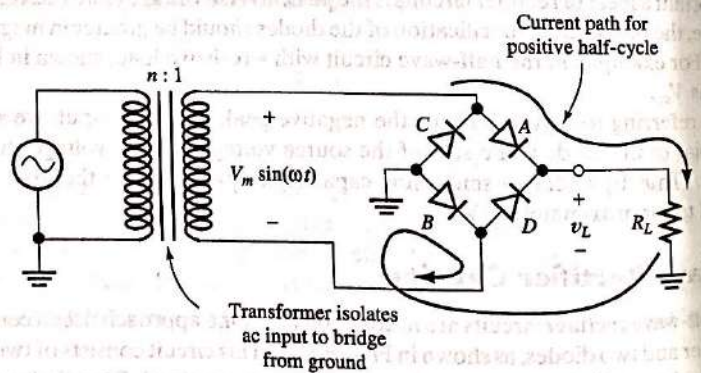


Figure 3.14 Diode-bridge full-wave rectifier.

Usually, a transformer is used, so that neither of the input terminals of the bridge are connected to ground. This is necessary if one side of the load is to be connected to ground as shown in the figure.

If we wish to smooth the voltage across the load, a capacitor can be placed in parallel with the load, as in the half-wave circuit discussed earlier. In full-wave circuits, the capacitor discharges for only a half-cycle before being recharged. Thus, the required capacitance is only half as much in the full-wave circuit as in the half-wave circuit. Therefore, we modify Equation (3.4) for the full-wave rectifier to obtain

$$C = \frac{I_L T}{2V_r} \quad (3.6)$$

Equation for estimating the filter capacitance needed in a full-wave rectifier.

EXERCISE

3.5 A power-supply circuit is needed to deliver 0.1 A and an average of 15 V to a load. The ac source available is 110 V rms with a frequency of 60 Hz. Assume that the full-wave circuit of Figure 3.14 is to be used with a smoothing capacitor in parallel with the load. The peak-to-peak ripple voltage is to be 0.4 V. Allow 0.7 V for forward diode drop. Find the turns ratio n that is needed and the approximate value of the smoothing capacitor. (*Hint:* To achieve an average load voltage of 15 V with a ripple of 0.4 V, design for a peak load voltage of 15.2 V.)

Answer $n = 9.37$, $C = 2083 \mu\text{F}$.

EXERCISE

3.6 Repeat Exercise 3.5 using the circuit of Figure 3.13 with a smoothing capacitor in parallel with R_L . (Define the turns ratio as the ratio of the number of primary turns to the number of secondary turns between the center tap and one end.)

Answer $n = 9.79$, $C = 2083 \mu\text{F}$.

3.5 WAVE-SHAPING CIRCUITS

A wide variety of **wave-shaping circuits** are useful in electronic systems. These circuits transform one waveform into another. Wave-shaping circuits are employed in function generators used to generate electrical test signals. Typically, an oscillator generates a square wave that is passed through an integrator (see Section 2.11), resulting in a triangular waveform. Then the triangular waveform is passed through a carefully designed wave-shaping circuit to produce a sinusoidal waveform. All three waveforms are available to the user. Numerous examples of wave-shaping circuits can be found in transmitters and receivers for television or radar.

Numerous examples of wave-shaping circuits can be found in transmitters and receivers for television or radar.

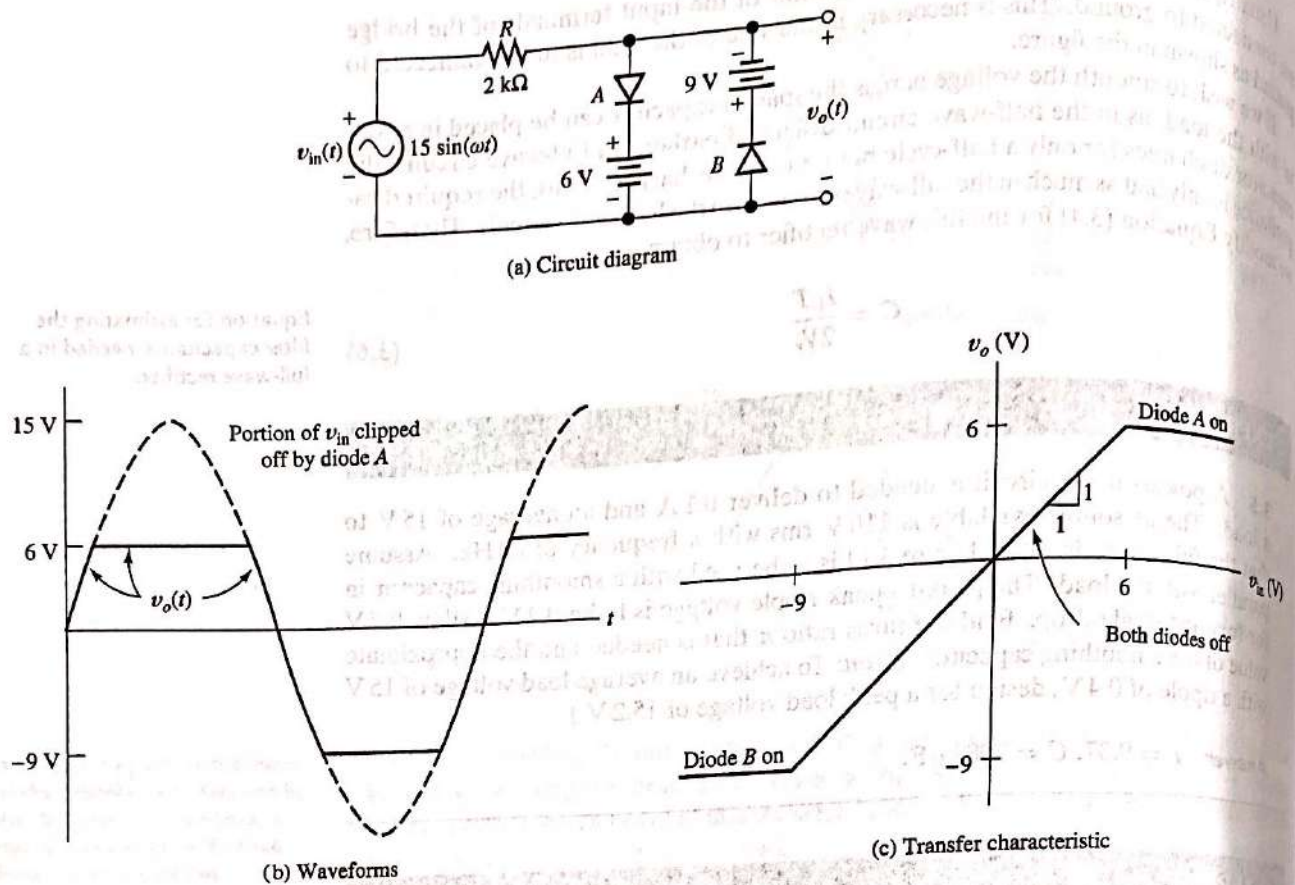
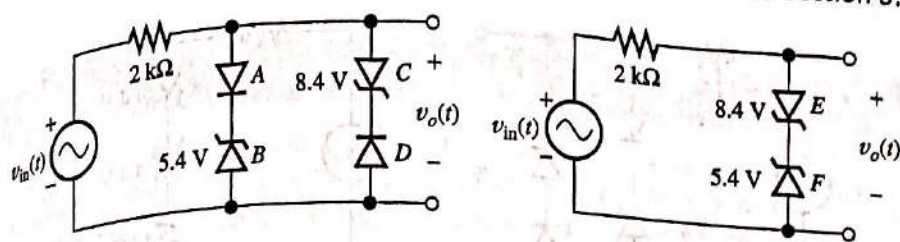


Figure 3.15 Clipper circuit.

Clipper Circuits

Diodes can be used to form **clipper circuits**, in which a portion of an input signal waveform is clipped off. For example, the circuit of Figure 3.15a clips off any part of the input waveform above 6 V or less than -9 V. (We are assuming ideal diodes.) If the input voltage is between -9 and +6 V, both diodes are off and no current flows. Then there is no drop across the resistance R , and the output voltage v_o is equal to the input voltage v_{in} . On the other hand, if v_{in} is larger than 6 V, diode A is on, and the output voltage is 6 V, because the diode connects the 6-V battery to the output terminals. Similarly, if v_{in} is less than -9 V, diode B is on and the output voltage is -9 V. The output waveform resulting from a 15-V-peak sinusoidal input is shown in Figure 3.15b, and the transfer characteristic of the circuit is shown in Figure 3.15c.

The resistor R is selected to be large enough so that the forward diode current is within reasonable bounds (usually, a few milliamperes), but small enough so that the reverse diode current results in a negligible voltage drop. Often, a wide range of resistance values provides satisfactory performance in a given circuit.



(a) Circuit of Figure 3.15 with batteries replaced by Zener diodes and allowance made for a 0.6 V forward diode drop

(b) Simpler circuit

Figure 3.16 Circuits with nearly the same performance as the circuit of Figure 3.15.

Replacing Batteries with Zener Diodes

In Figure 3.15, we have assumed ideal diodes. If small-signal silicon diodes are used, we expect a forward drop of about 0.6 to 0.7 V, so we should reduce the battery voltages to compensate. Furthermore, batteries are not desirable for use in circuits if they can be avoided, because they may need periodic replacement. Recall that in the breakdown region, the reverse voltage across a Zener diode is nearly constant. Thus, we can use Zener diodes in place of batteries in a clipper circuit. (Of course, a Zener diode behaves like a battery only in the reverse-breakdown region.)

Practical circuits equivalent to Figure 3.15 are shown in Figure 3.16. The Zener diodes are labeled with their breakdown voltages. In the circuit of Figure 3.16a, none of the diodes conduct if the input voltage is between -9 and $+6$ V. However, when the input voltage exceeds $+6$ V, diode *A* is forward biased and diode *B* is in reverse breakdown. Then the output voltage is the forward drop of diode *A* plus the reverse breakdown voltage of diode *B*. Hence, the output voltage is $0.6 + 5.4 = 6.0$ V. On the other hand, if the input voltage is less than -9 V, diode *D* is forward conducting and diode *C* is in reverse breakdown, resulting in an output voltage of -9 V.

In the circuit of Figure 3.16b, the diodes conduct no current and $v_o = v_{in}$, unless one of the diodes is in reverse breakdown. For $v_{in} > 6$ V, diode *E* is in forward bias and diode *F* is in reverse breakdown, resulting in $v_o = 6$ V. Similarly for $v_{in} < -9$ V, diode *F* is in forward bias and diode *E* is in reverse breakdown, resulting in $v_o = -9$ V.

EXERCISE

- 3.7 Sketch the transfer characteristics to scale for the circuits of Figures 3.17a and b. Allow a 0.6-V forward drop for the diodes. Sketch the output waveforms to scale if $v_{in}(t) = 15 \sin \omega t$.

Answer See Figures 3.17c and d.

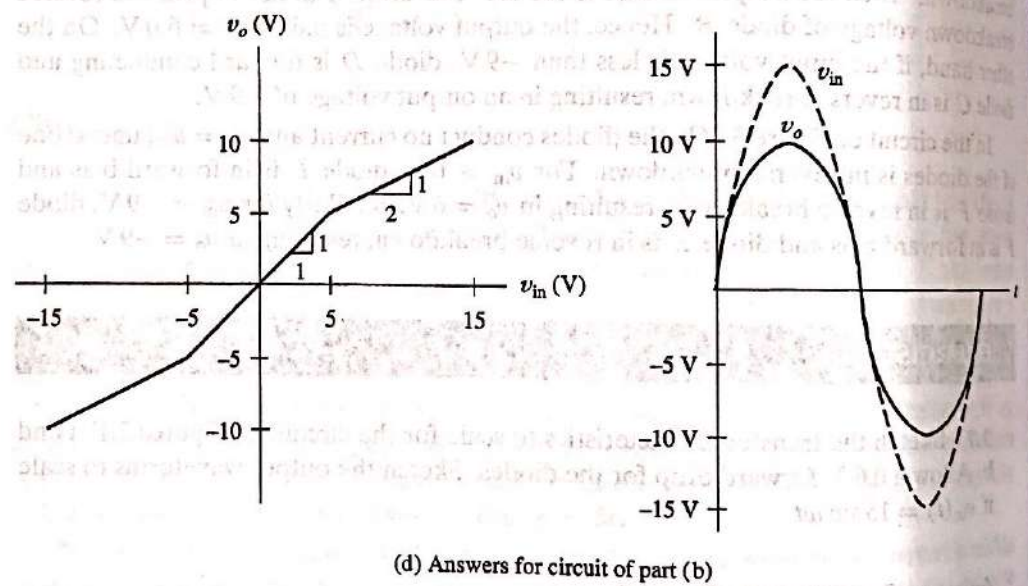
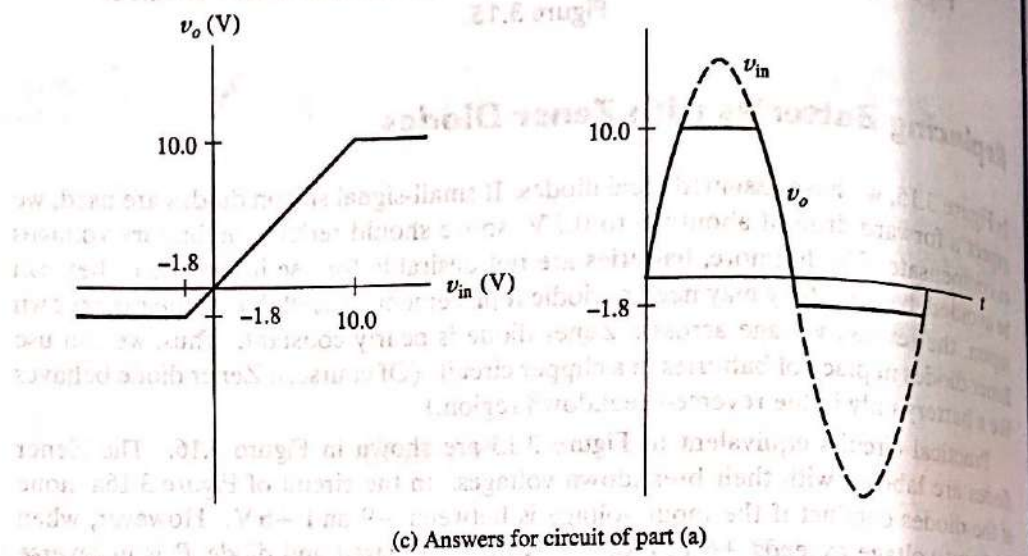
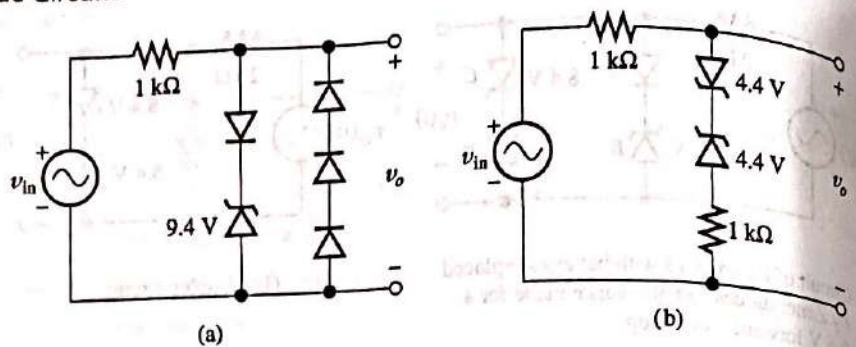


Figure 3.17 See Exercise 3.7.

EXERCISE

3.8 Design clipper circuits that have the transfer characteristics shown in Figures 3.18a and b. Allow for 0.6-V forward diode drops. (Hint for part b: Include a resistor in series with the diodes that begin to conduct at $v_{in} = 3\text{ V}$ to achieve the slope required for the section between $v_{in} = 3\text{ V}$ and 6 V .)

Answer See Figures 3.18c and d.

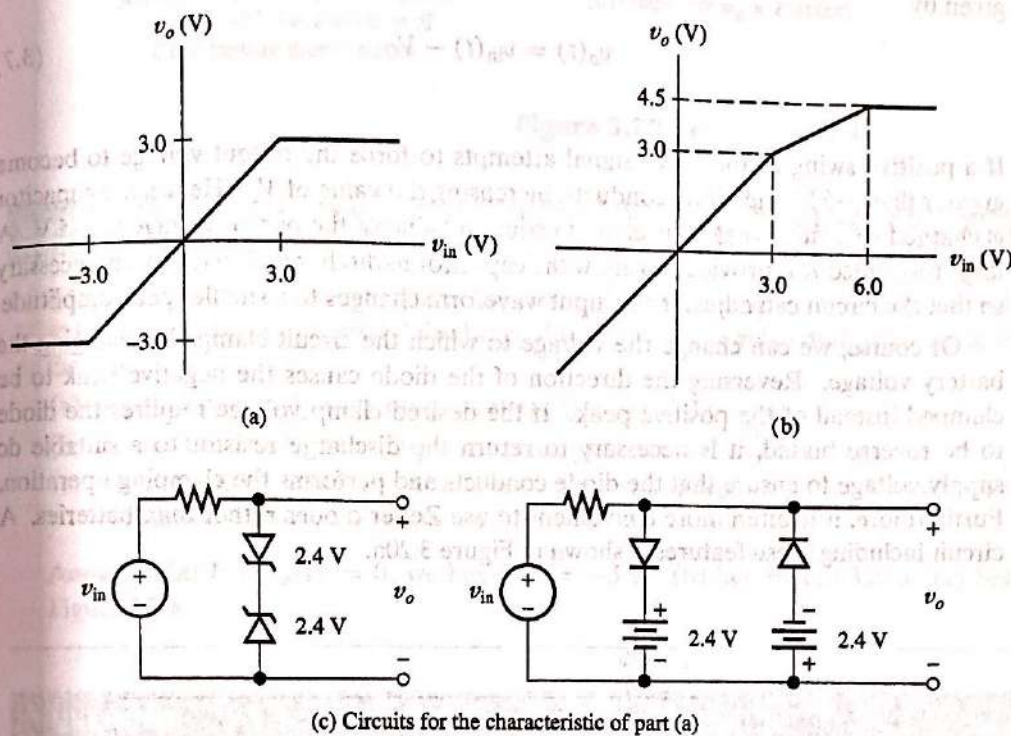


Figure 3.18 See Exercise 3.8.

Clamp Circuits

Another diode wave-shaping circuit is the **clamp circuit**, which is used to add a dc component to an ac input waveform so that the positive (or negative) peaks are forced to take a specified value. In other words, the peaks of the waveform are “clamped” to a specified voltage value. An example of a clamp circuit is shown in Figure 3.19. In this circuit, the positive peaks are clamped to -5 V .

The capacitor is a large value, so it discharges only very slowly, and we can consider the voltage across the capacitor to be constant. Because the capacitor is large, it has a very small impedance for the ac input signal. Thus, the output voltage of the circuit is given by

$$v_o(t) = v_{in}(t) - V_C \quad (3.7)$$

If a positive swing of the input signal attempts to force the output voltage to become greater than -5 V , the diode conducts, increasing the value of V_C . Hence, the capacitor is charged to a value that adjusts the maximum value of the output voltage to -5 V . A large resistance R is provided to allow the capacitor to discharge slowly. This is necessary so that the circuit can adjust if the input waveform changes to a smaller peak amplitude.

Of course, we can change the voltage to which the circuit clamps by changing the battery voltage. Reversing the direction of the diode causes the negative peak to be clamped instead of the positive peak. If the desired clamp voltage requires the diode to be reverse biased, it is necessary to return the discharge resistor to a suitable dc supply voltage to ensure that the diode conducts and performs the clamping operation. Furthermore, it is often more convenient to use Zener diodes rather than batteries. A circuit including these features is shown in Figure 3.20a.

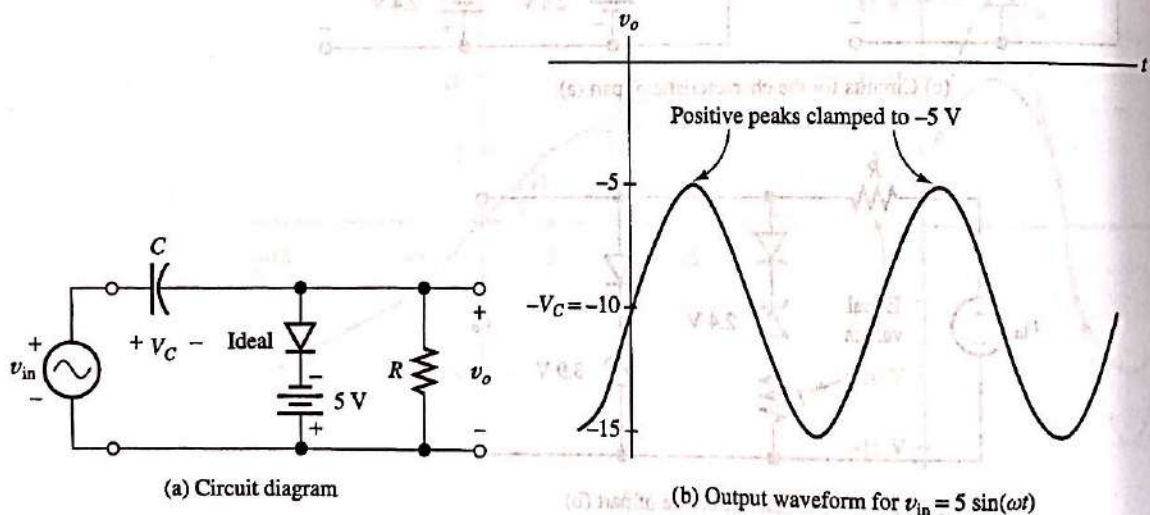


Figure 3.19 Example clamp circuit.

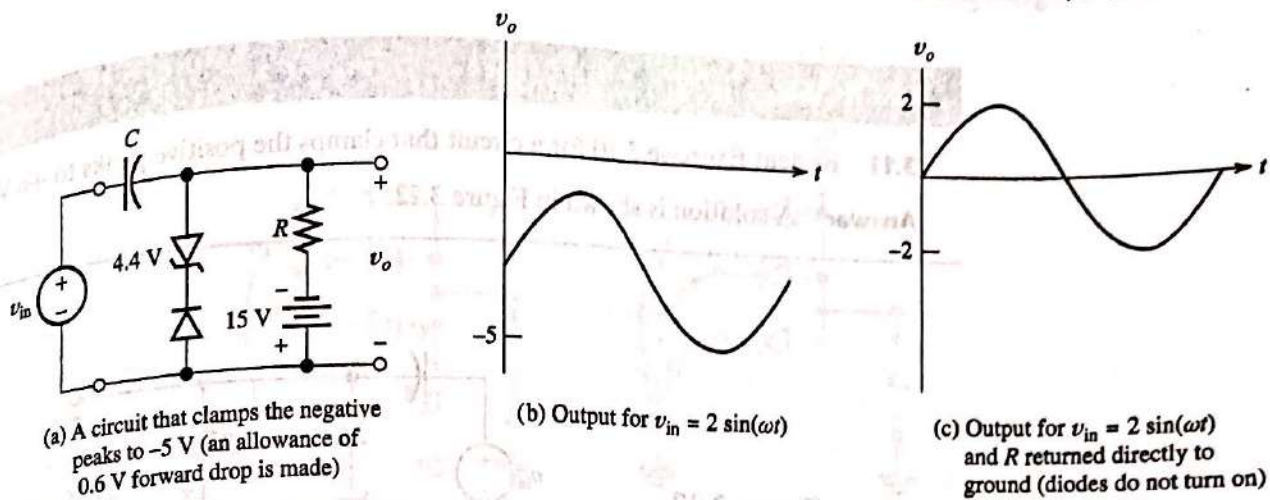


Figure 3.20 See Exercise 3.9.

EXERCISE

3.9 Consider the circuit of Figure 3.20a. Assume that the capacitor is large enough so the voltage across it does not discharge through R appreciably during one cycle of the input.

- What is the steady-state output voltage if $v_{in}(t) = 0$?
- Sketch the steady-state output to scale against time if $v_{in}(t) = 2 \sin(\omega t)$.
- Suppose that the resistor is returned to ground instead of -15 V. In this case, sketch the steady-state output against time if $v_{in}(t) = 2 \sin(\omega t)$.

Answer (a) For $v_{in}(t) = 0$, we have $v_o = -5$ V. (b) See Figure 3.20b. (c) See Figure 3.20c.

EXERCISE

3.10 Design a circuit that clamps the negative peaks of an ac signal to $+6$ V. You can use batteries, resistors, and capacitors of any value desired, in addition to Zener or conventional diodes (for both). Allow 0.6 V for the forward drop.

Answer A solution is shown in Figure 3.21.

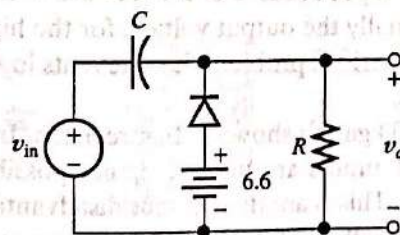


Figure 3.21
Answer for Ex-
ercise 3.10.

EXERCISE

3.11 Repeat Exercise 3.10 for a circuit that clamps the positive peaks to +6 V.

Answer A solution is shown in Figure 3.22.

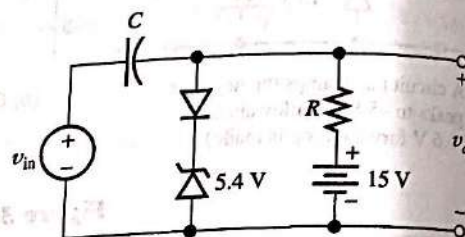


Figure 3.22
Answer for Exercise 3.11.

Selection of R and C

Selection of the R and C values for clamp circuits is a compromise.

Selecting the R and C values for clamp circuits is a compromise. On one hand, we want the capacitor to have a very small impedance compared with that of the resistor for the ac signal. This is necessary because we want the ac part of the output waveform to be identical to the input. On the other hand, if we make the RC time constant too long, the circuit takes a long time to adjust to reductions in input amplitude. For now, we can choose R to be a fairly large resistor, say, $10\text{ k}\Omega$ to $100\text{ k}\Omega$, so that the peak diode currents are not required to be too large (more than a few milliamperes). Next, we pick C so that the RC time constant is large compared with the period of the ac input signal—say, by an order of magnitude. This gives a clamp circuit with approximately the desired clamping action. Then we can simulate the circuit and adjust values until the performance is satisfactory.

3.6 DIODE LOGIC CIRCUITS

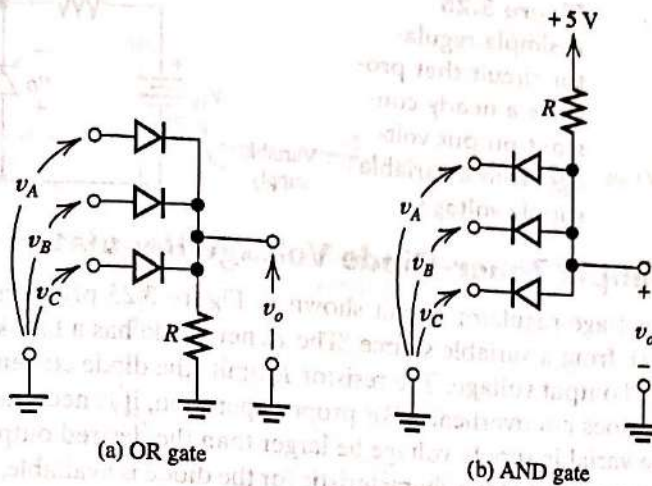
It is possible to construct a logic OR gate using diodes as shown in Figure 3.23a. Suppose that the input logic levels are +5 V for logic 1 and 0 V for logic 0. Then the output of the circuit is high (i.e., $v_o \cong 5\text{ V}$) if any of the inputs is high. If all of the inputs are low, the output is low ($v_o = 0$). Thus, the circuit performs the logical OR operation.

If we assume ideal diodes, the output logic levels are the same as those of the inputs. However, if real diodes are used, the high output of the OR gate of Figure 3.23a is a lower voltage than the input because of the forward diode drop. Thus, if a number of gates are cascaded, eventually the output voltage for the high state is too low to be recognized as logic 1. This is a serious problem that prevents logic circuits based solely on diodes from finding wide use.

A diode AND gate is shown in Figure 3.23b. In this circuit, the output is high (+5 V) only if all of the inputs are high. It is not possible to construct a logic inverter using ordinary diodes. This is another serious disadvantage of diode logic. Nevertheless, diode gates are occasionally useful.

It is not possible to construct a logic inverter using ordinary diodes.

Figure 3.23
Diode logic gates.



3.7 VOLTAGE-REGULATOR CIRCUITS

Sometimes we need to supply a nearly constant dc voltage to a load (typically, an electronic circuit such as an amplifier), but the raw sources of electrical power have variable voltages. For example, the rectifier circuits we discussed in Section 3.4 produce outputs with ripple. Furthermore, rectifier output voltages change when the ac line voltage fluctuates. To eliminate these fluctuations in voltage, we place a **voltage regulator** between the source and the load as shown in Figure 3.24.

The **source regulation** of a voltage regulator is a measure of how much the load voltage changes as the source voltage changes. It is defined as

$$\text{Source regulation} = \frac{\Delta V_{\text{load}}}{\Delta V_{SS}} \times 100\% \quad (3.8)$$

Equation defining source regulation.

where ΔV_{load} is the change in the load voltage resulting from a change of ΔV_{SS} in the source voltage.

Load regulation is a measure of the change in the load voltage as the load current changes. It is defined as

$$\text{Load regulation} = \frac{V_{\text{no-load}} - V_{\text{full-load}}}{V_{\text{full-load}}} \times 100\% \quad (3.9)$$

Equation defining load regulation.

where $V_{\text{no-load}}$ is the load voltage for zero load current and $V_{\text{full-load}}$ is the load voltage for rated load current. Ideally, we would like the source and load regulation to be zero in most applications.

Ideally, we would like the source and load regulation to be zero in most applications.

Figure 3.24
A voltage regulator
supplies constant
voltage to a load.

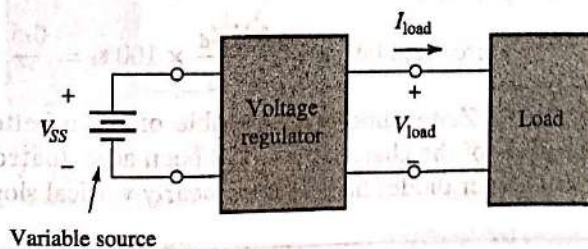
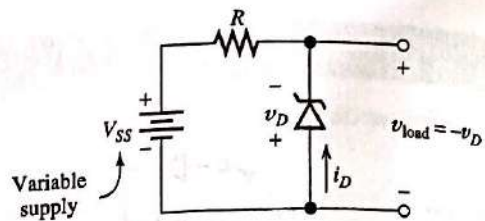


Figure 3.25

A simple regulator circuit that provides a nearly constant output voltage from a variable supply voltage.



A Simple Zener-Diode Voltage Regulator

This circuit is commonly used when a constant reference voltage is needed.

The voltage-regulator circuit shown in Figure 3.25 provides a nearly constant output voltage from a variable source. The Zener diode has a breakdown voltage equal to the desired output voltage. The resistor R limits the diode current to a safe value so that the diode does not overheat. (For proper operation, it is necessary that the minimum value of the variable supply voltage be larger than the desired output voltage.)

Assuming that the characteristic for the diode is available, we can use a load-line construction to analyze the operation of this regulator circuit. As before, we use Kirchhoff's voltage law to write an equation relating v_D and i_D . (In this circuit, the diode operates in the breakdown region with negative values for v_D and i_D .) For the circuit of Figure 3.25, we obtain

$$V_{SS} + Ri_D + v_D = 0 \quad (3.10)$$

This is the equation of a straight line, so locating any two points is sufficient to construct the load line. The intersection of the load line with the diode characteristic yields the operating point.

Example 3.4 Analysis of a Zener-Diode Regulator Circuit

The voltage-regulator circuit of Figure 3.25 has $R = 1 \text{ k}\Omega$ and uses the Zener diode having the characteristic shown in Figure 3.26. Find the output voltage for $V_{SS} = 15 \text{ V}$. Repeat for $V_{SS} = 20 \text{ V}$. Determine the percentage source regulation.

SOLUTION The load lines for both values of V_{SS} are shown in Figure 3.26. Notice that the two load lines are parallel. Inspection of Equation (3.10) shows that the slope of the load line is $-1/R$. Thus, a change in the supply voltage changes the position, but not the slope, of the load line.

The output voltages are determined from the operating points where the load lines intersect the diode characteristic. The output voltages are found to be $v_o = 10.0 \text{ V}$ for $V_{SS} = 15 \text{ V}$ and $v_o = 10.5 \text{ V}$ for $V_{SS} = 20 \text{ V}$. Thus, a 5-V change in the supply voltage results in only a 0.5-V change in the regulated output voltage. The source regulation is

$$\text{Source regulation} = \frac{\Delta V_{\text{load}}}{\Delta V_{SS}} \times 100\% = \frac{0.5}{5} \times 100\% = 10\%$$

Actual Zener diodes are capable of much better performance than this. The slope of the characteristic has been accentuated in Figure 3.26 for clarity—actual Zener diodes have a more nearly vertical slope in the breakdown region.

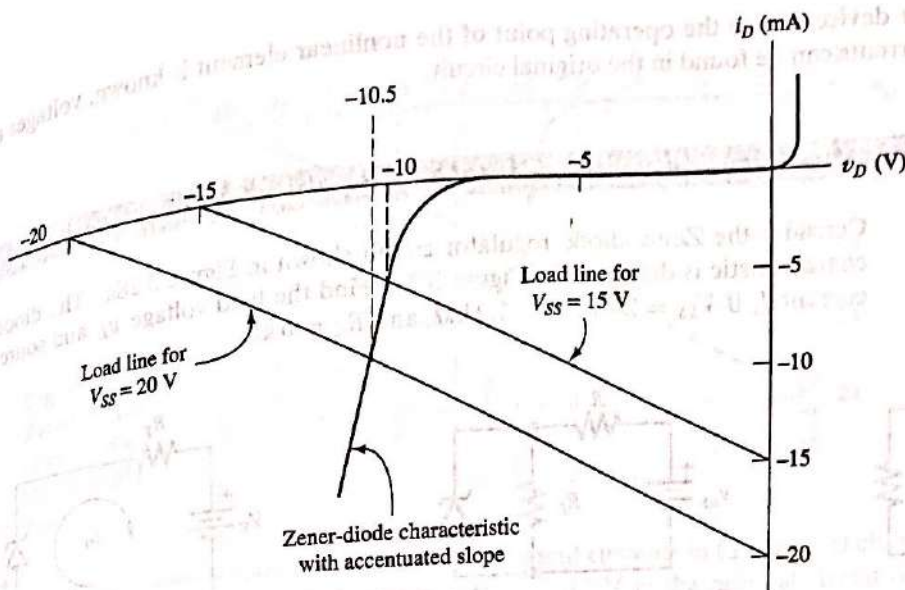


Figure 3.26 See Example 3.4.

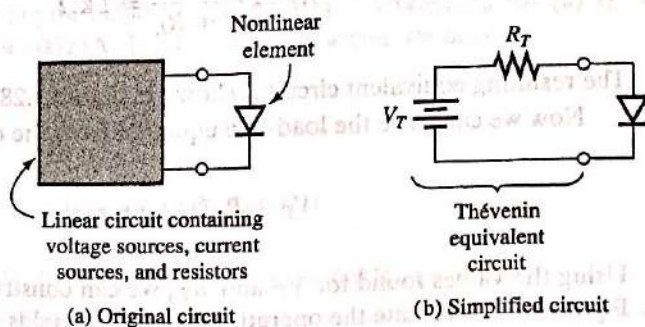
The breakdown voltages of Zener diodes are temperature dependent. In general, silicon diodes with breakdown voltages less than 6 V in magnitude display a reduction in breakdown voltage magnitude with increased temperature. Conversely, breakdown voltages greater than 6 V tend to increase in magnitude with temperature, whereas breakdown voltages of about 6 V tend to be nearly independent of temperature. Furthermore, the characteristic tends to be most vertical for Zener diodes with breakdown voltages close to 6 V. Thus, Zener diodes with a 6-V breakdown voltage provide the best performance as stable voltage references.

... Zener diodes with a 6-V breakdown voltage provide the best performance as stable voltage references.

Load-Line Analysis of Complex Circuits

Any circuit that contains resistors, voltage sources, current sources, and a single two-terminal nonlinear element can be analyzed by the load-line technique. First, the Thévenin equivalent is found for the linear portion of the circuit, as illustrated in Figure 3.27. Then, a load line is constructed to find the operating point on the characteristic of the nonlin-

Figure 3.27 Analysis of a circuit containing a singular nonlinear element can be accomplished by load-line analysis of a simplified circuit.



ear device. Once the operating point of the nonlinear element is known, voltages and currents can be found in the original circuit.

Example 3.5 Analysis of a Zener-Diode Regulator Circuit with Load

Consider the Zener-diode regulator circuit shown in Figure 3.28a. The diode characteristic is displayed in Figure 3.29. Find the load voltage v_L and source current I_s if $V_{SS} = 24\text{ V}$, $R = 1.2\text{ k}\Omega$, and $R_L = 6\text{ k}\Omega$.

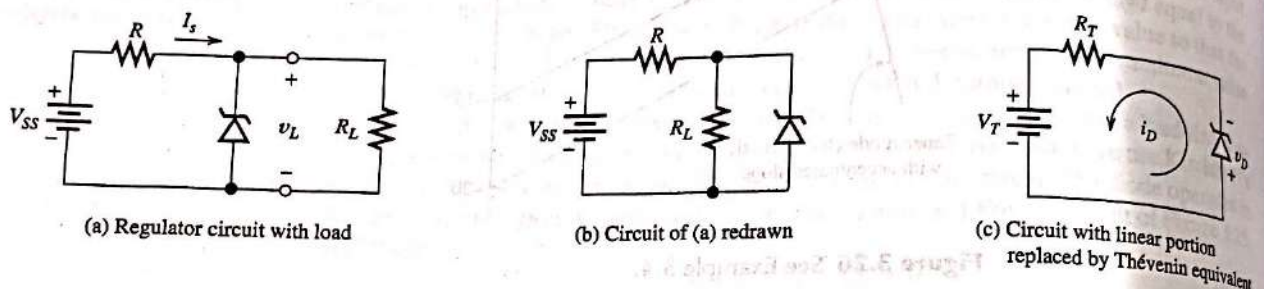


Figure 3.28 See Example 3.5.

First find the Thévenin equivalent for the linear part of the circuit. Then use load-line analysis of the simplified circuit.

SOLUTION First consider the circuit as redrawn in Figure 3.28b, in which we have grouped the linear elements together on the left-hand side of the diode. Next, we find the Thévenin equivalent for the linear portion of the circuit. The Thévenin voltage is the open-circuit voltage given by

$$V_T = V_{SS} \frac{R_L}{R + R_L} = 20\text{ V}$$

The Thévenin resistance can be found by setting the source voltage to zero. When reducing V_{SS} to zero, the voltage source becomes a short circuit. Then we have R and R_L in parallel, so the Thévenin resistance is

$$R_T = \frac{RR_L}{R + R_L} = 1\text{ k}\Omega$$

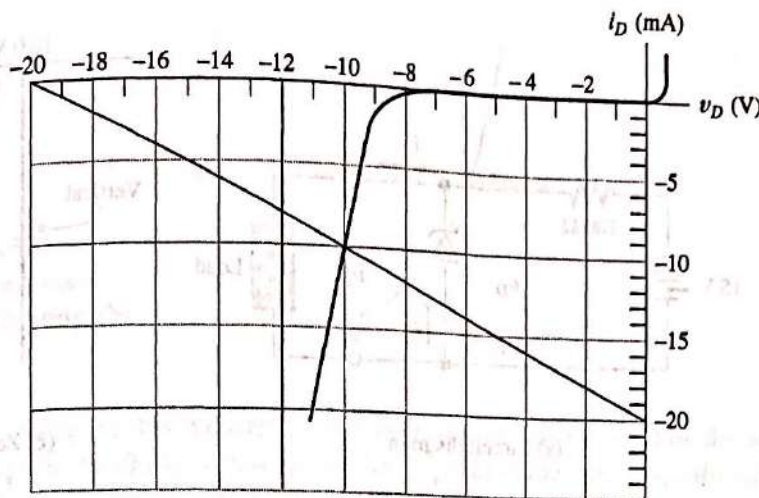
The resulting equivalent circuit is shown in Figure 3.28c.

Now we can write the load-line equation from the equivalent circuit as

$$V_T + R_T i_D + v_D = 0$$

Using the values found for V_T and R_T , we can construct the load line shown in Figure 3.29 and locate the operating point. This yields $v_L = -v_D = 10.0\text{ V}$.

Figure 3.29
Zener diode
characteristic
for Example
3.5.



Once v_L is known, we can find the voltages and currents in the original circuit. For example, using the output voltage value of 10.0 V in the original circuit of Figure 3.28a, we find that $I_s = (V_{SS} - v_L)/R = 11.67 \text{ mA}$.

EXERCISE

3.12 Find the voltage across the load in Example 3.5 if (a) $R_L = 1.2 \text{ k}\Omega$ and (b) $R_L = 400 \Omega$.

Answer (a) $v_L \cong 9.4 \text{ V}$; (b) $v_L \cong 6.0 \text{ V}$.

EXERCISE

3.13 Consider the circuit of Figure 3.30a. Assume that the breakdown characteristic is vertical, as shown in Figure 3.30b. Find the output voltage v_o for (a) $i_L = 0$; (b) $i_L = 20 \text{ mA}$; (c) $i_L = 100 \text{ mA}$. [Hint: From the circuit, we have

$$15 = 100(i_L - i_D) - v_D$$

Construct a different load line for each value of i_L .]

Answer (a) $v_o = 10.0 \text{ V}$; (b) $v_o = 10.0 \text{ V}$; (c) $v_o = 5.0 \text{ V}$.

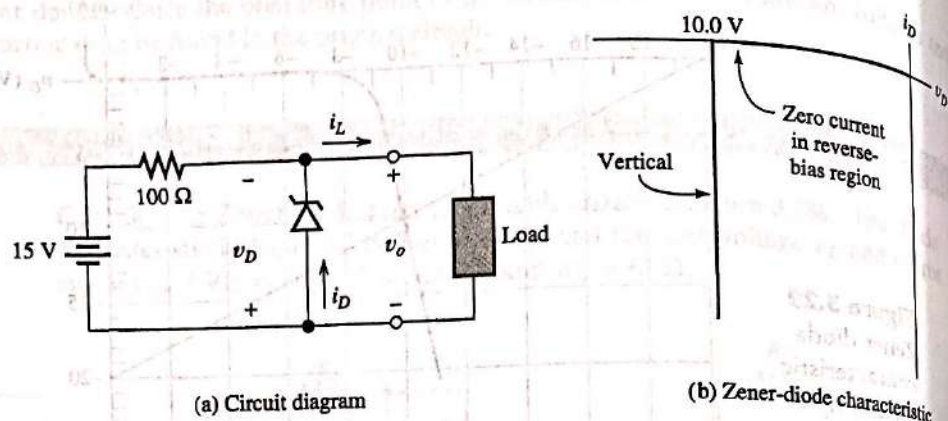


Figure 3.30 See Exercise 3.13.

3.8 LINEAR SMALL-SIGNAL EQUIVALENT CIRCUITS

We will encounter many examples of electronic circuits (especially amplifiers) in which dc supply voltages are used to **bias** a nonlinear device at an operating point and a small ac signal is injected into the circuit. We often split the analysis of such circuits into two parts. First, we analyze the dc circuit to find the operating point. In this analysis of bias conditions, we must deal with the nonlinear aspects of the device. In the second part of the analysis, we consider the small ac signal. Because device characteristics are approximately linear if we consider sufficiently small regions of operation, we can find a **linear small-signal equivalent circuit** for the nonlinear device to use in the ac analysis.

Often, the main concern in the design of such circuits is what happens to the ac signal. The dc supply voltages simply bias the device at a suitable operating point. For example, in a portable radio, the main interest is the signal being received, demodulated, amplified, and delivered to the speaker. The dc currents supplied by the battery are required for the devices to perform their intended function on the ac signals. However, most of our design effort is spent considering the small ac signals to be processed.

The small-signal linear equivalent circuit is an important analysis approach that applies to many types of electronic circuits. In this section, we demonstrate the principles with a simple diode circuit. In the next two chapters, we use similar techniques for transistor amplifier circuits.

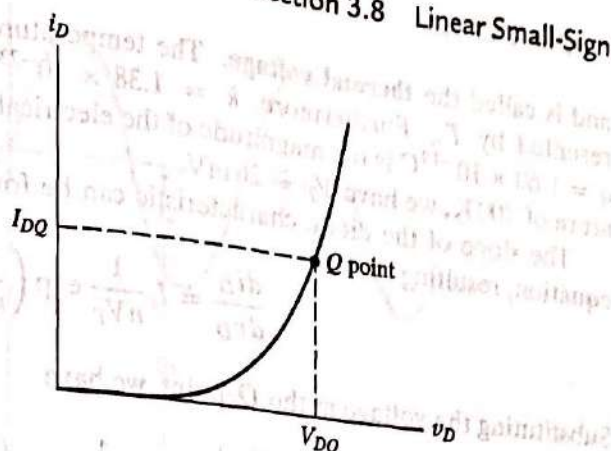
Dynamic Resistance

Now we show that in the case of a diode, the small-signal equivalent circuit consists of a resistance. Consider the diode characteristic shown in Figure 3.31. Assume that the dc supply voltage results in the circuit operating at the **quiescent point**, or ***Q*-point**, indicated on the characteristic. Then a small ac signal injected into the circuit swings the instantaneous point of operation slightly above and below the *Q*-point. For a sufficiently small ac signal, the characteristic is straight. Thus, we can write

$$\Delta i_D \cong \left(\frac{di_D}{dv_D} \right)_Q \Delta v_D \quad (3.1)$$

The small-signal linear equivalent circuit is an important analysis approach that applies to many types of electronic circuits.

Figure 3.31
Diode characteristic, illustrating the Q -point.



where Δi_D is the small change in diode current from the Q -point value caused by the ac signal, Δv_D is the change in the diode voltage from the Q -point value, and $(di_D/dv_D)_Q$ is the slope of the diode characteristic, evaluated at the Q -point. Notice that the slope has the units of inverse resistance. Thus, we define the **dynamic resistance** of the diode as

$$r_d = \left[\left(\frac{di_D}{dv_D} \right)_Q \right]^{-1} \quad (3.12)$$

and Equation (3.11) becomes

$$\Delta i_D \cong \frac{\Delta v_D}{r_d} \quad (3.13)$$

We find it convenient to drop the Δ notation and denote changes of current and voltage from the Q -point values as v_d and i_d . Therefore, for these small ac signals, we write

$$i_d = \frac{v_d}{r_d} \quad (3.14)$$

As shown by Equation (3.12), we can find the equivalent resistance of the diode for the small ac signal as the reciprocal of the slope of the characteristic curve.

The Shockley Equation

Under certain simplifying assumptions, theoretical considerations result in the following relationship between current and voltage in a pn -junction diode:

$$i_D = I_s \left[\exp \left(\frac{v_D}{nV_T} \right) - 1 \right] \quad (3.15)$$

This relationship is known as the **Shockley equation**. I_s is called the **saturation current** and has a value on the order of 10^{-14} A for small-signal junction diodes at 300 K. The parameter n is known as the **emission coefficient** and takes values between 1 and 2. The voltage V_T is given by

$$V_T = \frac{kT}{q} \quad (3.16)$$

The dynamic resistance of a diode is the inverse of the slope of the diode characteristic, evaluated at the Q -point.

and is called the **thermal voltage**. The temperature of the junction, in kelvins, is represented by T . Furthermore, $k = 1.38 \times 10^{-23} \text{ J/K}$ is Boltzmann's constant, and $q = 1.60 \times 10^{-19} \text{ C}$ is the magnitude of the electrical charge of an electron. At a temperature of 300 K, we have $V_T \cong 26 \text{ mV}$.

The slope of the diode characteristic can be found by differentiating the Shockley equation, resulting in

$$\frac{di_D}{dv_D} = I_s \frac{1}{nV_T} \exp\left(\frac{v_D}{nV_T}\right) \quad (3.17)$$

Substituting the voltage at the Q -point, we have

$$\left. \frac{di_D}{dv_D} \right|_Q = I_s \frac{1}{nV_T} \exp\left(\frac{V_{DQ}}{nV_T}\right) \quad (3.18)$$

For forward-bias conditions with V_{DQ} at least several times as large as V_T (i.e., for $V_{DQ} \geq 0.1 \text{ V}$), the -1 inside the brackets of Equation (3.15) is negligible. Thus, we can write

$$I_{DQ} \cong I_s \exp\left(\frac{V_{DQ}}{nV_T}\right) \quad (3.19)$$

Using Equation 3.19 to substitute into Equation (3.18), we obtain

$$\left. \frac{di_D}{dv_D} \right|_Q \cong \frac{I_{DQ}}{nV_T} \quad (3.20)$$

Substituting into Equation (3.12), we have the dynamic small-signal resistance of the diode at the Q -point:

$$r_d = \frac{nV_T}{I_{DQ}} \quad (3.21)$$

Key equation for diode dynamic resistance.

To summarize, for signals that cause small changes from the Q -point, we can treat the diode simply as a linear resistance.

To summarize, for signals that cause small changes from the Q -point, we can treat the diode simply as a linear resistance. Provided that the diode is forward biased, the value of the resistance is given by Equation (3.21).

Notation for Currents and Voltages in Electronic Circuits

Let us review the notation we have used for the diode currents and voltages, because we use similar notation throughout the book.

- v_D and i_D (lowercase symbols with uppercase subscripts) represent the total instantaneous diode voltage and current. At times, we may wish to emphasize the time-varying nature of these quantities and then we use $v_D(t)$ and $i_D(t)$.
 - V_{DQ} and I_{DQ} represent the dc diode current and voltage at the quiescent point.
 - v_d and i_d (lowercase symbols with lowercase subscripts) represent the (small) ac signals. If we wish to emphasize their time-varying nature, we use $v_d(t)$ and $i_d(t)$.
- This notation is illustrated in Figure 3.32.

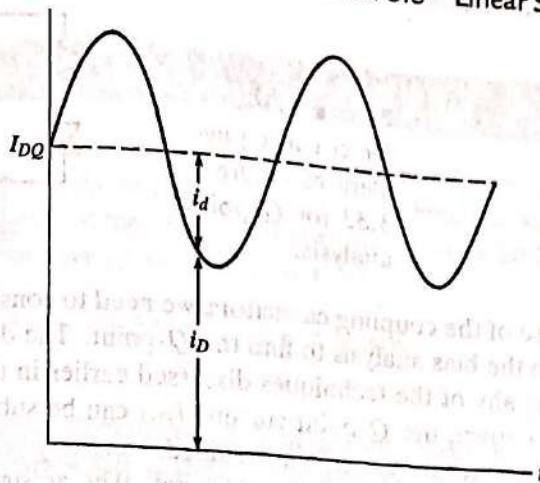


Figure 3.32
Illustration of diode currents.

EXERCISE

3.14 Compute the dynamic resistance of a pn -junction diode having $n = 1$ at a temperature of 300 K for $I_{DQ} =$ (a) 0.1 mA; (b) 1 mA; (c) 10 mA.

Answer (a) 260 Ω ; (b) 26 Ω ; (c) 2.6 Ω .

Voltage-Controlled Attenuator

Now we consider an example of linear equivalent circuit analysis for the simple voltage-controlled attenuator circuit shown in Figure 3.33. The input to the circuit is a small ac voltage, $v_{in}(t)$, and the output $v_o(t)$ is an attenuated version of the input. We will see that the amount of attenuation depends on the value of the dc control voltage V_C .

Notice that the ac signal to be attenuated is connected to the circuit by a **coupling capacitor**. The output voltage is connected to the load R_L by a second coupling capacitor. We select the capacitance values so that they are effectively short circuits for the ac signal. However, the coupling capacitors are open circuits for dc. Thus, the Q -point of the diode is unaffected by the signal source or the load. This can be important for a circuit that must work for various sources and loads that could affect the Q -point. Furthermore, the coupling capacitors prevent (sometimes undesirable) dc currents from flowing in the source or the load.

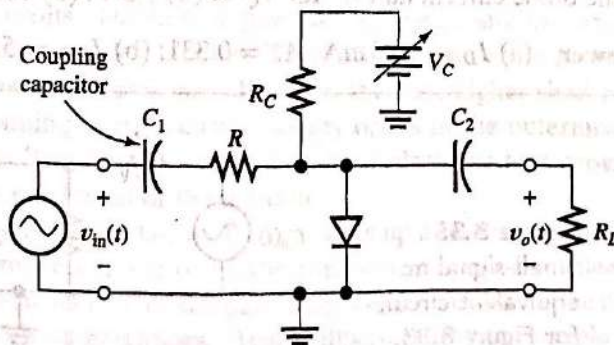
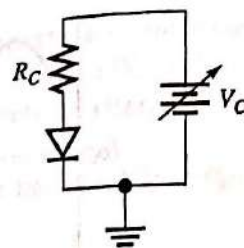


Figure 3.33
Variable attenuator using a diode as a controlled resistance.

This type of analysis will be very important in analyzing transistor circuits.

Figure 3.34
Dc circuit equivalent to Figure 3.33 for Q -point analysis.



Because of the coupling capacitors, we need to consider only V_C , R_C , and the diode to perform the bias analysis to find the Q -point. The dc circuit is shown in Figure 3.34. We can use any of the techniques discussed earlier in this chapter to find the Q -point. Once it is known, the Q -point current I_{DQ} can be substituted into Equation (3.21) to determine the dynamic resistance of the diode.

We turn our attention to the ac signal. The ac signal source causes an ac current to flow through the V_C source. However, V_C is a dc voltage source, and by definition, the voltage across it is constant. Because the dc voltage source has an ac component of current, but no ac voltage, the dc voltage source acts as a short circuit for ac signals. This is an important concept that we will use many times in drawing ac equivalent circuits.

The equivalent circuit for ac signals is shown in Figure 3.35. The control source and the capacitors have been replaced by short circuits, and the diode has been replaced by its dynamic resistance. This circuit is a voltage divider that can be analyzed by ordinary linear circuit analysis. We denote the parallel combination of R_C , R_L , and r_d as

$$R_p = R_C || R_L || r_d = \frac{1}{1/R_C + 1/R_L + 1/r_d} \quad (3.22)$$

Then the attenuation of the circuit is

$$A_v = \frac{v_o}{v_{in}} = \frac{R_p}{R + R_p} \quad (3.23)$$

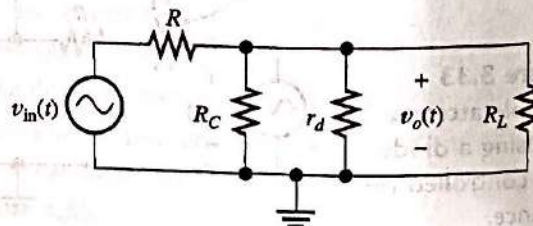
(Of course, A_v is less than unity.)

EXERCISE

3.15 Suppose that the circuit of Figure 3.33 has $R = 100 \Omega$, $R_C = 2 \text{ k}\Omega$, and $R_L = 2 \text{ k}\Omega$. The diode has $n = 1$ and is at a temperature of 300 K. For purposes of Q -point analysis, assume a constant diode voltage of 0.6 V. Find the Q -point value of the diode current and A_v for $V_C =$ (a) 1.6 V; (b) 10.6 V.

Answer (a) $I_{DQ} = 0.5 \text{ mA}$, $A_v = 0.331$; (b) $I_{DQ} = 5 \text{ mA}$, $A_v = 0.0492$.

Figure 3.35
Small-signal ac equivalent circuit for Figure 3.33.



EXERCISE

3.16 At a temperature of 300 K, a certain junction diode has $i_D = 0.1$ mA for $v_D = 0.6$ V. Assume that n is unity and use $V_T = 0.026$ V. Find the value of the saturation current I_s . Then compute the diode current at $v_D = 0.65$ V and at 0.70 V. [Hint: Because $v_D > 0.1$ V, we have $i_D \cong I_s \exp(v_D/nV_T)$.]

Answer $I_s = 9.50 \times 10^{-15}$ A, $i_D = 0.684$ mA, $i_D = 4.68$ mA.

EXERCISE

3.17 Consider a diode under forward bias, so that $i_D \cong I_s \exp(v_D/nV_T)$. Assume that $V_T = 0.026$ V and $n = 1$. (a) By what increment must v_D increase to double the current? (b) To increase the current by a factor of 10?

Answer (a) $\Delta v_D = 18$ mV; (b) $\Delta v_D = 59.9$ mV.

3.9 BASIC SEMICONDUCTOR CONCEPTS

In this section and the next, we discuss basic semiconductor physics and internal operation of diodes. Our discussion of device physics is brief and mostly of a qualitative nature. It is intended to give you a framework for understanding diode and transistor behavior—particularly high-frequency and switching characteristics.

Several materials are useful for the fabrication of solid-state electronic devices—most notably, silicon (Si), germanium (Ge), and gallium arsenide (GaAs). Because of the widespread use of silicon, we reference most of our discussion to it. At least on a qualitative basis, the physics of other semiconductors is similar to that of silicon.

Intrinsic Silicon

The Bohr model of an isolated silicon atom consists of a nucleus containing 14 protons and most of the mass of the atom. A total of 14 electrons surround the nucleus in specific orbits. The electron orbits occur in groups known as **shells**. The innermost (lowest energy) shell consists of two orbits. The next highest energy shell contains eight orbits. Each orbit can contain at most a single electron. Thus, for a silicon atom in its lowest energy state, the innermost shell contains two electrons, the next higher shell contains eight electrons, and the remaining four electrons occupy orbits in the outermost shell, also called the **valence shell**. It is these outermost valence electrons that provide the moving charge carriers in the solid form of the material.

In an **intrinsic** (i.e., pure) silicon crystal, each atom takes up a lattice position having four nearest neighboring atoms. Each pair of neighboring atoms forms a **covalent bond** consisting of two electrons that orbit around the pair. Each atom contributes one electron to each of the four bonds with its neighbors. This is illustrated by the simple planar

A qualitative knowledge of semiconductor physics helps us to understand diode and transistor behavior, especially in high-speed digital logic circuits.

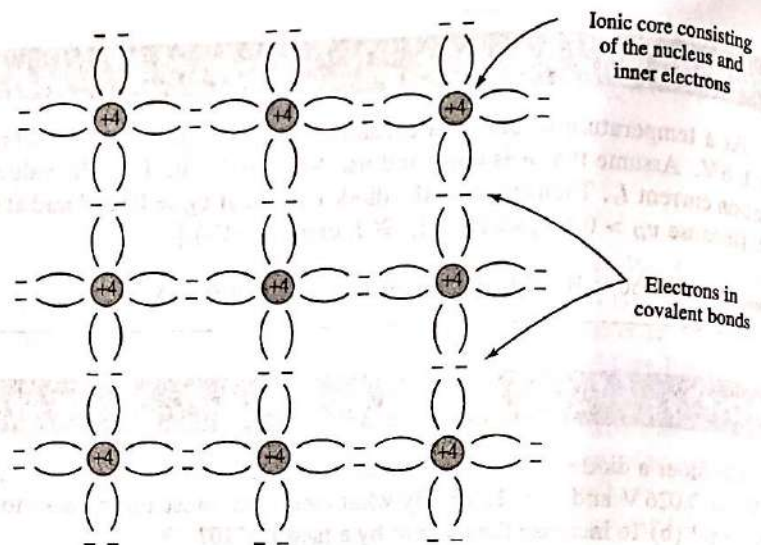


Figure 3.36 Intrinsic silicon crystal.

diagram shown in Figure 3.36. (In the actual crystal, the arrangement of the atoms is three dimensional—each atom is at the center of a tetrahedron with a neighbor located at each corner.)

At absolute zero temperature, electrons take the lowest energy states available. Thus, all of the valence electrons are bound in covalent bonds and are not free to move through the crystal. In this condition, silicon is an electrical insulator. However, at “room temperature” (approximately 300 K), a small fraction of the electrons gain sufficient thermal energy to break loose from their bonds. These **free electrons** can easily move through the crystal. This situation is illustrated in Figure 3.37.

If voltage is applied to intrinsic silicon, current flows. However, the number of free electrons is relatively small compared with that found in a good conductor. Thus, intrinsic silicon is classed as a **semiconductor**. Silicon contains about 5×10^{22} atoms/cm³. At

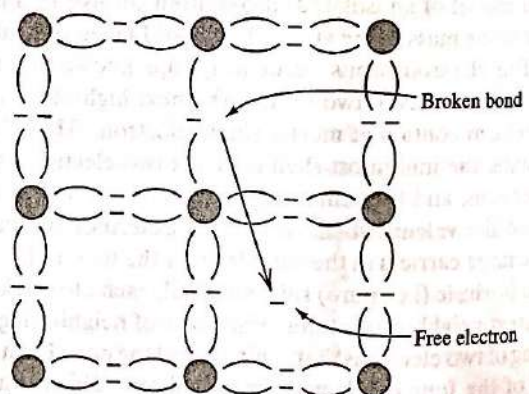
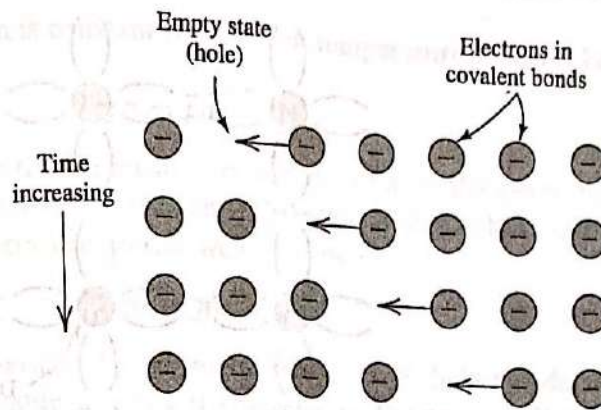


Figure 3.37
Thermal energy can break a bond, creating a vacancy and a free electron, both of which can move freely through the crystal.

Figure 3.38

As electrons move to the left to fill a hole, the hole moves to the right.



room temperature, there are $n_i \cong 1.45 \times 10^{10}$ free electrons per cm^3 . Thus, only about one valence electron in 1.4×10^{13} has broken loose from its bond at room temperature.

Conduction by Holes

Free electrons are not the only means by which current flows in intrinsic silicon. A broken bond can be filled by an electron from a nearby bond, as is illustrated in Figure 3.38. Even though it is the bound electrons that actually move, it is helpful to focus on the vacancy, or **hole**. We can think of a hole as a positive charge carrier that is free to move through the crystal, whereas bound electrons can move only if a vacancy exists nearby.

In an intrinsic semiconductor, an equal number of holes and free electrons are available to move easily through the crystal. We denote the free-electron concentration as n_i and the hole concentration as p_i . Thus, we can write

$$n_i = p_i \quad (3.24)$$

for a pure material. When an electric field is applied to the crystal, both types of carriers contribute to the flow of current.

Generation and Recombination

Free electrons and holes are generated by thermal energy, which causes covalent bonds to break at a rate depending strongly on temperature. The higher the temperature, the higher the rate of **generation**. On the other hand, when a free electron encounters a hole, **recombination** can occur: The hole and free electron combine to form a filled covalent bond. As the concentration of holes and electrons builds up, recombination occurs more frequently. Thus, at a given temperature, an equilibrium exists at which the rate of recombination equals the rate of generation of charge carriers. As the temperature increases, this equilibrium pertains to ever larger concentrations of charge carriers.

A higher concentration of charge carriers results in an increased capability of the material to conduct electrical current. Thus, the conductivity of an intrinsic semiconductor increases with temperature.

We can think of a hole as a positive charge carrier that is free to move through the crystal...

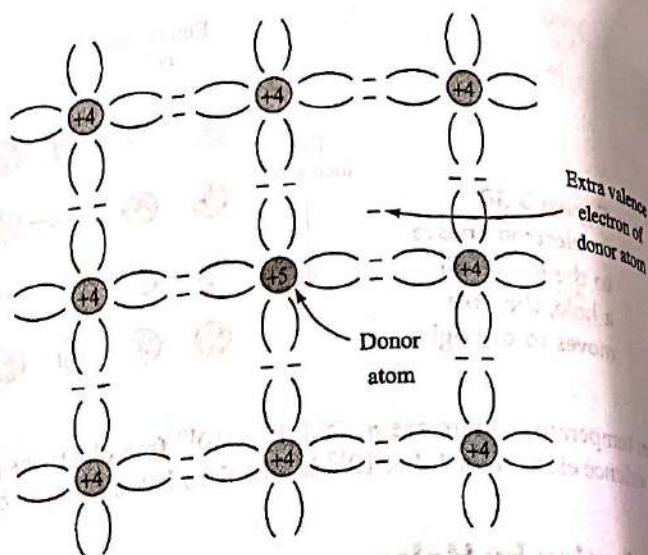


Figure 3.39
n-type silicon is created by adding valence five impurity atoms.

n-Type Semiconductor Material

Adding small amounts of suitable impurities to the crystal dramatically affects the relative concentration of holes and electrons. Then we have an **extrinsic** semiconductor. For example, if we add phosphorus, which has five valence electrons, the phosphorus atoms take positions in the crystal lattice and form covalent bonds with their four neighbors. The fifth valence electron is only weakly bound to the phosphorus atom.

At normal operating temperatures, this extra electron breaks its bond with the impurity atom and becomes a free electron. However, a hole is not created by the impurity atom—the positive charge that balances the free electron is locked in the ionic core of the impurity atom. Thus, we can create free electrons by adding pentavalent impurities known as **donors** to silicon. The resulting material is called ***n*-type material**. The crystal lattice of *n*-type silicon is depicted in Figure 3.39.

In *n*-type material, conduction is due mainly to the numerous free electrons. Thus, free electrons are called **majority carriers**, whereas holes are called **minority carriers**.

At normal operating temperatures, nearly all of the donor atoms give up their fifth electron. We say that the donors have become **ionized**. Positive charge is associated with each ionized donor atom. Of course, the net charge concentration in the material is zero. The positive charge of the ionized donors (and holes) is balanced by the negative charge of free electrons. Thus, we can equate the concentration of free electrons to the sum of the hole and donor concentrations; that is,

$$n = p + N_D \quad (3.25)$$

where N_D represents the concentration of donor atoms.

The Mass-Action Law

Not only is the free-electron concentration increased by the addition of donor atoms; the hole concentration is reduced, because the increased electron concentration makes hole recombination more likely. It turns out that the product of the hole concentration and

In *n*-type material, free electrons are called **majority carriers**, whereas holes are called **minority carriers**.

the free-electron concentration is constant (for a given temperature). This is known as the mass-action law,

$$pn = p_i n_i \quad (3.26)$$

where p_i is the hole concentration in intrinsic material and n_i is the electron concentration in intrinsic material. Because Equation (3.24) states that the hole and electron concentrations are equal in intrinsic material, we can write

$$pn = n_i^2 \quad (3.27)$$

Holes are continually generated by thermal energy. Each hole wanders through the material until it finally combines with a free electron. The **average lifetime** of the minority carriers is an important parameter in the switching behavior of diodes and other semiconductor devices. We denote the average lifetime of the holes in n -type material as τ_p .

p-Type Semiconductor Material

Adding a trivalent impurity such as boron to pure silicon produces **p-type material**. Each impurity atom occupies a position in the crystal lattice and forms covalent bonds with three of its nearest neighbors. The impurity atom does not have the fourth electron needed to complete the bond with its fourth neighbor. At usual operating temperatures, an electron from a nearby silicon atom moves in to fill the fourth bond of each impurity atom. This creates a hole moving freely through the crystal. However, the electron is bound to the ionized impurity atom. Thus, conduction in p -type material is due mainly to holes.

In p -type material, holes are called majority carriers and electrons are called minority carriers. Of course, this is the reverse of the terminology for n -type material.

Valence-three impurities are called **acceptors**, because they accept an extra electron. Negative charge is associated with each ionized acceptor atom—four bound electrons are present, but only enough positive charge is present in the ionic core to balance the charge of three electrons. The crystal lattice structure of p -type silicon is depicted in Figure 3.40.

In p -type material, holes are called majority carriers and electrons are called minority carriers.

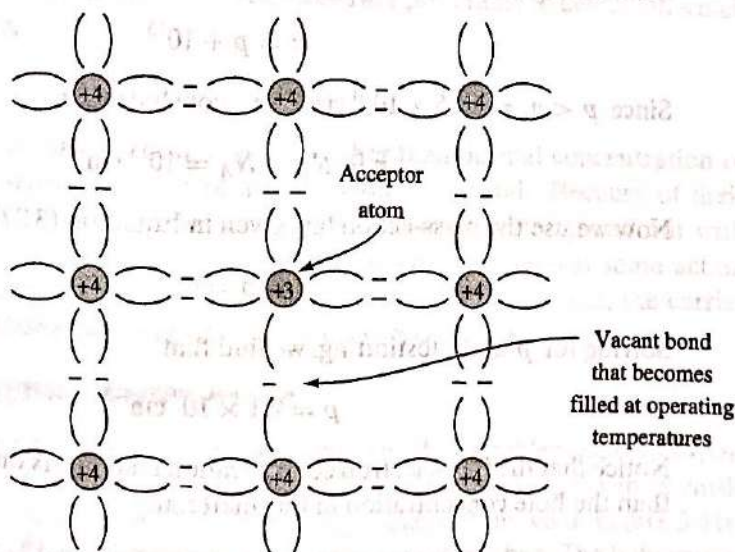


Figure 3.40
 p -type silicon is created by adding valence three impurity atoms.

If we denote the concentration of acceptor atoms as N_A , we can write

$$N_A + n = p \quad (3.28)$$

because the net charge concentration in the material must be zero. The negative charge of the ionized acceptor atoms plus that of the free electrons equals the positive charge of the holes.

Cycling the Type of the Material

In fabricating integrated circuits, it is necessary to add impurities in stages, as discussed in Section 1.3. For example, we may start with n -type material, part of which we wish to change to p -type. This is accomplished by adding acceptors. When the acceptor concentration exceeds the original donor concentration, the material becomes p -type. Later, more donors can be added to part of the p region to change it back to n -type. For materials with both types of impurities, we have

$$p + N_D = n + N_A \quad (3.29)$$

Example 3.6 Calculation of Hole and Free-Electron Concentrations

Often we state units such as atoms/cm³ (or electrons/cm³) simply as cm⁻³ because the number of atoms (or electrons) is a pure number without units.

Suppose that we have silicon with $N_A = 10^{13}$ atoms/cm³ and $N_D = 2 \times 10^{13}$ atoms/cm³. The intrinsic electron concentration of silicon at room temperature (300 K) is 1.45×10^{10} cm⁻³. Find the approximate hole and electron concentration for this doped material.

SOLUTION Because the donor concentration is greater than the acceptor concentration, we have n -type material. Thus, we anticipate that n is greater than n_i , and that p is less than n_i . Rearranging Equation (3.29), we obtain

$$n = p + N_D - N_A$$

Substituting values into this equation, we have

$$n = p + 10^{13}$$

Since $p < n_i = 1.45 \times 10^{10}$ cm⁻³, we conclude that

$$n \cong N_D - N_A = 10^{13} \text{ cm}^{-3}$$

Now we use the mass-action law given in Equation (3.27), to get

$$np = n_i^2$$

Solving for p and substituting, we find that

$$p = 2.1 \times 10^7 \text{ cm}^{-3}$$

Notice that the free-electron concentration is about six orders of magnitude greater than the hole concentration in this material. $\square$

Drift

Charge carriers move about randomly in the crystal due to thermal agitation. Collisions with the lattice cause the charge carriers to change direction frequently. The direction of travel after a collision is random. Consequently, with no applied electric field, the average velocity of the charge carriers in any particular direction is zero.

If an electric field is applied, force is exerted on the free charge carriers. (For holes, the force is in the same direction as the electric field, whereas for electrons, the force is opposite to the field.) Between collisions, the charge carriers are accelerated in the direction of the force. When the carriers collide with the lattice, their direction of travel becomes random again. Thus, the charge carriers do not keep accelerating. The net result is a constant average velocity in the direction of the force.

The average motion of the charge carriers due to an applied electric field is called **drift**. The average drift velocity is proportional to the electric field vector $\mathcal{E}$. We denote the drift velocity vector of electrons as V_n and the hole velocity vector as V_p . Thus, we can write

$$V_n = -\mu_n \mathcal{E} \quad (3.30)$$

in which the constant of proportionality μ_n is called the **mobility** of the free electrons. Because of the minus sign, the direction of the drift velocity is opposite that of the electric field.

Similarly, for holes, we have

$$V_p = \mu_p \mathcal{E} \quad (3.31)$$

For silicon at 300 K, the approximate electron mobility is $\mu_n = 1500 \text{ cm}^2/(\text{Vs})$, whereas for holes it is $\mu_p = 475 \text{ cm}^2/(\text{Vs})$. (These values are approximate—the exact values depend on the concentrations of impurities and defects in the crystal.)

For a given applied field, electrons move about three times faster than holes in silicon. Later, we will see that transistors can be fabricated such that the current is mainly carried either by holes or by electrons. For fast digital circuits and high-frequency analog circuits, devices in which conduction is due to electrons are preferable to devices in which conduction is due to holes.

For fast digital circuits and high-frequency analog circuits, devices in which conduction is due to electrons are preferable to devices in which conduction is due to holes.

Diffusion

We will see that several mechanisms can create a higher-than-normal concentration of holes or electrons in a particular region of a semiconductor crystal. Because of their random thermal velocity, a concentration of charge carriers tends to spread out with time. This causes a flow of current known as **diffusion current**. Unless some action keeps producing excess charge carriers in a particular region of the crystal, the carrier concentration tends to become uniform and diffusion current ceases.

The Shockley-Haynes Experiment

Diffusion, recombination, and drift can be demonstrated by the Shockley-Haynes experiment. In this experiment, an excess of minority charge carriers is observed in an extrinsic semiconductor. For example, consider the bar of n -type material shown in Figure 3.41a. At $t = 0$, an intense flash of light illuminates a narrow region of the bar. The light causes

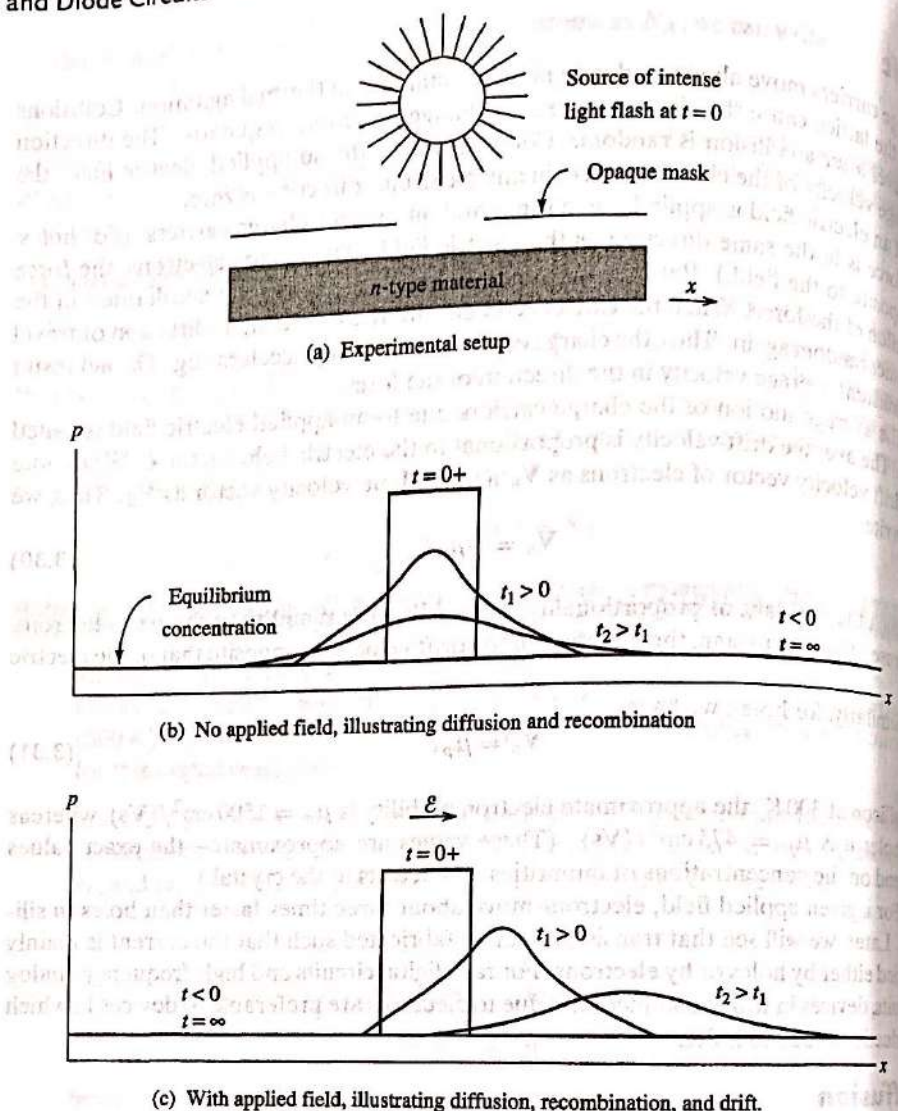


Figure 3.41 Shockley-Haynes experiment.

covalent bonds to be broken and increases the hole concentration in the illuminated portion of the bar. Figure 3.41b shows the plot of hole concentration versus x for $t = 0+$ (i.e., immediately after the flash at $t = 0$). With time, the concentration of holes spreads out due to diffusion.

Of course, the excess holes tend to recombine in addition to spreading by diffusion. Thus, the hole concentration eventually returns to its equilibrium value. The interval required for this to take place depends on the hole lifetime, τ_p .

If an external electric field is applied to the crystal, the carriers also move due to drift. (See Figure 3.41c.)

In this section, we have discussed conduction in semiconductors. Recombination, drift, and diffusion of charge carriers are important concepts in understanding device behavior. In the next section, we apply these concepts to the pn junction.

EXERCISE

3.18 Doped silicon contains 10^{16} donor atoms/cm³. Find the free-electron concentration and the hole concentration.

Answer $n \cong 10^{16}$ electrons/cm³, $p \cong 2.1 \times 10^4$ holes/cm³.

3.10 PHYSICS OF THE JUNCTION DIODE

The Unbiased pn Junction

A pn junction consists of a single crystal of semiconductor material that is doped to produce n -type material on one side and p -type on the other side. The impurities can be added to the crystal as it is grown or added later, either by diffusion of impurity atoms into the crystal or by ion implantation. It is important for the crystal lattice to join the n -side to the p -side without disruption. This is possible only if the junction is grown as a single crystal. However, it is instructive to imagine the formation of a pn junction by joining a p -type crystal to an n -type crystal.

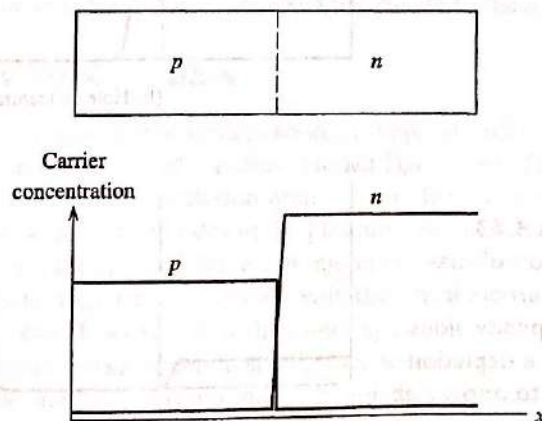
Before the two halves of the junction are joined together, the n side contains a high concentration of free electrons and a low concentration of holes. The reverse condition exists in the p -type material. Immediately after the two types of material are joined, a concentration gradient exists across the junction for both types of carriers. (See Figure 3.42.)

Charge carriers diffuse whenever a concentration gradient exists (unless some force opposes the diffusion). Consequently, after the junction is formed, holes diffuse from the p -side to the n -side, and electrons diffuse in the opposite direction. This mutual diffusion

... it is instructive to imagine the formation of a pn junction by joining a p -type crystal to an n -type crystal.

Figure 3.42

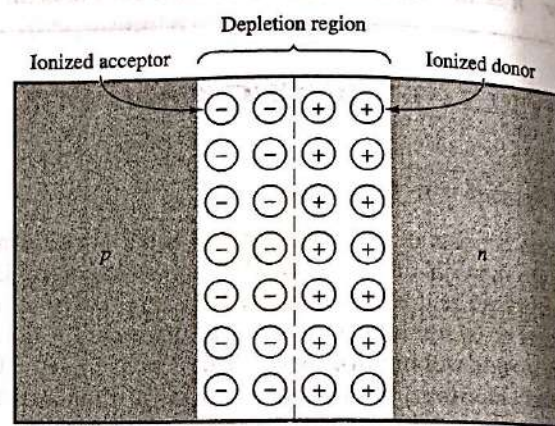
If a pn junction could be formed by joining a p -type crystal to an n -type crystal, a sharp gradient of hole concentration and electron concentration would exist at the junction immediately after joining the crystals.



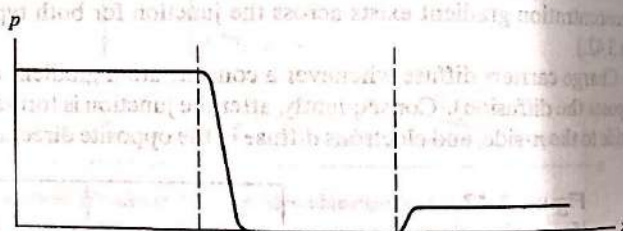
causes net negative charge to build up on the p -side of the junction (because positively charged holes are leaving and electrons are entering). Similarly, positive charge builds up on the n -side. Thus, an electric field is created in the crystal pointing from the n -side to the p -side. This field opposes further diffusion, which soon comes to a halt. After diffusing across the junction, the charge carriers become minority carriers that quickly recombine.

The result is that a **depletion region** is formed at the junction, extending a short distance into both sides. This is illustrated in Figure 3.43a. Virtually no free charge carriers exist in the depletion region. On the p -side of the depletion region, a layer of

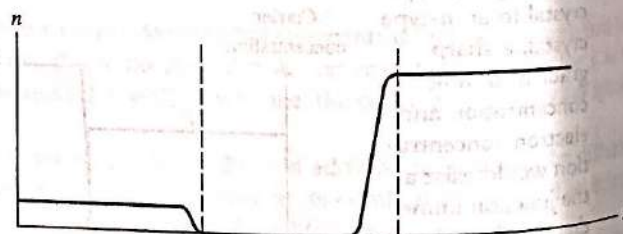
On the p -side of the depletion region, a layer of bound negative charge is present.



(a) pn junction



(b) Hole concentration



(c) Free-electron concentration

Figure 3.43
Diffusion of majority carriers into the opposite sides causes a depletion region to appear at the junction.

bound negative charge is present—the charge associated with the ionized acceptor atoms. Some of the holes that originally balanced this negative charge have crossed to the n -side, and some have combined with electrons that crossed from the n -side.

Similarly, on the n -side of the depletion region, we have a layer of bound positive charge. This is the positive charge associated with the ionized donor atoms.

In Figure 3.43a, we have shown the layer of negatively charged acceptor atoms just inside the p -side and the layer of positively charged donor atoms just inside the n -side. Of course, acceptor atoms extend throughout the p -material, but outside the depletion region their negative charge is balanced by the positive charge on the holes. Similarly, donor atoms extend throughout the n -material, and outside the depletion region their positive charge is balanced by the negative charge of the free electrons. The concentrations of holes and free electrons versus distance are illustrated in Figures 3.43b and 3.43c.

Notice that the net charge concentration and the resulting electric field are confined to the depletion region. Of course, the entire crystal is electrically neutral—the positive charge on the n -side of the depletion layer is balanced by the negative charge on the p -side.

The primary effect of the electric field in the depletion region is to repel the further diffusion of majority carriers across the junction. For example, a hole on the p -side that tries to cross the junction experiences a force pushing it back to the p -side. We say that a **built-in barrier potential** exists for the majority carriers.

An electron crossing from the n -side to the p -side loses energy to the electric field in the depletion region. Thus, the electron sees a potential-energy barrier at the junction. The height of this barrier, denoted by ϕ_0 , is typically about one electron volt. Similarly, holes on the p -side have less potential energy than holes on the n -side.

With no external voltage applied to the junction, two equal, but opposite, currents cross the junction, so that zero net current flows. One component of current is due to minority carriers on both sides of the junction that enter the depletion region. For example, holes on the n -side that enter the depletion region are pulled across to the p -side by the field. Similarly, electrons on the p -side that enter the depletion region are pulled to the n -side. This minority current is directed from the n -side to the p -side. On the other hand, particularly energetic majority carriers can cross the depletion region in opposition to the field, resulting in a current directed from the p -side to the n -side.

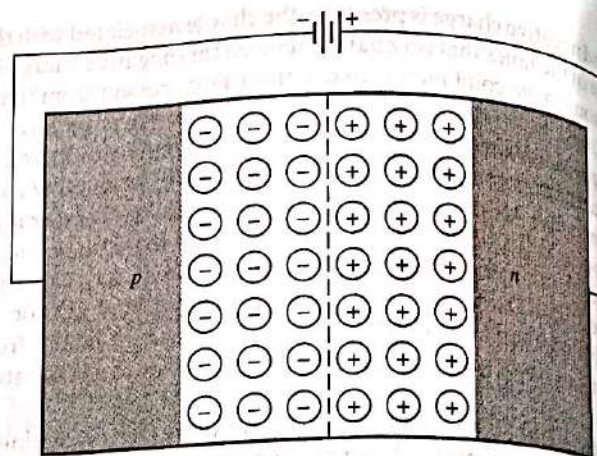
The pn Junction with Reverse Bias

A pn junction is reverse biased if an external voltage source is applied with the positive polarity on the n -side with respect to the p -side, as illustrated in Figure 3.44. The applied voltage aids the built-in barrier field in the depletion region. Thus, the majority carriers are held even more firmly on their respective sides of the junction. Because the majority carriers are pulled back from the junction, the depletion region becomes wider.

With an applied voltage greater than a few tenths of a volt, the current due to majority carriers is reduced to virtually zero. Thus, it is only the minority carriers that contribute to current under reverse bias. The reverse current is small, since few minority carriers are available. Furthermore, because the current is limited by the number of minority charge carriers, the current is almost independent of the magnitude of the reverse voltage.

... on the n -side of the depletion region, we have a layer of bound positive charge.

The primary effect of the electric field in the depletion region is to repel the diffusion of majority carriers across the junction.

**Figure 3.44**

Under reverse bias, the depletion region becomes wider.

Minority carrier concentration is maintained on both sides of the junction by thermal generation. As the temperature increases, the minority carrier concentration and reverse current increase.

The current through a pn junction is related to the applied voltage by the Shockley equation,

$$i_D = I_s \left[\exp \left(\frac{v_D}{nV_T} \right) - 1 \right]$$

Under reverse bias, v_D is negative, and if v_D is sufficiently large in magnitude, the equation yields $i_D = -I_s$. Thus, we can identify the saturation current I_s as the current carried by minority carriers crossing the junction.

The device designer can control the magnitude of I_s by selecting the degree of doping. For example, if both sides of the junction are doped very heavily, the minority carrier concentrations are very small and I_s is small. On the other hand, light doping (either on one side or on both sides) leads to higher values for I_s . Typical small-signal silicon diodes have I_s on the order of 10^{-14} A.

Besides depending on the doping levels, the value of I_s depends on the area of the junction. The value of I_s is approximately proportional to the junction area. A diode intended for high-power rectifier applications must have a large junction area to allow the dissipated power to flow away without an excessive rise in temperature. Thus, I_s is much larger for high-power devices than for small-signal devices. Furthermore, I_s increases with temperature—doubling for approximately each 5°C , due to increased thermal generation of minority carriers.

The actual reverse-bias current observed for real silicon diodes is much larger than I_s because of secondary effects for which the Shockley equation does not account—particularly the generation of carriers in the depletion region. Thus, we cannot find a value for I_s that is valid in the forward-bias region by measuring the actual reverse current. (Even though the actual reverse current is much larger than I_s , the reverse current is usually small enough to be neglected in circuit applications.)

At high currents, the ohmic voltage drop caused by current flowing through the doped semiconductor becomes significant. This drop can be taken into account by placing a

The actual reverse-bias current observed for real silicon diodes is much larger than I_s because of secondary effects for which the Shockley equation does not account.

resistance R_s in series with the junction modeled by the Shockley equation. In that case, the terminal voltage and current of the device are related by

$$v_D = nV_T \ln[(i_D/I_s) + 1] + R_s i_D \quad (3.32)$$

Typically, R_s ranges from $10\ \Omega$ to $100\ \Omega$ for small-signal devices.

This equation accounts for the series resistance of the pn junction.

The pn Junction with Forward Bias

If a positive voltage is applied to the p -side with respect to the n -side, the pn junction is forward biased. Forward bias acts in opposition to the built-in field in the depletion region. The depletion region becomes narrower, and the electric field is reduced. Thus, the built-in barrier for the majority carriers is reduced, and a large current flows across the junction.

In practice, a barrier exists even with forward bias. If sufficient forward bias were applied to reduce the barrier to zero, an excessively large current would flow, and the junction would be destroyed by overheating.

After crossing the junction, the carriers diffuse away from the junction until they combine with the majority carriers. For example, electrons on the n -side overcome the barrier and cross to the p -side, where they are minority carriers. These electrons diffuse into the p -side and eventually combine with holes.

The hole and electron concentrations versus distance for a junction under forward bias are illustrated in Figure 3.45. Notice that the hole concentration p is high in the p -type material and drops rapidly across the depletion region because the field pushes the holes back toward the p -side. On the n -side, we see a declining hole density with distance because the holes combine with electrons as they diffuse. Far from the junction on the n -side, the hole concentration is determined by the donor doping level. Similar statements apply to the electron concentration.

Part of the current carried across the junction is due to holes, and part is due to electrons. Thus, we can divide the current into hole current and electron current. The total current is the sum of the two constituents. As the distance from the junction in

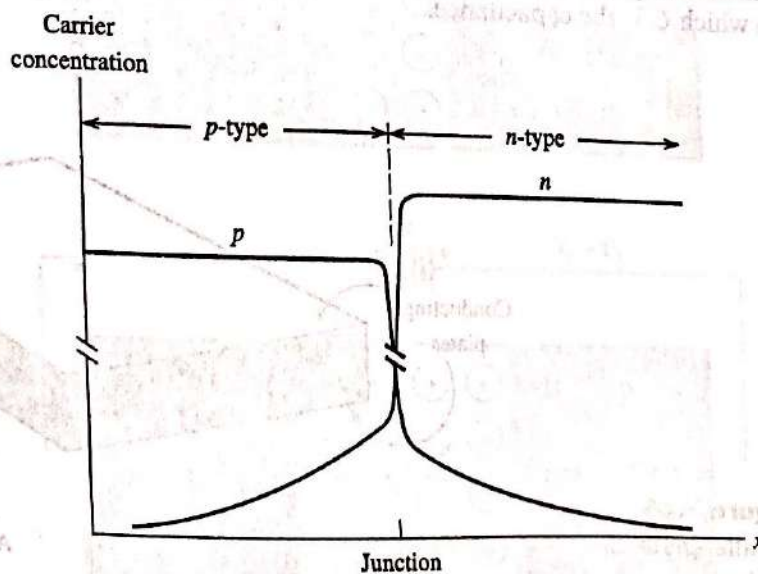


Figure 3.45
Carrier concentrations versus distance for a forward-biased pn junction.

The device designer can control the fraction of the current crossing the junction due to electrons by appropriately selecting the doping levels on the two sides of the junction.

In many applications, ... diodes that can rapidly switch between the conducting and the nonconducting states are extremely desirable.

the n -side increases, the hole concentration declines and the current is predominantly electron current. Similarly, far from the junction on the p -side, the current becomes predominantly hole current.

The device designer can control the fraction of the current crossing the junction due to electrons by appropriately selecting the doping levels on the two sides of the junction. For example, if the n -side is doped very heavily compared with the p -side, the current crossing the junction is due mostly to electrons. On the other hand, if the p -side is doped more heavily, the current at the junction is mostly hole current. This point will be important in Chapter 4, when we consider bipolar transistors.

3.11 SWITCHING AND HIGH-FREQUENCY BEHAVIOR

We have seen that the pn junction conducts little current when it is reverse biased and easily conducts large current when it is forward biased. In many applications, such as high-speed logic circuits and high-frequency rectifiers, diodes that can rapidly switch between the conducting and the nonconducting states are extremely desirable.

Unfortunately, the pn junction displays two charge-storage mechanisms that slow switching. Both of these mechanisms can be modeled as nonlinear capacitances. Before we consider charge storage in pn junctions, we briefly review conventional linear capacitors.

Review of Capacitance

A capacitor is constructed by separating two conducting plates by an insulator. (See Figure 3.46.) If voltage is applied to the capacitor terminals, charge flows in and collects on one plate. Meanwhile, current flows out of the other terminal, and a charge of opposite polarity collects on the other plate.

The magnitude of the net charge Q on one plate is proportional to the applied voltage V . Thus, we have

$$Q = CV \quad (3.33)$$

in which C is the capacitance.

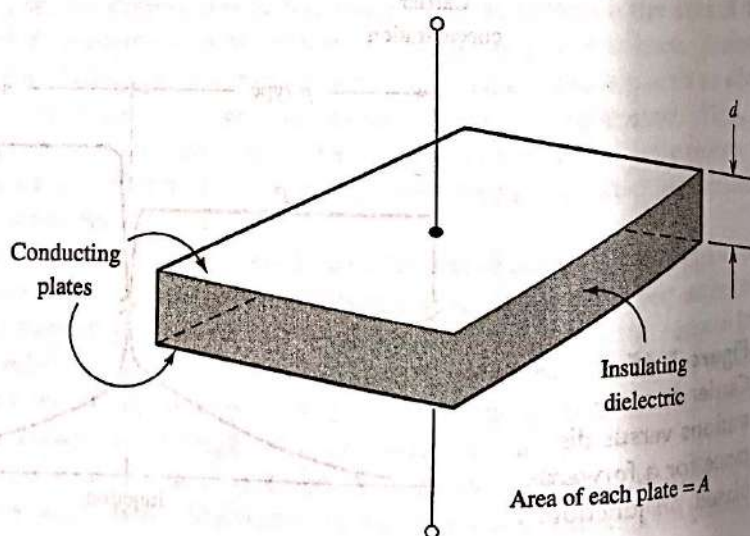


Figure 3.46
Parallel-plate capacitor.

For a parallel-plate capacitor, such as that shown in Figure 3.46, the capacitance is given by

$$C = \frac{\epsilon A}{d} \quad (3.34)$$

where A is the area of one plate, d is the distance between the plates, and ϵ is the dielectric constant of the material between the plates. Often, the dielectric constant is expressed as

$$\epsilon = \epsilon_r \epsilon_0 \quad (3.35)$$

where ϵ_r is the relative dielectric constant and $\epsilon_0 \cong 8.85 \times 10^{-12} \text{ F/m}$ is the dielectric constant for a vacuum. [Actually, Equation (3.34) is an approximation that is accurate only if d is much smaller than the width and the length of the plates.]

Notice especially that the capacitance of the parallel-plate capacitor is proportional to the area of the plates and inversely proportional to the distance between the plates.

Depletion Capacitance

Consider the pn junction under reverse bias. As the magnitude of the voltage applied to the junction is increased, the field in the depletion region becomes stronger and the majority carriers are pulled back farther from the junction. This is illustrated in Figure 3.47.

The charge in the depletion region is similar to the charge stored on a parallel-plate capacitor. Unlike the situation with the parallel-plate capacitor, however, each additional increment of charge stored in the depletion region is separated by a larger distance. Thus,

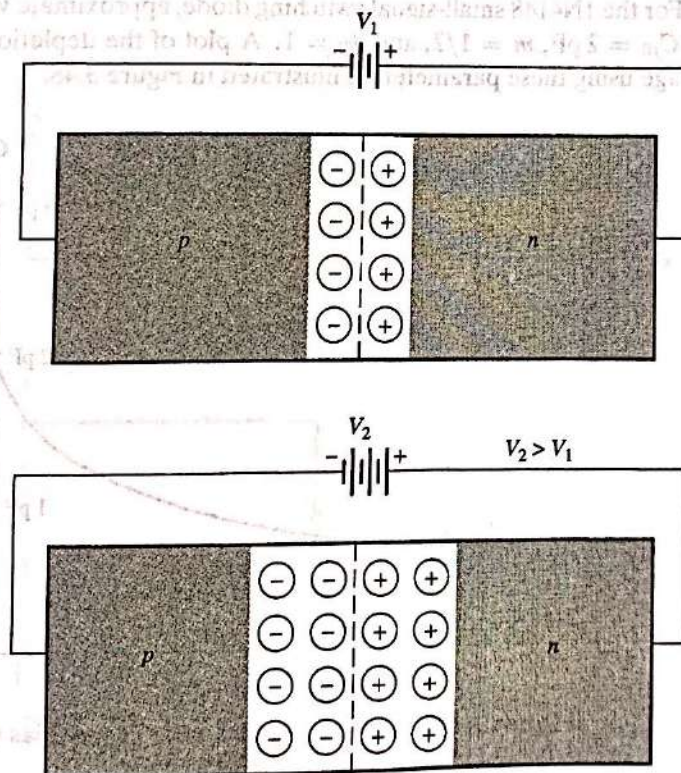


Figure 3.47

As the reverse bias voltage becomes greater, the charge stored in the depletion region increases.

the reverse-biased junction behaves as a capacitor, but the **depletion capacitance** is not constant. In other words, the stored charge is not directly proportional to the applied voltage. Because the relationship between the stored charge and the applied voltage is not linear, we say that the depletion capacitance is nonlinear.

For this nonlinear depletion capacitance, we define the incremental capacitance as

$$C_J = \left| \frac{dQ}{dv_D} \right| \quad (3.36)$$

in which dQ is the differential of the charge stored on one side of the depletion region and dv_D is the differential voltage. (This is similar to the concept of the dynamic resistance of a diode discussed in Section 3.8.) C_J is the capacitance of the diode for a small ac signal superimposed on a dc Q -point.

The incremental depletion capacitance is

$$C_J = \frac{C_{J0}}{[1 - (V_{DQ}/\phi_0)]^m}, \quad (3.37)$$

in which C_{J0} is the incremental depletion capacitance for zero bias, V_{DQ} is the operating-point (Q -point) voltage (which is negative for reverse bias), ϕ_0 is the built-in barrier potential (typically about one volt), and m is called the grading coefficient. The value of m depends on how the doping changes with distance across the junction. For a linear change in doping across the junction, $m = 1/3$, and for an abrupt junction, $m = 1/2$.

For the 1N4148 small-signal switching diode, approximate values of these parameters are $C_{J0} = 2$ pF, $m = 1/2$, and $\phi_0 = 1$. A plot of the depletion capacitance versus bias voltage using these parameters is illustrated in Figure 3.48.

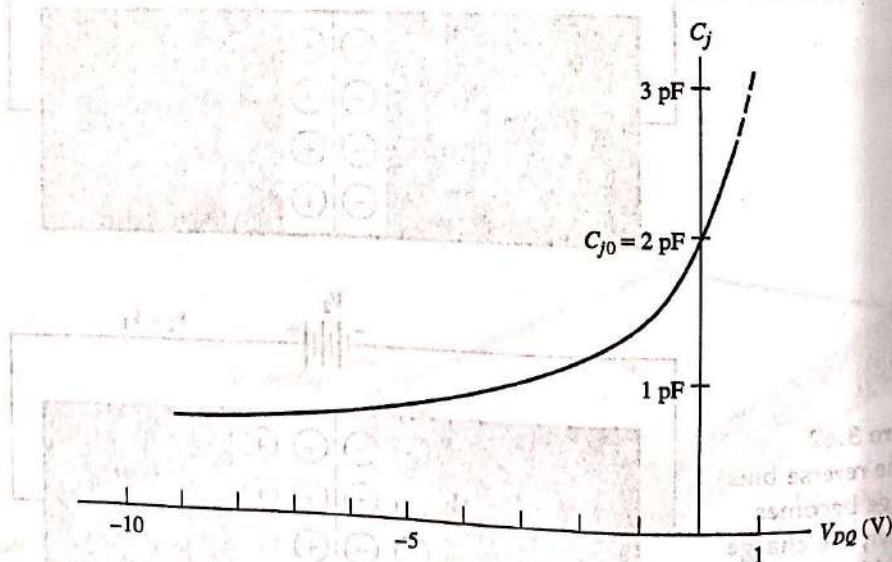


Figure 3.48 Depletion capacitance versus bias voltage for the 1N4148 diode.

Key equation for incremental (small-signal) depletion capacitance.

The zero-bias depletion capacitance C_{j0} is approximately proportional to the area of the junction. Thus, it is larger for high-power rectifiers, which must be physically large to accommodate high power dissipation.

The value of C_{j0} also depends on the doping levels. In highly doped junctions, a large amount of charge can be stored close to the junction—as in a parallel-plate capacitor with a small plate separation. Thus, C_{j0} is relatively large for highly doped junctions and small for lightly doped junctions.

Diffusion Capacitance

Another basic charge-storage mechanism occurs when the pn junction is forward biased. To simplify our discussion, we consider an abrupt junction with much heavier doping on the p -side than on the n -side. (i.e., $N_A \gg N_D$) Sometimes this is called a p^+n junction, where p^+ refers to heavy doping of the p -material. For such a diode under forward bias, the current crossing the junction is due mainly to holes crossing from the p -side to the n -side.

Consider the hole concentration of the forward-biased p^+n junction shown in Figure 3.49. The charge associated with the holes that have crossed the junction is stored charge and is represented by the shaded areas in the figure. As the forward current is

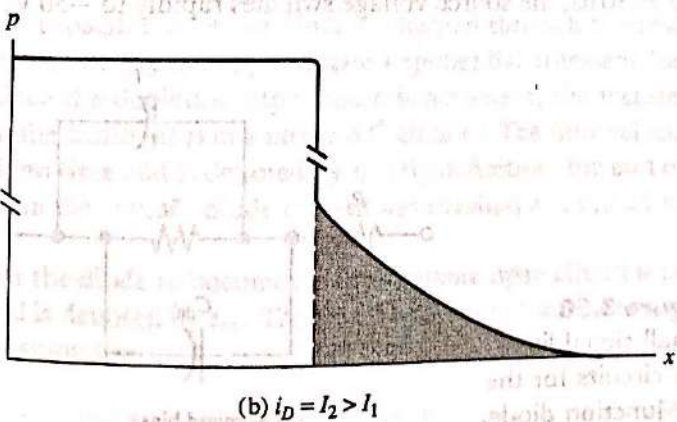
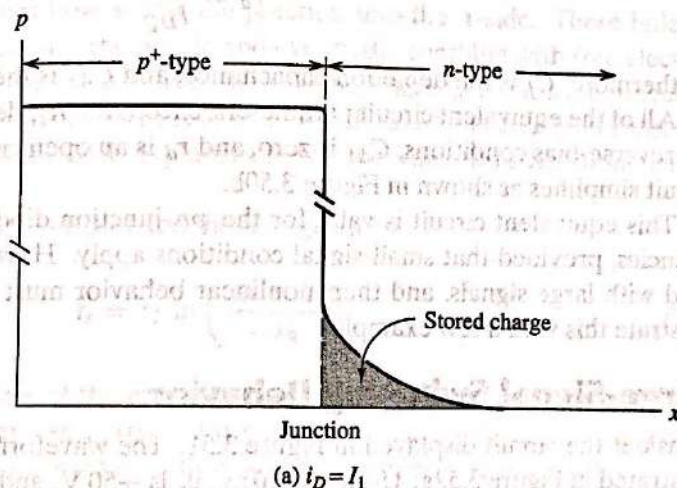


Figure 3.49
Hole concentration versus distance for two values of forward current.

increased, more holes cross the junction and the stored charge increases. Because this charge is associated with the holes that are diffusing into the n -side of the junction, we call the effect **diffusion capacitance**.

The incremental diffusion capacitance is given approximately by

$$C_{\text{dif}} = \frac{\tau_T I_{DQ}}{V_T} \quad (3.38)$$

in which τ_T is a parameter known as the **transit time** of the minority carriers. For the p^+n junction, $\tau_T = \tau_p$ is the lifetime of the holes on the n -side of the junction. On the other hand, for a pn^+ junction, we have $\tau_T = \tau_n$, which is the lifetime of the free electrons on the p -side. For a junction with comparable doping levels, τ_T is a weighted average of both lifetimes. Finally, I_{DQ} is the Q -point diode current, and as before, $V_T = kT/q$.

Complete Small-Signal Diode Model

A small-signal equivalent circuit for the pn -junction diode under forward bias is shown in Figure 3.50a. The resistance R_s represents the ohmic resistance of the bulk material on both sides of the junction. r_d is the dynamic resistance of the pn junction discussed in Section 3.8, where we saw that

$$r_d = \frac{nV_T}{I_{DQ}}$$

Furthermore, C_j is the depletion capacitance, and C_{dif} is the diffusion capacitance.

All of the equivalent circuit parameters, except for R_s , depend on the bias point. Under reverse-bias conditions, C_{dif} is zero, and r_d is an open circuit. Hence, the equivalent circuit simplifies as shown in Figure 3.50b.

This equivalent circuit is valid for the pn -junction diode over a wide range of frequencies, provided that small-signal conditions apply. However, diodes are most often used with large signals, and their nonlinear behavior must be taken into account. We illustrate this with a few examples.

Large-Signal Switching Behavior

Consider the circuit displayed in Figure 3.51. The waveform of the source voltage v_s is illustrated in Figure 3.52a. Until $t = 10$ ns, v_s is +50 V, and the diode is forward biased. At $t = 10$ ns, the source voltage switches rapidly to -50 V, reverse biasing the diode.

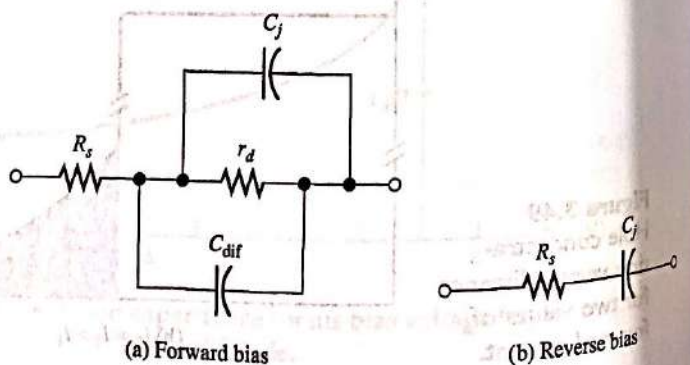
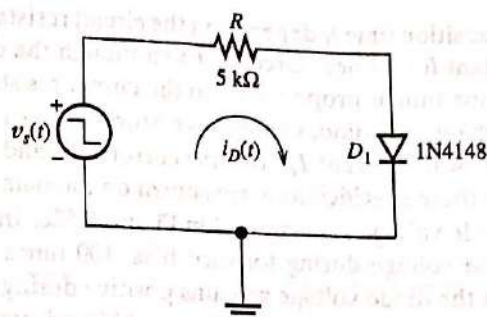


Figure 3.50
Small-signal linear circuits for the pn -junction diode.

Figure 3.51
Circuit illustrating
switching behavior
of a *pn*-junction
diode.



The resulting diode current is shown in Figure 3.52b. As we might expect, the diode current is approximately $50\text{ V}/5\text{ k}\Omega = +10\text{ mA}$ until $t = 10\text{ ns}$. Then the source voltage jumps to -50 V . Instead of dropping immediately to zero, the diode current reverses to $I_R \cong -10\text{ mA}$. At approximately $t = 18\text{ ns}$, the current begins to fall in magnitude and approaches zero at $t = 25\text{ ns}$. In the interval immediately after the source reverses polarity, the diode continues to act as if it were forward biased. This is called the **storage interval** t_s , as labeled in Figure 3.52b.

We can explain the behavior of the diode as follows. (To simplify the discussion, we assume a diode that is heavily doped on the *p*-side compared with the *n*-side.) When forward bias is applied, holes flow across the junction into the *n*-side. These holes are minority carriers that diffuse into the *n*-side and eventually combine with free electrons. When v_s reverses polarity, the holes stored on the *n*-side can again cross the junction to the *p*-side. Until the supply of excess holes on the *n*-side is exhausted, the current flows easily in the reverse direction. This explains the storage interval of the diode-current waveform.

The storage interval for a *pn*-junction diode is given by

$$t_s = \tau_T \ln \left(\frac{I_F - I_R}{-I_R} \right) \quad (3.39)$$

in which τ_T is the transit time of the minority carriers. I_F is the forward current before switching, and I_R is the reverse current during the storage interval. Notice that the current is referenced in the forward direction, and I_R assumes a negative value.

After the excess holes have all recrossed the junction (or combined with free electrons on the *n*-side), the depletion capacitance of the diode is charged through the resistor. Thus, after the storage interval, we see an approximate exponential transient for the current in Figure 3.52b. (Since the depletion capacitance is nonlinear, the transient is not precisely exponential, as the transient is in a linear *RC* circuit.) The interval for this transient is called the **transition time** and is denoted by t_t . (By definition, the end of the transition interval occurs when the reverse diode current has reached a specified value, typically $I_R/10$.)

The total time interval for the diode to become an approximate open circuit is called the **reverse recovery time** and is denoted by t_{rr} . The reverse recovery time is the sum of the storage time and the transition time:

$$t_{rr} = t_s + t_t \quad (3.40)$$

The transition time t_t depends on the circuit resistance. (Recall the concept of the RC time constant for a linear circuit.) Even though the depletion capacitance is not linear, the transition time is proportional to the circuit resistance.

Data sheets for diodes often give storage times and reverse recovery times for a specified forward current I_F , reverse current I_R , and circuit resistance. Usually, the test circuits for these specifications are shown on the data sheet.

The diode voltage is illustrated in Figure 3.52c. In order to be able to see the details of the diode voltage during forward bias, 100 times the diode voltage is also plotted. Notice that the diode voltage remains positive during the storage time, showing that the diode continues to act as if it were forward biased, even though the current has reversed direction.

The terminal voltage of the diode does fall somewhat when the current reverses, because the voltage drop across the ohmic resistance R_s of the diode reverses polarity. Prior to $t = 10$ ns, the terminal voltage is the sum of the junction voltage and the ohmic

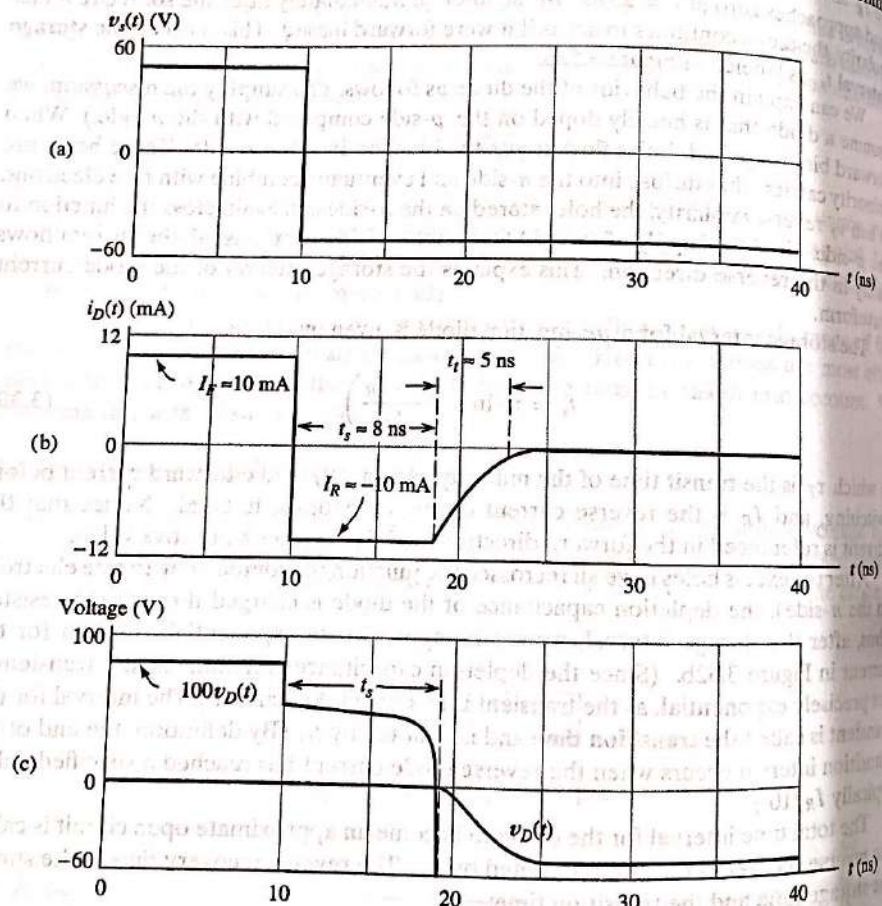


Figure 3.52 Waveforms for the circuit of Figure 3.51.

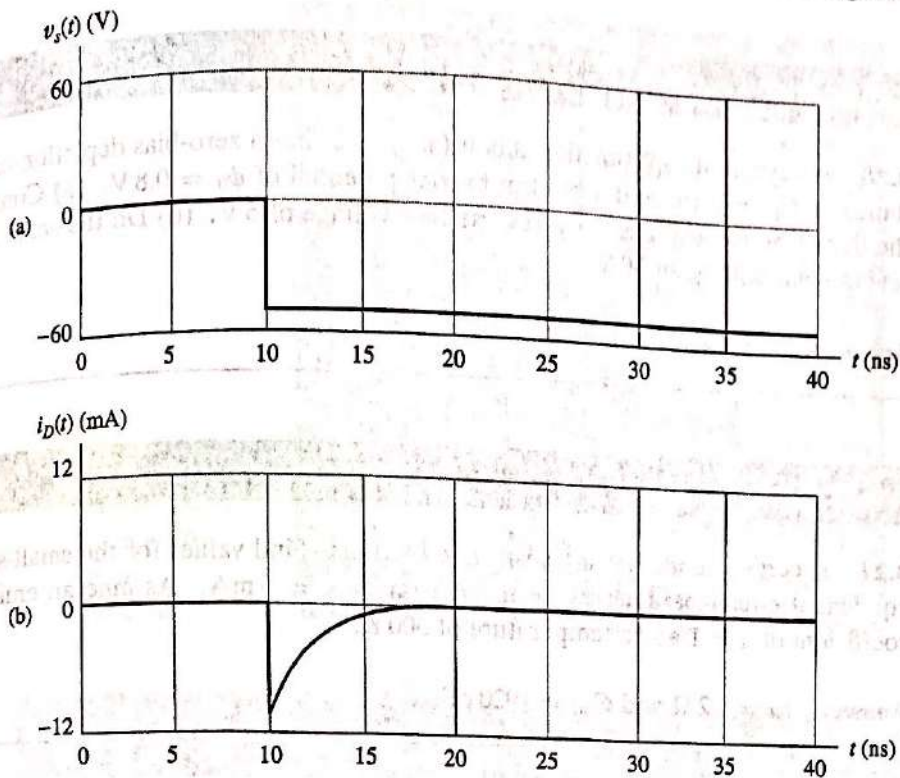


Figure 3.53 Another set of waveforms for the circuit of Figure 3.51. Notice the absence of a storage interval.

drop. On the other hand, between $t = 10$ ns and $t = 18$ ns, the terminal voltage is the junction voltage minus the ohmic drop.

It is instructive to consider another source voltage waveform for the circuit of Figure 3.51. For example, Figure 3.53a shows a source voltage that is zero until $t = 10$ ns. Then it switches to -50 V. The corresponding diode current is illustrated in Figure 3.53b. In this case, because the diode current is zero prior to $t = 10$ ns, there is no excess hole concentration on the n -side of the junction. Therefore, there is no storage interval. The diode immediately enters the transition phase, and it switches to an open circuit much more quickly if the forward current is zero before switching.

EXERCISE

3.19 Consider the parallel-plate capacitor shown in Figure 3.46. The plates have dimensions of $20 \mu\text{m} \times 30 \mu\text{m}$. The relative dielectric constant of the material between the plates is $\epsilon_r = 11.9$ (the value for silicon). The capacitance is 1 pF, a typical zero-bias depletion capacitance for a discrete small-signal diode. Find the distance between the plates. (The answer is the approximate zero-bias thickness of the depletion region.)

Answer $d = 6.32 \times 10^{-8} \text{ m}$.

EXERCISE

3.20 A certain abrupt-junction diode ($m = 1/2$) has a zero-bias depletion capacitance of $C_{j0} = 5 \text{ pF}$ and a built-in barrier potential of $\phi_0 = 0.8 \text{ V}$. (a) Compute the depletion capacitance for a reverse-bias voltage of 5 V . (b) Do the same for a reverse-bias voltage of 50 V .

Answer (a) $C_j = 1.86 \text{ pF}$; (b) $C_j = 0.627 \text{ pF}$.

EXERCISE

3.21 A certain diode has a transit time of 10 ns . Find values for the small-signal equivalent circuit parameters r_d and C_{dif} at $I_{DQ} = 5 \text{ mA}$. Assume an emission coefficient of $n = 1$ and a temperature of 300 K .

Answer $r_d = 5.2 \Omega$ and $C_{\text{dif}} = 1920 \text{ pF}$.

3.12 COMPUTER-AIDED ANALYSIS OF DIODE CIRCUITS

In this section, we show several examples of how to use SPICE to analyze diode circuits.

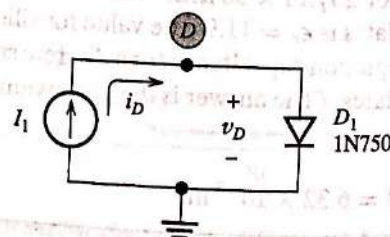
Example 3.7 Plotting V - I Diode Characteristics with SPICE

Obtain a plot of the room-temperature volt-ampere characteristic of the 1N750 Zener diode for currents ranging from -10 mA to 10 mA . The 1N750 has a breakdown voltage of approximately 4.7 V . Repeat for temperatures of $0, 25, 50, 75$, and 100°C .

SOLUTION First we start Schematics and draw a circuit containing a dc current source and a 1N750 diode. The resulting circuit is shown in Figure 3.54. Then

Figure 3.54

Circuit used to display the V - I characteristics of the 1N750 Zener diode.



The circuit file is named Fig3_54 and is found on the website.

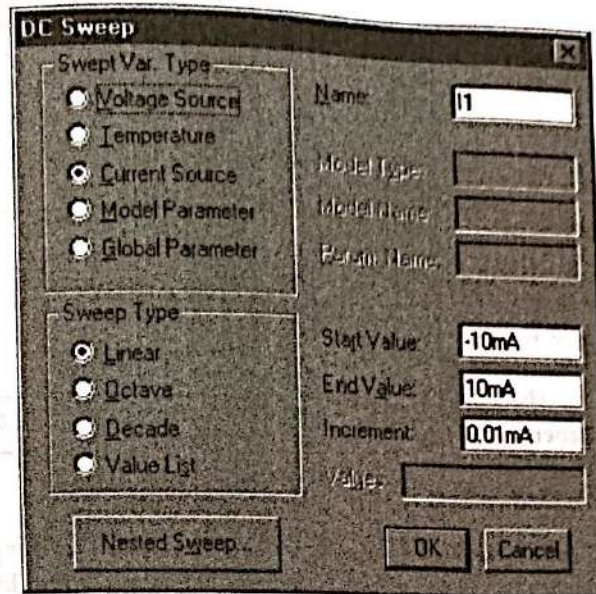


Figure 3.55
Dc-sweep-
setup
window.

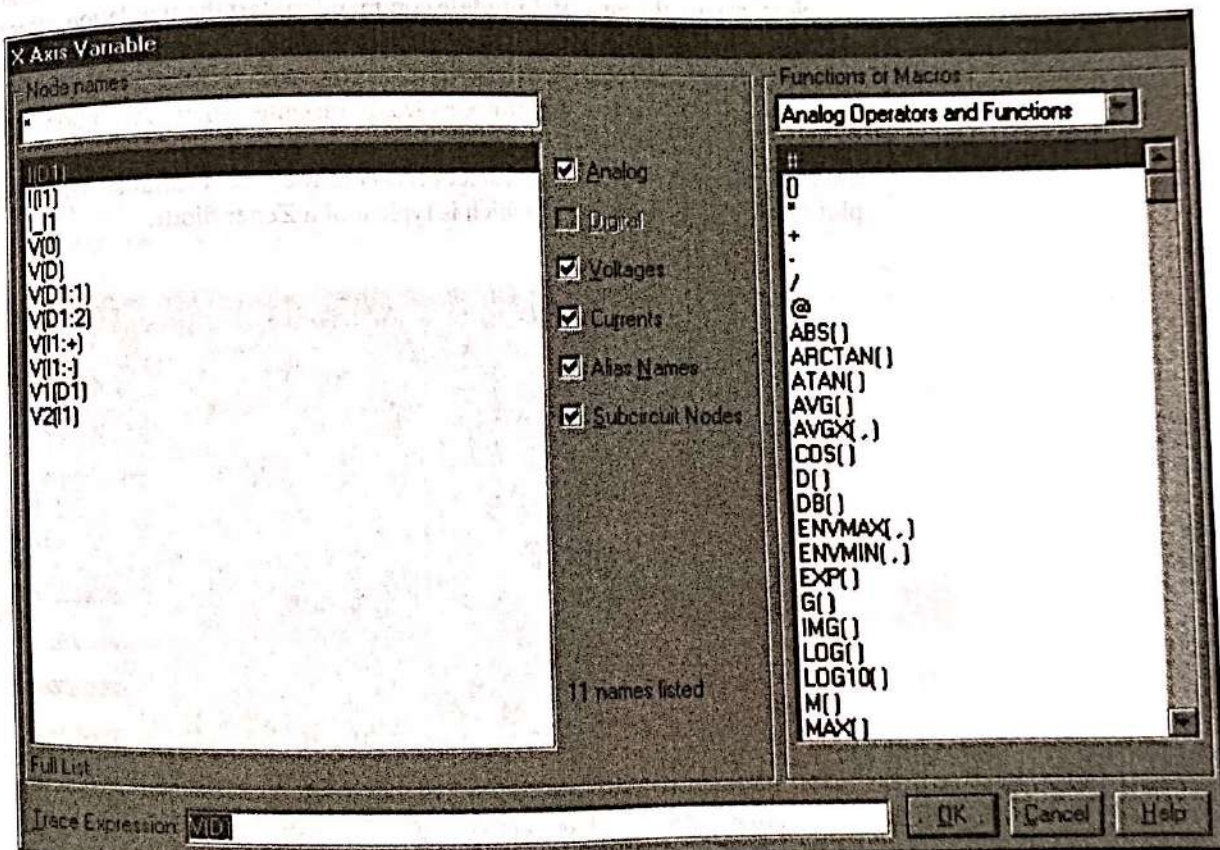
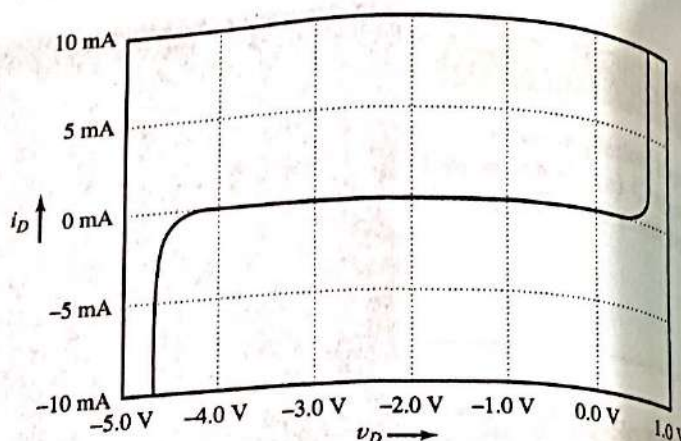


Figure 3.56 X-axis-variable window.

Figure 3.57
SPICE generated plot for
the 1N750
Zener diode
at 25°C.



we use the **analysis/setup/dc sweep** commands to bring up the window shown in Figure 3.55. In this window, we give the name of the dc source that we wish to vary and the range of current values. Notice that we have selected a linear sweep.

Next, we use the **analysis/simulate** command to start the simulation, after which Probe starts. Since we have swept the current source, Probe comes up with current on the x-axis. However, we want to plot the current on the y-axis and voltage on the x-axis. Thus, we use the **plot/x-axis/axis variable** commands to bring up the window shown in Figure 3.56. Then we choose $V(D)$ as the variable. Next, we use the **trace/add** command and select $I(D1)$ as the y-axis variable. This yields the plot displayed in Figure 3.57, which is typical of a Zener diode.

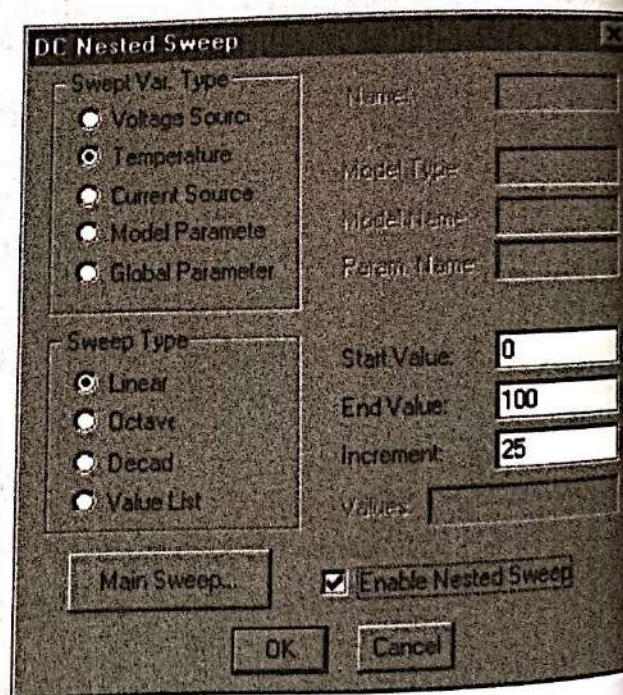


Figure 3.58
Dc-nested-
sweep win-
dow.

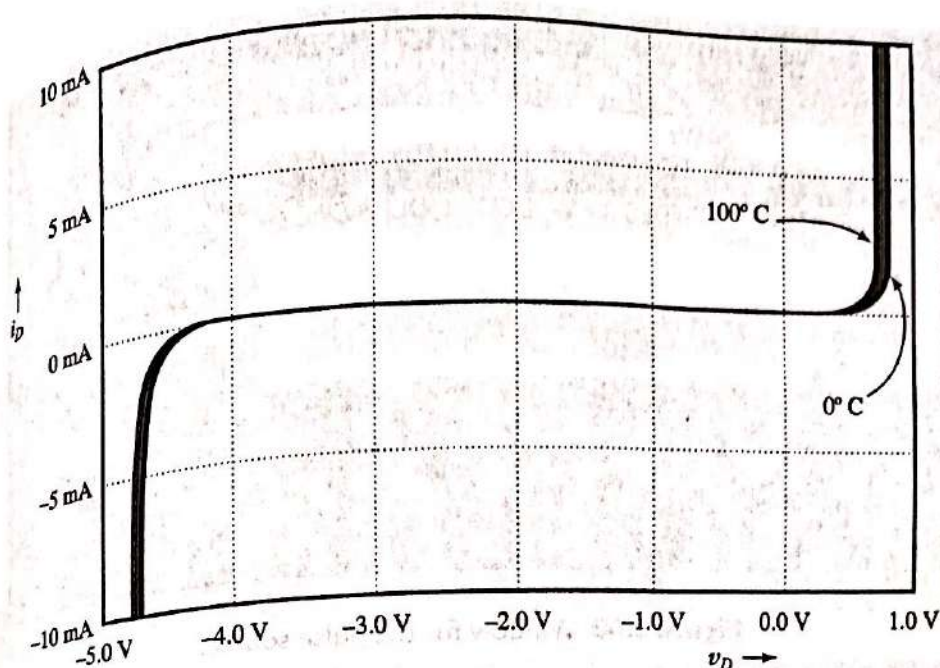


Figure 3.59 1N750 characteristics for temperature ranging from 0 to 100°C in 25° increments.

To obtain a family of plots for various temperatures, we return to Schematics and use the **analysis/setup/dc sweep/nested sweep** commands to bring up the window illustrated in Figure 3.58. We select temperature as the nested sweep variable, and we choose the linear sweep type and the desired range of temperatures. *Be sure to enable the nested sweep.* Then if we return to Schematics and use the **analysis/simulate** command, the circuit is simulated for each temperature and Probe comes up. As before, we change the x-axis variable to V(D) and select I(D1) as the trace. The family of plots is displayed in Figure 3.59. □

Example 3.8 Switching Behavior of the 1N4148 Diode

Use DesignLab to simulate the circuit of Figure 3.51. Compare your results with those shown in Figure 3.52.

SOLUTION First we use Schematics to draw the circuit (Figure 3.51). Then we double click the left button of the mouse on the voltage source symbol to bring up the window displayed in Figure 3.60. To set up the pulse waveform of Figure 3.52a, we need to specify the attributes as $V1 = 50$ V, $V2 = -50$ V, and $TD = 10$ ns. Next, we use the **analysis/setup/transient** command to bring up the

The circuit file is named Fig3_51 and can be found on the website.

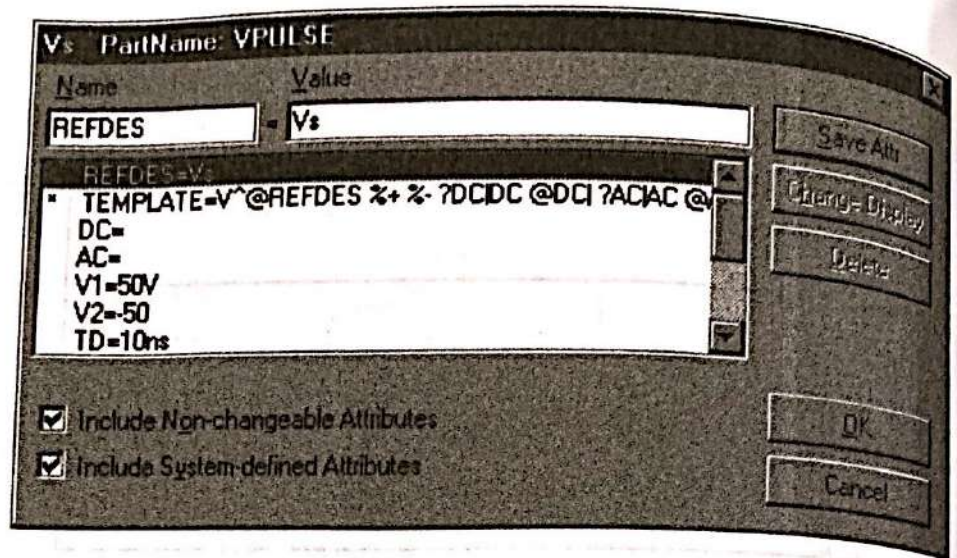


Figure 3.60 Window for the pulse source.

window illustrated in Figure 3.61. We select a final time of 40 ns and a step of 0.1 ns. After using the **analysis/simulate** command, Probes starts and we select **I(D1)** as the variable to plot. The resulting plot is identical to Figure 3.52b.

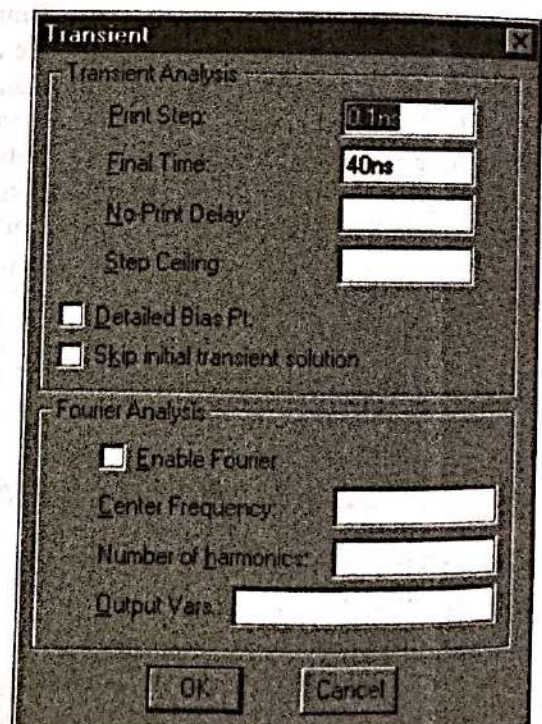


Figure 3.61
Transient
setup win-
dow.

Almost all of the circuits discussed in this book can be simulated by using DesignLab or similar software packages. Intelligent use of computer simulation can help you become an expert electronic-circuit designer. Select a circuit, think about how it works, then simulate it, and compare the results with your expectations. When the results agree, try a more complex circuit; when they don't, rethink your understanding of the circuit. After you have some experience with existing circuits, start designing your own.

Intelligent use of computer simulation can help you become an expert electronic-circuit designer.

EXERCISE

3.22 Use SPICE to obtain the volt-ampere characteristic of the 1N4148 diode.

EXERCISE

3.23 Use SPICE to simulate the circuit of Figure 3.51 for the source waveform shown in Figure 3.53a. Plot the diode current against time.

Answer The result should be very similar to Figure 3.53b. Some variation may occur depending on the diode model.

SUMMARY

- Diodes are two-terminal devices that conduct current easily in one direction, but not in the other.
- At room temperature, a small-signal silicon diode has a voltage of approximately 0.6 V when carrying current in the forward direction. As the temperature increases, the forward voltage decreases by about 2 mV/K. Under reverse bias, the current is very small, typically 1 nA. A rule of thumb is that the reverse current doubles for each 10-K increase in temperature. Eventually, if sufficient reverse voltage is applied, the diode enters the reverse-breakdown region.
- Diodes that are intended to operate in the breakdown region are called Zener diodes. Zener diodes are often used in applications for which a constant voltage in breakdown is desirable.
- Circuits containing a nonlinear device such as a diode can be analyzed using a graphical technique called a load-line analysis. The load-line equation is obtained by applying KVL or KCL. The equation plots as a straight line that can be drawn by locating two points.
- The ideal-diode model is a short circuit for forward currents and an open circuit for reverse voltages.

- Rectifier circuits are useful in battery-charging circuits and for converting ac into nearly constant dc to power electronic circuits such as amplifiers. Transformers are used to adjust the ac voltage to the value needed. Half-wave and several full-wave circuits can be used.
- The reverse-breakdown voltage of the diodes used in a rectifier must exceed the expected PIV of the circuit.
- Waveshaping circuits transform one waveform into another. Examples are clipping and clamp circuits.
- AND and OR logic gates can be constructed from diodes, resistors, and voltage sources. However, diode logic gates have two drawbacks: First, they produce output levels that are not as well separated as the input voltage levels; second, a practical diode logic inverter does not exist.
- Operating from variable supplies, voltage regulators supply nearly constant voltages to loads. Percentage source regulation and load regulation are important specifications for a voltage regulator.
- The analysis of nonlinear electronic circuits is often accomplished in two steps: First, the dc operating point is determined, and a linear small-signal equivalent circuit is found for the nonlinear devices; second, the equivalent circuit is analyzed.
- At low frequencies, The small-signal equivalent circuit of a diode is its dynamic resistance, which is equal to the inverse slope of the diode characteristic, evaluated at the operating point.
- The Shockley equation relates the voltage and current in a pn junction. Secondary effects result in higher reverse current than that predicted by the equation. For large forward current, the equation becomes inaccurate due to ohmic drop across the series resistance.
- Silicon forms a crystal in which each atom develops covalent bonds with its four nearest neighbors. At normal temperatures, a small fraction of the bonds are broken, producing holes and free electrons that can carry current. The hole and free-electron concentrations are equal in pure silicon. As temperature increases, the carrier concentrations and the conductivity increase.
- Adding donor (valence-five) impurities to silicon produces an n -type material, in which conduction is due mainly to free electrons. Holes (minority carriers) are produced by thermal generation and eventually recombine with electrons.
- Adding acceptor (valence-four) impurities to silicon produces p -type material, in which conduction is due mainly to holes.
- According to the mass-action law, the product of the free-electron concentration and the hole concentration is a constant that is independent of the doping. Thus, as the concentration of one type of carrier increases, the concentration of the other type decreases.
- Silicon can be cycled from n -type to p -type and back several times by alternately adding donor and acceptor impurities. This is necessary in the fabrication of inte-

grated circuits. For material with both types of impurities, we can write

$$p + N_D = n + N_A$$

- Carriers move through a semiconductor by diffusion when a concentration gradient exists. Carriers move from regions of high concentration, to regions of low concentration.
- When an electric field is applied, the carriers move by drift.
- Electrons diffuse and drift more rapidly in silicon than holes do. Hence, for rapid response, devices in which current is carried by free electrons are preferred.
- In a pn junction, a depletion region appears at the junction, with a layer of net positive charge just inside the n -side and a layer of negative charge on the p -side. These charge layers set up an electric field barrier that tends to hold the majority carriers on their respective sides of the junction. Equal and opposite currents cross the junction. One component is due to minority, the other to majority, carriers.
- Under reverse bias, the junction barrier becomes larger, stopping the majority carrier current. The reverse current is due to minority carriers and second-order effects.
- Under forward bias, the junction barrier becomes smaller, and the majority carrier current increases dramatically.
- The current in a pn junction is given by the Shockley equation,

$$i_D = I_s \left[\exp \left(\frac{v_D}{nV_T} \right) - 1 \right]$$

- Depletion capacitance is associated with charge storage in the depletion region. Diffusion capacitance results from minority carriers stored on opposite sides of the junction under forward bias. Both capacitances are nonlinear. The high-frequency equivalent circuit for the pn junction is illustrated in Figure 3.50.
- Charge-storage effects slow diode switching. If a junction has been forward biased, it conducts well in the reverse direction until the minority carrier concentration is depleted on the two sides of the junction.
- Computer-aided analysis is a powerful tool for circuit design.

PROBLEMS

Section 3.1: Diode Characteristics

- 3.1. Draw the circuit symbol for a diode. Label the anode and cathode.
- 3.2. Draw the volt-ampere characteristic of a typical small-signal diode to scale, and label the various regions.
- 3.3. What is a Zener diode? For what is it typically used? What are two other names for it? Sketch the volt-ampere

characteristic to scale for a 5.6-V Zener diode (i.e., a Zener diode having a reverse-breakdown voltage of 5.6 V).

3.4. Recall that the forward voltages of small-signal silicon diodes decrease about 2 mV/K. Such a diode has a voltage of 0.600 V, with a current of 1 mA at a temperature of 25°C. Find the diode voltage at 1 mA and a temperature of 175°C.

3.5. Sketch i against v to scale for the circuits shown in Figure P3.5. The diodes are typical small-signal silicon devices at 300 K. The reverse-breakdown voltages of the Zener diodes are shown. Assume 0.6 V for all diodes (including Zeners) in

the forward-bias region.

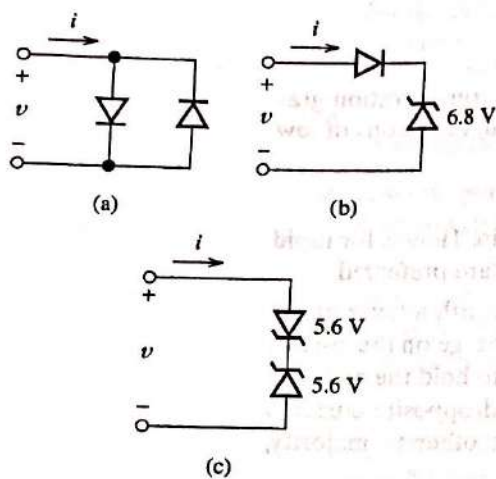


Figure P3.5

3.6. Consider the circuit shown in Figure P3.6. Assume that the reverse diode current is independent of the reverse voltage. If $v_o = 0.5$ V at a temperature of 70°C , estimate its values at 50°C and at 100°C . (Hint: A rule of thumb is that the reverse current doubles for each 10-K increase in temperature.)

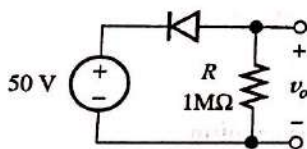


Figure P3.6

3.7. A certain diode is at a temperature of 25°C . Suddenly, a forward current of 100 mA is applied, and the voltage becomes 0.65 V. After several minutes, the diode warms due to its power dissipation, and the voltage is 0.45 V. Estimate the diode temperature.

3.8. Sometimes we may want to obtain a reference voltage by combining ordinary diodes in series, rather than using a Zener diode. How many diodes must be placed in series to obtain a 3-V reference voltage? Assume that each diode has a forward drop of 0.6 V. By what percentage does this voltage change when the temperature increases by 10°C ?

Section 3.2: Load-Line Analysis

3.9. Use graphical load-line analysis to find the currents and voltages labeled in the circuits shown in Figure P3.9. The device characteristics are illustrated in Figures P3.9d and e.

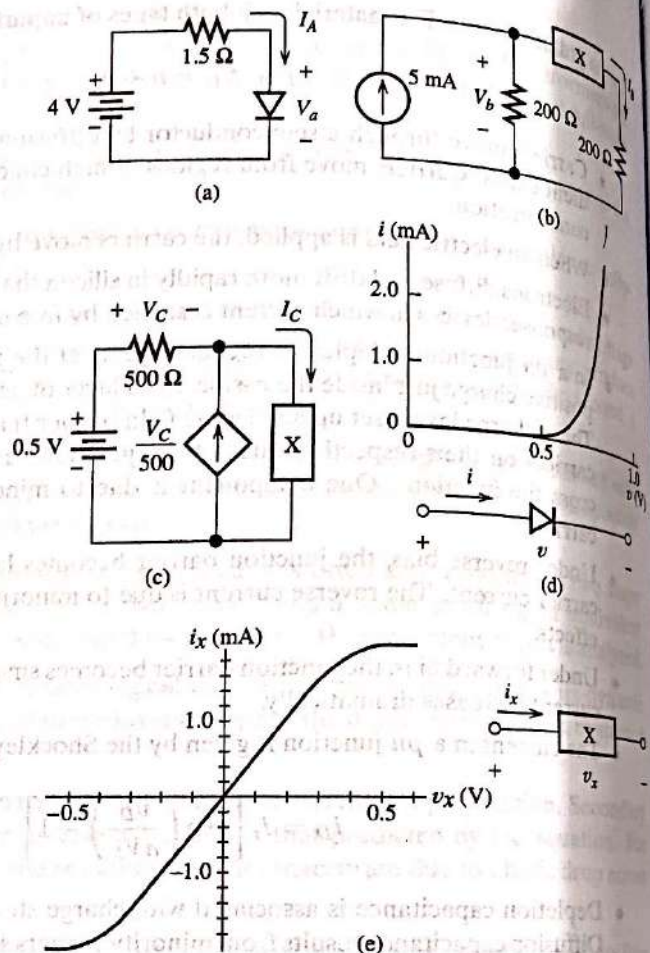


Figure P3.9

3.10. Consider the circuit of Figure 3.4. Draw the load line for the circuit for a 1-V source and $R = 500 \Omega$. Repeat for a 0.5-V source and $R = 500 \Omega$. Does the slope of the load line change when the source voltage changes? Find an expression for the slope of the load line in terms of the circuit resistance R .

3.11. Sketch the load line to scale on the i_D - v_D axes for the circuit illustrated in Figure P3.11a. Repeat for Figure P3.11b.

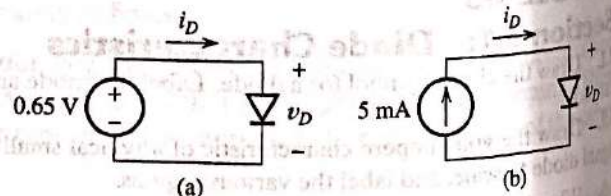


Figure P3.11

3.12. Sketch i against v to scale for the circuits displayed in Figure P3.12. The individual device characteristics are shown in Figures P3.9d and e.

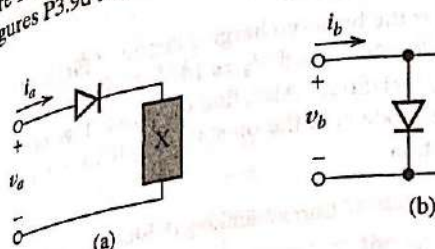


Figure P3.12

Section 3.3: The Ideal-Diode Model

3.13. Describe the ideal-diode model. Draw its i - v characteristic.

3.14. After solving a circuit with ideal diodes, what check is necessary for diodes initially assumed to be on? Off?

3.15. Assuming that the diodes are ideal, find the values of I and V for the circuits of Figure P3.15.

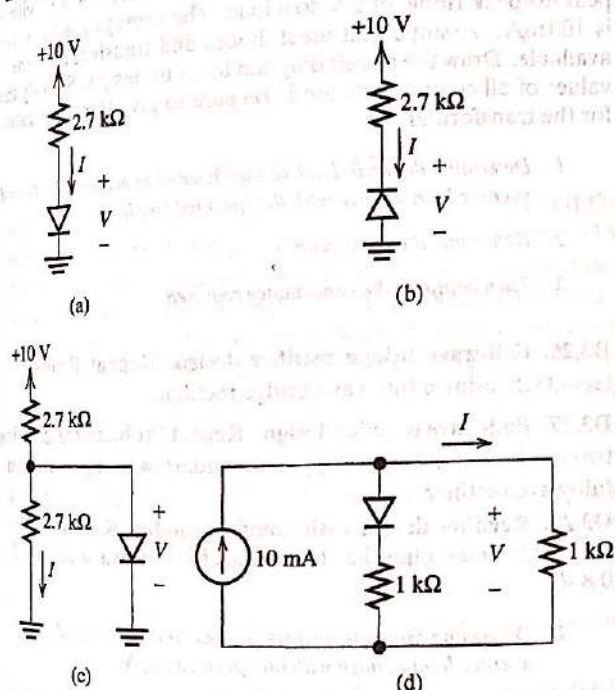


Figure P3.15

3.16. Assuming that the diodes are ideal, find the values of I and V for the circuits of Figure P3.16.

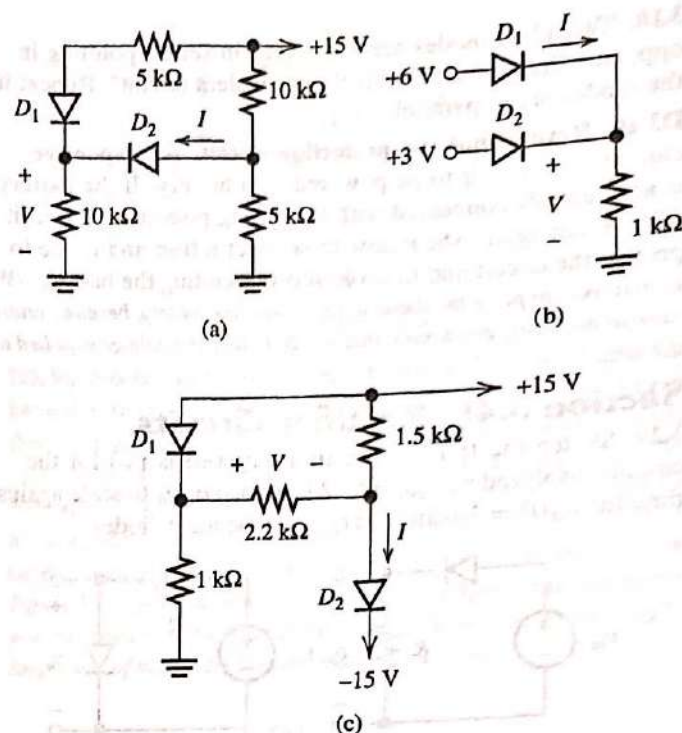


Figure P3.16

3.17. Assuming that the diodes are ideal, find the values of I and V for the circuits of Figure P3.17. For part (b), consider $V_{in} = 0, 2, 6, \text{ and } 10 \text{ V}$. Then plot V against V_{in} for $-10 \leq V_{in} \leq 10$.

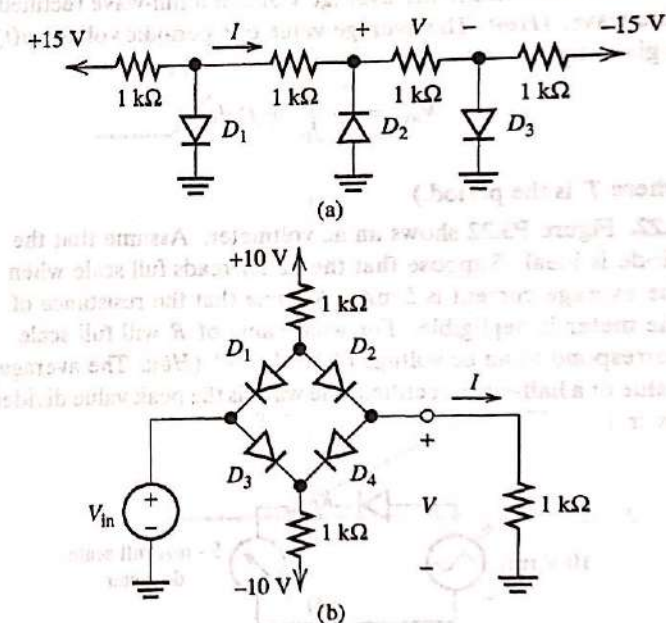


Figure P3.17

3.18. Two ideal diodes are connected in series, pointing in opposite directions. What is the equivalent circuit? Repeat if the diodes are in parallel.

D3.19. Reverse-polarity-protection circuit. An expensive electronic circuit is to be powered by a battery. If the battery is accidentally connected with the wrong polarity, the circuit will be damaged. Show how to connect a fuse and diode to protect the circuit and to avoid short-circuiting the battery. (We do not want to place the diode in series with the battery, because, under normal operating conditions, that would reduce the voltage supplied to the circuit.)

Section 3.4: Rectifier Circuits

3.20. Sketch the transfer functions (v_o versus v_{in}) for the circuits displayed in Figure P3.20. Also, plot v_o to scale against time for $v_{in}(t) = 10 \sin(200\pi t)$. Assume ideal diodes.

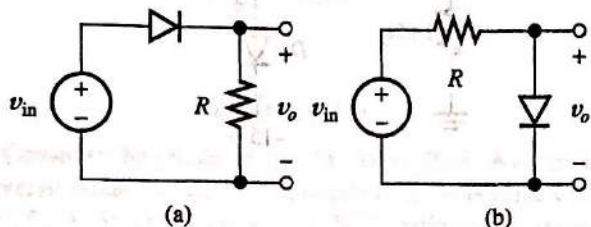


Figure P3.20

3.21. (a) Show that the average value of a half-wave rectified sine wave is the peak value divided by π .

(b) Determine the average value of a full-wave rectified sine wave. (Hint: The average value of a periodic voltage $v(t)$ is given by

$$V_{avg} = \frac{1}{T} \int_0^T v(t) dt$$

where T is the period.)

3.22. Figure P3.22 shows an ac voltmeter. Assume that the diode is ideal. Suppose that the meter reads full scale when the average current is 5 mA. Assume that the resistance of the meter is negligible. For what value of R will full scale correspond to an ac voltage of 10 V rms? (Hint: The average value of a half-wave rectified sine wave is the peak value divided by π .)

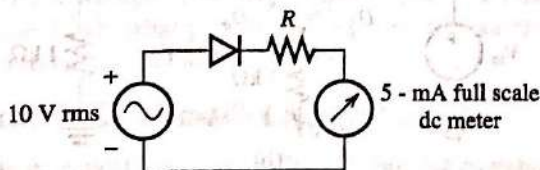


Figure P3.22

3.23. Draw the circuit diagram of a half-wave rectifier that will deliver a nearly steady dc voltage to a load from an ac source. Include a transformer to adjust the voltage level. Draw two different full-wave circuits.

3.24. Consider the battery-charging circuit of Figure P3.24 with $V_m = 20$ V, $R = 10 \Omega$, and $V_B = 14$ V. Find the peak current, assuming an ideal diode. Also, find the percentage of each cycle for which the diode is in the on state. Sketch $v_s(t)$ and $i(t)$ to scale against time.

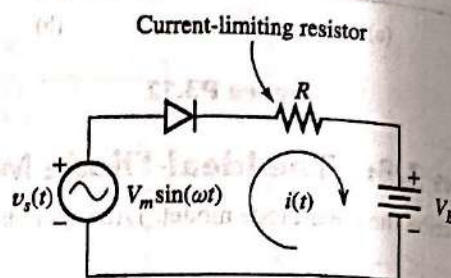


Figure P3.24 Half-wave battery charger.

D3.25. Half-wave rectifier design. Power is available from a 110-V rms, 60-Hz ac source. Design a half-wave rectifier power supply that will deliver an average voltage of 9 V with a peak-to-peak ripple of 2 V to a load. The average load current is 100 mA. Assume that ideal diodes and transformers are available. Draw the circuit diagram for your design. Specify the values of all components used. Be sure to give the turns ratio for the transformer.

1. Determine the peak load voltage needed to achieve the desired average load voltage with the specified ripple.
2. Determine the turns ratio.
3. Then compute the capacitance required.

D3.26. Full-wave bridge rectifier design. Repeat Problem D3.25 using a full-wave bridge rectifier.

D3.27. Full-wave rectifier design. Repeat Problem D3.25 using two diodes and a center-tapped secondary winding to form a full-wave rectifier.

D3.28. Rectifier design with nonideal diodes. Repeat Problem D3.25, assuming that the diodes have forward drops of 0.8 V.

1. Determine the peak voltage needed to achieve the desired average load voltage with the specified ripple.
2. Allow for the diode drops and determine the peak secondary voltage required.
3. Determine the turns ratio.
4. Then compute the capacitance required.

3.29. A full-wave rectifier is to be used to convert 400-Hz ac to dc. The dc output voltage is 15 V and the load current is 1 A. The ripple voltage is required to have a peak-to-peak value of 0.5 V or less. Estimate the capacitance required. Repeat for a 60-Hz source. Comment.

Section 3.5: Wave-Shaping Circuits

3.30. What is a clipper circuit? Draw a sample circuit diagram, including component values, an input waveform, and the corresponding output waveform.

3.31. Repeat Problem 3.30 for a clamp circuit.

3.32. **Voltage-doubler circuit.** Consider the circuit of Figure P3.32. The capacitors are very large, so that they discharge only a very small amount per cycle. (Thus, no ac voltage appears across the capacitors, and the ac input plus the dc voltage of C_1 must appear at point A.) Sketch the voltage at point A against time. Find the voltage across the load. Why is this circuit called a voltage doubler? Determine the peak inverse voltage across each diode in terms of V_m .

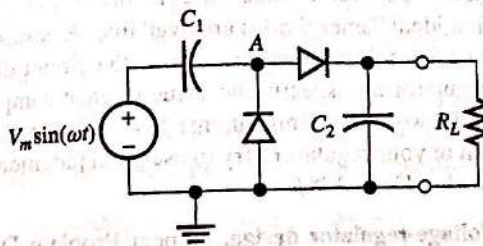


Figure P3.32

D3.33. **Clipper design.** Design a clipper circuit to clip off the portions of an input voltage that fall above 3 V or below -5 V. The input voltage ranges from -10 to +10 V. Assume that diodes having a forward drop of 0.7 V are available. Ideal Zener diodes of any breakdown voltage required are available. Use standard 5%-tolerance resistor values, and design for a peak current of about 1 mA in the diodes. The power-supply voltages that are available are ± 15 V. Try the circuit configuration shown in Figure 3.16a.

D3.34. **Clipper design.** Repeat Problem D3.33, assuming that the clipping levels are +2 V and +5 V (i.e., every part of the input waveform below +2 or above +5 is clipped off). Try a circuit configuration like that shown in Figure 3.16a but add a resistor connected to the positive power supply to keep one of the Zener diodes in the breakdown region.

3.35. Consider the circuit shown in Figure P3.35. Allow 0.6 V for the forward drops of the diodes. Sketch the transfer characteristic to scale. (Combining the bridge rectifier with a Zener diode is a neat way to obtain nearly identical characteristics for both polarities of the input voltage.)

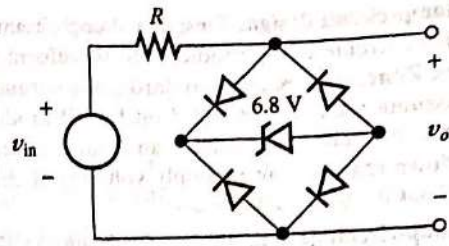
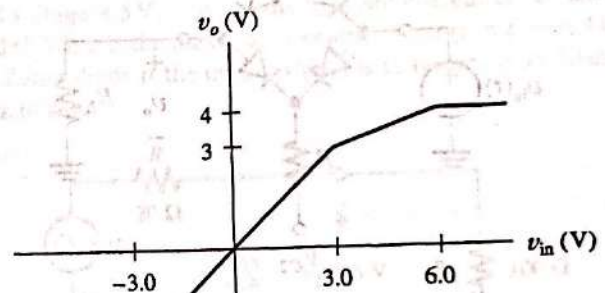
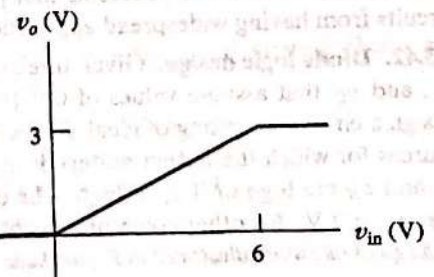


Figure P3.35

D3.36. **Nonlinear transfer characteristics.** Design circuits that have the transfer characteristics shown in Figure P3.36. Assume that v_{in} ranges from -10 to +10 V. Use diodes, Zener diodes, and standard 5%-tolerance resistor values. Assume a 0.6-V forward drop for all diodes, and suppose that the Zener diodes have an ideal characteristic in the breakdown region. Power-supply voltages of ± 15 V are available. Look at Exercise 3.17 and Figure 3.7 to get some ideas for the circuit configurations. For part b you may need to add a resistor connected to the positive power supply to keep some of the diodes forward biased with $v_o = 0$.



(a)



(b)

Figure P3.36

D3.37. Clamp-circuit design. Design a clamp circuit to clamp the negative extreme of a periodic input waveform to -5 V . Use diodes, Zener diodes, and standard 5%-tolerance resistor values. Assume a 0.6-V forward drop for all diodes, and suppose that the Zener diodes have an ideal characteristic in the breakdown region. Power-supply voltages of $\pm 15\text{ V}$ are available. Look at Figure 3.20a for ideas.

D3.38. Clamp-circuit design. Repeat Problem D3.37 to clamp the positive extreme to $+5\text{ V}$. Look at Figure 3.20a for ideas.

3.39. (a) Consider the electronic switch shown in Figure P3.39. Assume ideal diodes, $R = R_L = 1\text{ k}\Omega$, $V_{C1} = +5\text{ V}$, and $V_{C2} = -5\text{ V}$. Plot the transfer characteristic (v_o versus v_{in}) for v_{in} ranging from -5 V to $+5\text{ V}$. (b) Repeat for $V_{C1} = -5\text{ V}$ and $V_{C2} = +5\text{ V}$.

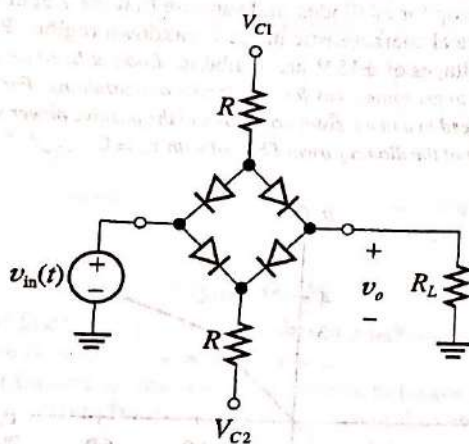


Figure P3.39 Electronic switch.

Section 3.6: Diode Logic Circuits

3.40. Draw the circuit diagram of a two-input diode AND gate. Repeat for a two-input OR gate.

3.41. Briefly discuss two problems that prevent diode logic circuits from having widespread application.

D3.42. Diode logic design. Given three input logic signals v_A , v_B , and v_C that assume values of 0 V (low) or 5 V (high), design a circuit consisting of ideal diodes, resistors, and voltage sources for which the output voltage is high (i.e., $v_o > 3\text{ V}$) if v_A and v_B are high or if v_C is high. The output should be low (i.e., $v_o < 1\text{ V}$) for other combinations of the inputs. Combine diode gates like those illustrated in Figure 3.23.

3.43. Assuming real diodes with forward drops of 0.6 V and input logic levels of 0 V and 5 V , how many diode OR gates can be cascaded if the output voltage for the high state is required to be greater than 3.5 V ?

Section 3.7: Voltage-Regulator Circuits

3.44. Draw the circuit diagram of a simple voltage regulator. Give the definitions of source regulation and load regulation.

3.45. A 6-V Zener diode regulator circuit operates from a source that varies from 10 to 14 V , the series resistance is 100Ω , and the load draws a current that varies from 0 to 30 mA . Determine the power dissipation in the Zener diode under worst-case conditions (i.e., the highest power dissipation).

3.46. We want to design a simple 5-V Zener diode voltage regulator that operates from a source that varies from 10 to 14 V . The load current varies from 0 to 10 mA . Determine the value of the series resistance so that the minimum magnitude of the Zener-diode current is 5 mA .

D3.47. Voltage-regulator design. Design a voltage regulator circuit that will provide a constant voltage of 5 V to a load from a variable supply voltage. The load current varies from 0 to 100 mA , and the source voltage varies from 8 to 10 V . You may assume that ideal Zener diodes are available. Resistors should be standard 5%-tolerance values. Draw the circuit diagram of your regulator and specify the value of each component. Also, find the worst-case (maximum) power dissipated in each component of your regulator. Try to use good judgment in your design. Look at Figure 3.28 for ideas.

D3.48. Voltage-regulator design. Repeat Problem D3.47, assuming that the supply voltage ranges from 6 to 10 V .

D3.49. Voltage-regulator design. Repeat Problem D3.47, assuming that the load current varies from 0 to 1 A .

Section 3.8: Linear Small-Signal Equivalent Circuits

3.50. An ideal Zener diode has a vertical volt-ampere characteristic in the breakdown region. What is the value of the dynamic resistance of the ideal Zener diode in the breakdown region?

3.51. A small-signal diode conducts 1 mA for a forward voltage of 0.6 V at a temperature of 300 K . Determine I_s , assuming that $n = 1$. Repeat for $n = 2$.

3.52. Solve the Shockley equation for v_D .

3.53. Consider the circuit illustrated in Figure P3.53. The source voltage consists of a dc component plus an ac ripple. The diode has a forward drop of approximately 0.6 V and $n = 1$. Find an approximate expression for the output voltage $v_D(t)$, including both the dc term and a small ac term.

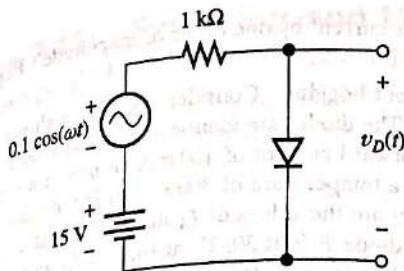


Figure P3.53

3.54. A certain integrated circuit *pn*-junction diode has $n = 1$ and a forward voltage of 0.6 V for a forward current of 1 mA. Another junction on the same chip has identical structure and doping as the first diode, except that the junction area is 10 times larger. Find the forward voltage of the second diode for a forward current of 1 mA. (Hint: I_s is proportional to the junction area.)

3.55. The circuit displayed in Figure P3.55 is used to provide an output voltage of approximately 2.4 V. The diodes have $n = 1$. (a) With the load disconnected, determine the change in v_o when the source voltage changes from 10 V to 12 V. Compute the percentage source regulation for this circuit. (b) For $V_s = 12$ V, determine the change in v_o when the load is connected, and find the percentage load regulation.

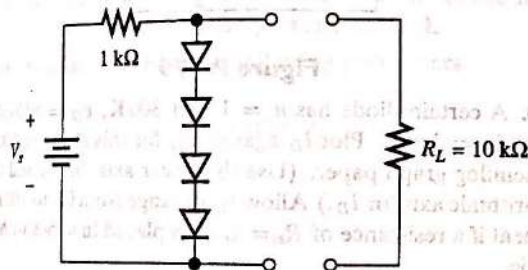


Figure P3.55

3.56. Suppose that a certain diode has $n = 1$ and carries a forward current of 2 mA. Assume that $V_T = 26$ mV. Determine the dynamic resistance of the diode. Now suppose that an identical diode is placed in parallel with the first diode and the current splits equally between them. Determine the dynamic resistance of the parallel combination. Compare the results and comment.

3.57. Consider the voltage regulator circuit shown in Figure 3.28a. Suppose that the dynamic resistance of the Zener diode is denoted as r_z . Derive expressions for the source and load regulations in terms of R , r_z , and R_L . Assume that the no-load current is zero (i.e., R_L is disconnected from the circuit).

3.58. A certain diode has $I_s = 10^{-14}$ A and $n = 1$. Assume that $V_T = 26$ mV.

- Determine the dynamic resistance if the forward current is 1 mA.
- Use the dynamic resistance to find the change in the diode voltage if the current changes to 1.1 mA.
- Use the Shockley equation to determine the diode voltages for 1 mA and 1.1 mA. Compare the difference between these values with the change computed in part (b). What is the percentage error?

3.59. A breakdown diode has

$$i_D = \frac{-10^{-6}}{(1 + v_D/5)^3} \text{ for } -5 \text{ V} < v_D < 0$$

where i_D is in amperes. Plot i_D against v_D in the reverse-bias region. Find the dynamic resistance of this diode at $I_{DQ} = -1$ mA and at $I_{DQ} = -10$ mA.

3.60. Consider the voltage regulator circuit illustrated in Figure P3.60. The ac ripple voltage is 1 V peak to peak. The dc load voltage is 5 V. What is the Q -point current in the Zener diode? What is the maximum dynamic resistance allowed for the Zener diode if the output ripple is to be less than 10 mV peak to peak?

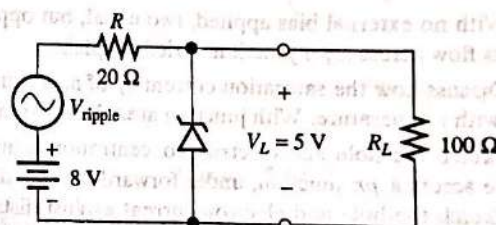


Figure P3.60

Section 3.9: Basic Semiconductor Concepts

3.61. Sketch the crystal lattice structure of intrinsic silicon, and label the important features.

3.62. What is the relationship between hole concentration and free-electron concentration in an intrinsic semiconductor?

3.63. Briefly discuss the generation and recombination of charge carriers in a semiconductor.

3.64. How does the conductivity of intrinsic silicon depend on temperature? Why?

3.65. Sketch the crystal lattice structure for *n*-type silicon. Repeat for *p*-type. Label the important features on the sketches.

- 3.66. Write an equation relating the donor-atom concentration, the acceptor-atom concentration, the free-electron concentration, and the hole concentration for a doped semiconductor.
- 3.67. Briefly discuss the mass-action law.
- 3.68. Briefly discuss conduction due to drift. Define mobility.
- 3.69. Briefly discuss conduction due to diffusion.
- 3.70. Given that silicon has about 5×10^{22} atoms/cm³, find the volume occupied by each silicon atom and an (order-of-magnitude) estimate of the center-to-center spacing between nearest atoms.
- 3.71. Doped silicon at 300 K contains 10^{16} acceptor atoms/cm³. Find the hole concentration and the free-electron concentration.
- 3.72. Find the hole concentration and free-electron concentration of silicon at 300 K if
- The acceptor concentration is 10^{15} cm⁻³ and the donor concentration is 10^{17} cm⁻³.
 - The acceptor concentration is 10^{15} cm⁻³ and the donor concentration is 10^{15} cm⁻³.

Section 3.10: Physics of the Junction Diode

- 3.73. Sketch a *pn* junction, showing the charge stored in the depletion region. Also, sketch the hole and electron concentrations against distance across the junction.
- 3.74. With no external bias applied, two equal, but opposite, currents flow across a *pn* junction. Briefly explain.
- 3.75. Discuss how the saturation current I_s of a *pn* junction varies with temperature. With junction area. With doping.
- 3.76. Sketch the hole and electron concentration against distance across a *pn* junction, under forward-bias conditions. Also, sketch the hole and electron current against distance. Assume equal doping levels on both sides of the junction.
- 3.77. Consider the circuit displayed in Figure P3.77. The diodes are identical and have $n = 1$. The temperature of each diode is 300 K. Before the switch is closed, the voltage v is 600 mV. Find v after the switch is closed. Repeat for $n = 2$.

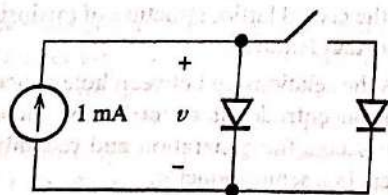


Figure P3.77

- 3.78. A junction diode has $n = 1$ and is operating at 300 K, with a current of 1 mA and a voltage of 600 mV. By how much must the voltage be increased (a) to double the current? (b) to

increase the current by one order of magnitude? Repeat part (a) and (b) if $n = 2$.

3.79. **Current hogging.** Consider the diodes shown in Figure P3.79. The diodes are identical and have $n = 1$. For each diode, a forward current of 100 mA results in a voltage of 700 mV at a temperature of 300 K. (a) If both diodes are at 300 K, what are the values of I_A and I_B ? (b) If diode A is at 300 K and diode B is at 305 K, again find I_A and I_B . [Hint: Answer part (a) by the use of symmetry. For part (b), a transcendental equation for the voltage across the diodes can be found. Solve by trial and error.] An important observation to be made from this problem is that, starting at the same temperature, the diodes should theoretically each conduct half of the total current. However, if one diode conducts slightly more, it becomes warmer, resulting in even more current. Eventually, one of the diodes hogs most of the current. Even particularly noticeable with large currents for which significant heating occurs.

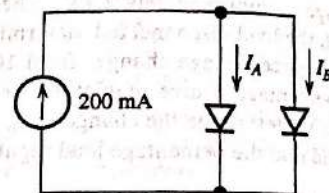


Figure P3.79

- 3.80. A certain diode has $n = 1$. At 300 K, $v_D = 650$ mV when $i_D = 1$ mA. Plot i_D against v_D for this diode at 300 K on semilog graph paper. (Use the linear axis for v_D and the logarithmic axis for i_D .) Allow i_D to range from 0.1 to 100 mA. Repeat if a resistance of $R_s = 10 \Omega$ is placed in series with the diode.
- 3.81. A certain p^+n -junction diode is known to have an emission coefficient $n = 1$. For a forward voltage of 0.6 V, the current is 1 mA. A second diode is identical, except that the dopant concentrations on both sides of the junction are twice as great as for the first diode. What is the forward voltage of the second diode for a current of 1 mA? Assume a temperature of 300 K. (Hint: The saturation current I_s is proportional to the minority carrier concentration on the n -side of the junction. Increased doping reduces the minority carrier concentration.)
- 3.82. A certain *pn* junction has $N_A = 10^{15}$ cm⁻³ on the p -side and $N_D = 10^{15}$ cm⁻³ on the n -side. Plot the hole and free-electron concentrations to scale against distance across the junction. Use a logarithmic scale for the concentrations. Label the p -side, the depletion region, and the n -side. Assume zero bias and a temperature of 300 K.

Section 3.11: Switching and High-Frequency Behavior

3.83. Name the two capacitances associated with a pn -junction diode. Which is most important under reverse bias? Under forward bias?

3.84. Draw the small-signal equivalent circuit for a pn -junction diode under forward-bias conditions.

3.85. A junction diode is connected in series with a resistance and a voltage source. Prior to $t = 0$, the source forward biases the diode, and the current is I_F . At $t = 0$, the polarity of the source reverses. Sketch the diode current against time. Label the storage interval, the transition interval, and the reverse recovery time on the sketch.

3.86. A capacitor is formed by a square plate of aluminum separated from a silicon substrate by a layer of silicon dioxide that has a thickness of 1000 angstroms (1 angstrom = 10^{-10} m). Find the dimensions of the aluminum plate for a capacitance of 30 pF. The relative dielectric constant of silicon dioxide is approximately 3.97.

3.87. A pn junction has $C_{j0} = 100$ pF, $\phi_0 = 1.0$ V, and $m = 1/2$. Find the depletion capacitance for a reverse-bias voltage of 1 V and for 10 V. Repeat for $m = 1/3$.

3.88. A certain diode has a saturation current $I_s = 10^{-12}$, an emission coefficient $n = 1$, and a transit time $\tau_T = 1$ μ s. Plot the diffusion capacitance against forward voltage for $0 < v_D < 0.7$ V. Assume a temperature of 300 K.

3.89. A certain diode has the following parameters:

$$I_s = 10^{-15} \text{ A};$$

$$n = 1;$$

$$C_{j0} = 5 \text{ pF};$$

$$\phi_0 = .9 \text{ V};$$

$$m = 0.333;$$

$$R_s = 20 \Omega;$$

$$\tau_T = 6 \text{ ns}.$$

Find the small-signal equivalent circuit for the diode, including values, if the diode is

- Reverse biased with $V_{DQ} = -20$ V.
- Forward biased with $I_{DQ} = 1$ mA.
- Forward biased with $I_{DQ} = 10$ mA.

3.90. Consider the circuit shown in Figure P3.90. Prior to $t = 0$, the source voltage is +5 V. At $t = 0$, it switches

abruptly to -5 V. The voltage across the diode is observed on an oscilloscope having an input capacitance of 7 pF. The voltage waveform is shown in the figure. For the diode, find

- The ohmic resistance R_s .
- The zero-bias junction capacitance C_{j0} . Neglect the effect of R_s for this part of the problem. [Hint: $dQ/dv_D = (dQ/dt)/(dv_D/dt)$. Also, $dQ/dt = i_D$.]
- The transit time τ_T .

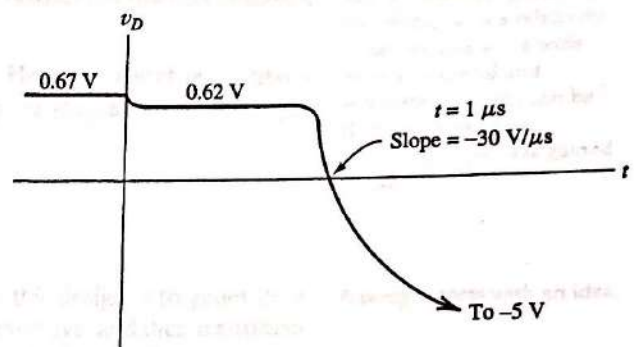
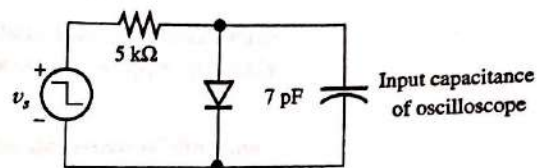


Figure P3.90

Section 3.12: Computer-Aided Analysis of Diode Circuits

D3.91. Electronic thermometer design. A diode can be used as a temperature sensor because its forward voltage decreases by about 2 mV/°C. Design an electronic thermometer that produces $v_o = T/10$, where T is the diode temperature in °C and v_o is the output voltage of the circuit in volts. Design for temperatures ranging from 0 to 50°C. Use power-supply voltages of ± 15 V, any diodes or op amps for which you have SPICE models, and 5%-tolerance discrete resistors. Include two adjustable resistances in your design, so that the zero and full-scale outputs can be adjusted. Verify your design using SPICE. Suggestions: Use a Zener-diode regulator to obtain a constant reference voltage to supply current to the sensor diode(s). Use several diodes in series for the sensor to obtain a larger voltage change with temperature. Use amplifiers and a summer (see Figure 2.7) to derive the desired output voltage from the reference voltage and the sensor voltage.

A FUNCTION GENERATOR

After studying the first three chapters of this book, you have seen many useful circuits and become familiar with some important concepts. Just as beautiful poetry can be written with a relatively small vocabulary, a wide variety of useful and interesting circuits can be designed using the knowledge you have gained so far. In this section, "Anatomy of a Circuit Design," you will have a chance to look over the shoulder of a circuit designer at work. We will observe the design of a function generator having the following specifications:

- The circuit must generate a sine wave, a symmetrical square wave, and a symmetrical triangular wave. All waveforms must have peak amplitudes of approximately 5 V.
- The circuit must have a convenient means for varying the frequency of the waveforms through the range from 1 kHz to 10 kHz.
- The circuit must be composed of standard-value fixed resistors, adjustable resistors, standard-value capacitors, op amps, and diodes.
- The circuit must be powered from +15 V and -15 V. However, the characteristics of the output waveforms must not depend strongly on the exact power-supply voltages.

Just as beautiful poetry can be written with a relatively small vocabulary, a wide variety of useful and interesting circuits can be designed using the knowledge you have gained so far.

Development of a Block Diagram

A design starts with an idea. For example, the idea used in this design is to generate a square wave, integrate the square wave to obtain the triangular wave, and then transform the triangular wave into a sine wave, using a nonlinear wave-shaping circuit.

A design starts with an idea.

Of course, many alternative ideas are possible for most design problems. For example, we could design a sinusoidal oscillator, apply the sine wave to a Schmitt trigger to generate the square wave, and integrate the square wave to obtain the triangular wave. Another idea would be to store amplitude values of the three waveforms in digital memory circuits. The stored values would be read from the memories and applied to digital-to-analog converters to generate successive points on the waveforms. Periodic waveforms would result from cycling through the stored values.

Actually, none of these ideas is original. All of the approaches mentioned have been used many times and are standard ways of designing waveform generators. A wealth of approaches to common design problems is accumulated with experience.

A wealth of approaches to common design problems is accumulated with experience.

After selecting an approach, the designer draws the block diagram of the circuit to be designed. The block diagram for the present design is shown in Figure AD1.1. The Schmitt trigger produces a square-wave output with levels of ± 5 V. (Schmitt trigger circuits were discussed near the end of Section 2.3; see Figure 2.10 and the related discussion.) The output of the Schmitt trigger is integrated to form the triangular waveform. The designer has anticipated using the op-amp integrator of Section 2.11, which has a negative gain constant. Thus, the negative slope of the triangle corresponds to the positive half-cycle of the square wave.

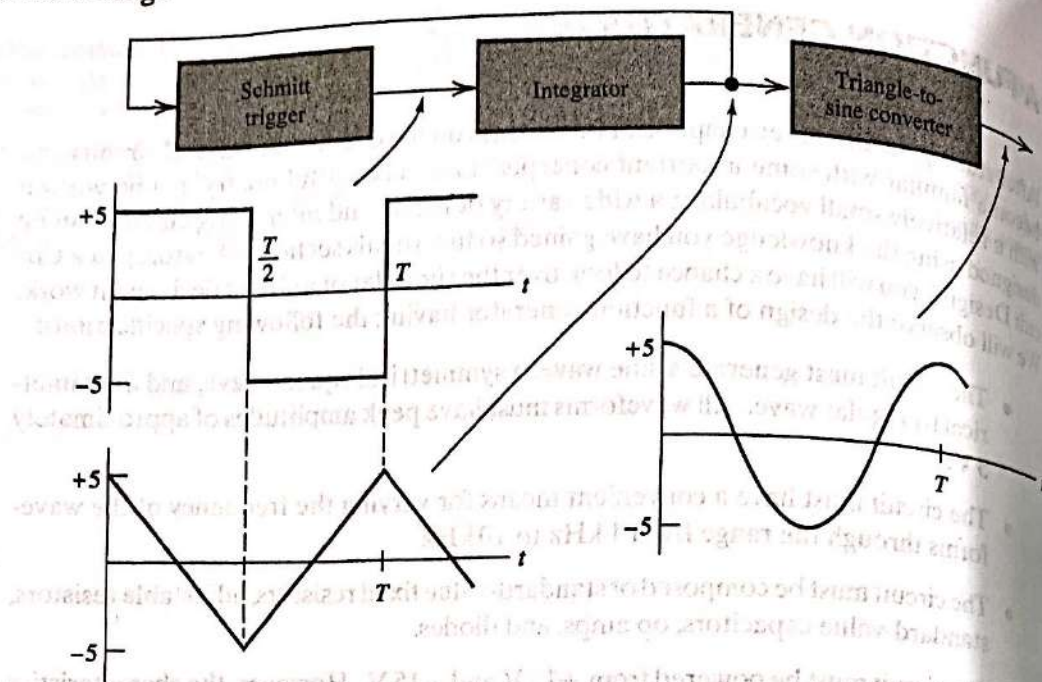


Figure AD1.1 Block diagram of the function generator.

Notice that the output of the integrator is returned to the input of the Schmitt trigger. When the triangular waveform reaches $+5$ V or -5 V, the output of the Schmitt trigger changes state. Thus, a Schmitt trigger having input threshold levels of ± 5 V and output levels of ± 5 V is required. The desired circuit is similar to the circuit discussed in Section 2.3.

The output voltage of an op-amp integrator circuit is given by Equation 2.53.

$$v_o(t) = -\frac{1}{RC} \int_0^t v_{in}(x) dx$$

(The variable x is a dummy variable.) The designer plans to vary the frequency of the waveforms by changing the gain $1/RC$ of the integrator (with a variable resistance). With low integrator gain (i.e., high resistance), the triangular wave changes slowly, taking longer to go from one extreme to the other, thereby resulting in low frequency. On the other hand, higher integrator gain results in higher frequency.

Notice that the amplitudes of both the triangular and square waves are independent of the integrator gain. Instead, these amplitudes depend on the thresholds and output levels of the comparator. Thus, the frequency can be changed without affecting the amplitudes.

The designer works with each of the functional blocks separately and then puts the blocks together to form the complete function generator. Of course, the circuits affect one another, and designers find themselves going back and forth between the blocks. In the interest of conserving space and reducing confusion, we show the final design of each circuit, rather than present a complete history of how it was developed. As in baking a cake or building a house, circuit design is often a messy process, but the end result can be very neat.

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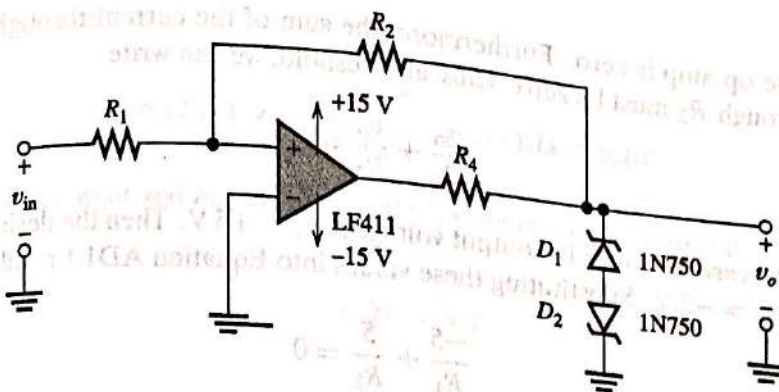


Figure AD1.2 Circuit diagram of the Schmitt trigger circuit.

Design of the Schmitt Trigger

We will try to use parts with which we have become familiar earlier. Thus, we will use the LF411 as the comparator in designing the Schmitt trigger. Actually, the LF411 is intended for use as an op amp, and because of slew-rate limitations, it is not as fast as ICs that are intended for use as comparators. However, the LF411 is adequate for this design.

With supply voltages of ± 15 V, the LF411 output saturates at about ± 14 V. Hence, we must add some components to ensure that the output levels of our circuit are the desired values (which are ± 5 V). We employ a Zener-diode clipper circuit similar to those of Section 3.5 to establish the output levels. With the exception of the diode clipper circuit, the circuit for the Schmitt trigger is similar to that of Figure 2.10. The proposed circuit diagram is shown in Figure AD1.2.

The resistor R_4 and the two Zener diodes D_1 and D_2 form a clipper circuit, ensuring that the output voltage levels are symmetrical and nearly independent of the supply voltages. For example, when the output of the LF411 is high (approximately $+14$ V), D_2 is forward biased and D_1 is in reverse breakdown. The resulting output voltage is the sum of the forward drop of D_2 and the breakdown voltage of D_1 . This turns out to be about 5 V.

When the output of the LF411 is low, approximately -14 volts appears at its output terminal. This voltage acts through R_4 to forward bias D_1 and cause D_2 to be in reverse breakdown. In that case, the output voltage becomes approximately -5 V.

The value of R_4 should be picked high enough so that the output current of the LF411 is reasonable (say, less than 10 mA in magnitude) for both output states. However, if R_4 is too large, insufficient current is available for R_2 and the integrator input. We choose R_2 to be $100\text{ k}\Omega$ —a large value to minimize its current requirements. Furthermore, we will design the integrator so that its minimum input impedance is about $20\text{ k}\Omega$. Then, choosing $R_4 = 5.1\text{ k}\Omega$ allows sufficient current for R_2 and for the input to the integrator, as well as ensuring that the diodes operate as intended.

Finally, the value of R_1 is selected so that the threshold voltages of the Schmitt trigger are as close as possible to $+5$ and -5 V. At threshold, the voltage at the noninverting

input of the op amp is zero. Furthermore, the sum of the current through R_1 and the current through R_2 must be zero. Thus, at threshold, we can write

$$\frac{v_{in}}{R_1} + \frac{v_o}{R_2} = 0 \quad (AD1.1)$$

Consider the case for which the output voltage is $v_o = +5$ V. Then the desired threshold voltage is $v_{in} = -5$ V. Substituting these values into Equation AD1.1 results in

$$\frac{-5}{R_1} + \frac{5}{R_2} = 0$$

Solving this equation for R_1 , we obtain $R_1 = R_2$. Because we have previously selected $R_2 = 100$ k Ω , we also select $R_1 = 100$ k Ω .

We have completed the design of the Schmitt trigger. The circuit diagram is shown in Figure AD1.2, and the resistor values are

$$R_1 = 100 \text{ k}\Omega$$

$$R_2 = 100 \text{ k}\Omega$$

$$R_4 = 5.1 \text{ k}\Omega$$

The input thresholds are (approximately) ± 5 V and the output levels are ± 5 V.

Clearly, circuit designers need to be familiar with the size, cost, and other parameters of readily available components. This knowledge can be gained by reading device-manufacturer data sheets and distributor catalogs. You could start by looking at the catalog located at www.digikey.com.

Look at the catalog located at www.digikey.com to become familiar with practical components for electronic circuits.

Design of the Integrator

The circuit diagram of the integrator is illustrated in Figure AD1.3. (This circuit is discussed in Section 2.11.) The variable resistor is used as the frequency control. The output voltage is given by

$$v_o(t) = -\frac{1}{R_5 C_1} \int_0^t v_{in}(x) dx + v_o(0)$$

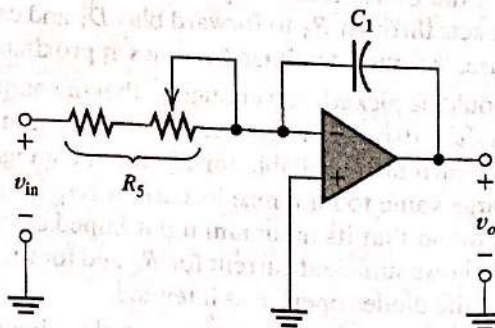


Figure AD1.3 Variable-gain integrator.

At $t = T/2$, this becomes

$$v_o(T/2) = -\frac{1}{R_5 C_1} \int_0^{T/2} v_{in}(x) dx + v_o(0) \quad (\text{AD1.2})$$

Referring to the input and output waveforms for the integrator shown in Figure AD1.1, we find that

$$v_o(0) = 5.0$$

and

$$v_o(T/2) = -5.0$$

During the time interval from 0 to $T/2$, we have $v_{in}(t) = 5$. Substituting these values into Equation AD1.2, we obtain

$$-5 = -\frac{1}{R_5 C_1} \int_0^{T/2} 5 dx + 5.0$$

which yields

$$R_5 C_1 = 0.25T \quad (\text{AD1.3})$$

We want to select a small value for the capacitance (to minimize its size and cost). Suppose that we select $C_1 = 1000$ pF. Let us consider a frequency of 10 kHz, for which $T = 100$ μ s. Then we can use Equation AD1.3 to determine that $R_5 = 25$ k Ω . For a frequency of 1 kHz, we have $R_5 = 250$ k Ω . Thus, we select R_5 to be the series combination of a 15-k Ω fixed resistor and a 500-k Ω variable. This allows the frequency to be adjusted over a bit more than the desired range (to allow for component tolerances).

Of course, the choice of a value for C_1 is not arbitrary. If we select a larger value for C_1 , the value of R_5 becomes smaller. Consequently, R_5 draws more current from the Schmitt trigger. If C_1 is too large and R_5 too small, the Schmitt is incapable of delivering the current. In the actual design process, we must go back and forth between the design of the integrator and the Schmitt trigger, so that the circuits are compatible.

Thus, we have completed the integrator design. The circuit diagram is shown in Figure AD1.3. We have chosen the LF411 op amp, C_1 to be 1000 pF, and R_5 to be the series combination of a 15-k Ω fixed resistor and a 500-k Ω variable resistor.

Design of the Triangle-to-Sine-Wave Converter

A triangular wave can be converted into a sine wave with the use of a circuit having the proper nonlinear transfer characteristic. This process is illustrated in Figure AD1.4. The equation for the ideal transfer characteristic is

$$v_s = V_{sm} \sin\left(\frac{\pi}{2} \frac{v_t}{V_{tm}}\right) \quad (\text{AD1.4})$$

where v_s is the sine-wave output voltage, which has a peak value of V_{sm} . The triangular input voltage is denoted as v_t , and V_{tm} is its peak value.

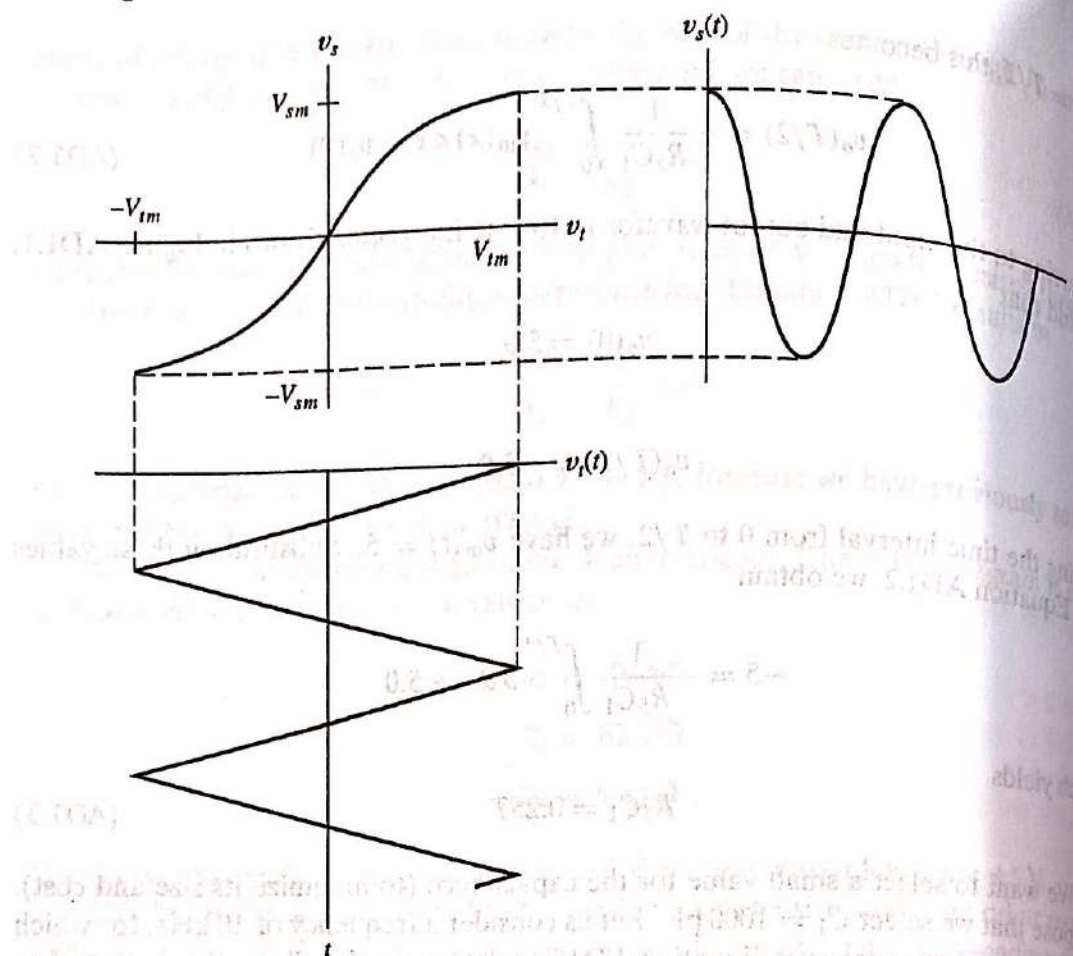


Figure AD1.4 A triangular wave is converted to a sine wave by use of the proper nonlinear transfer characteristic.

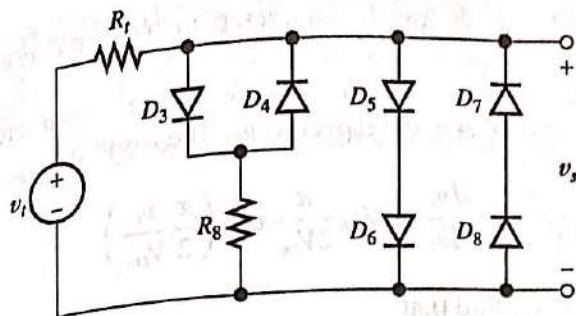
A variety of nonlinear amplifiers and diode circuits can be used to approximate this nonlinear transfer characteristic. We propose to use the circuit shown in Figure AD1.5.

Basic Operation of the Wave Shaper

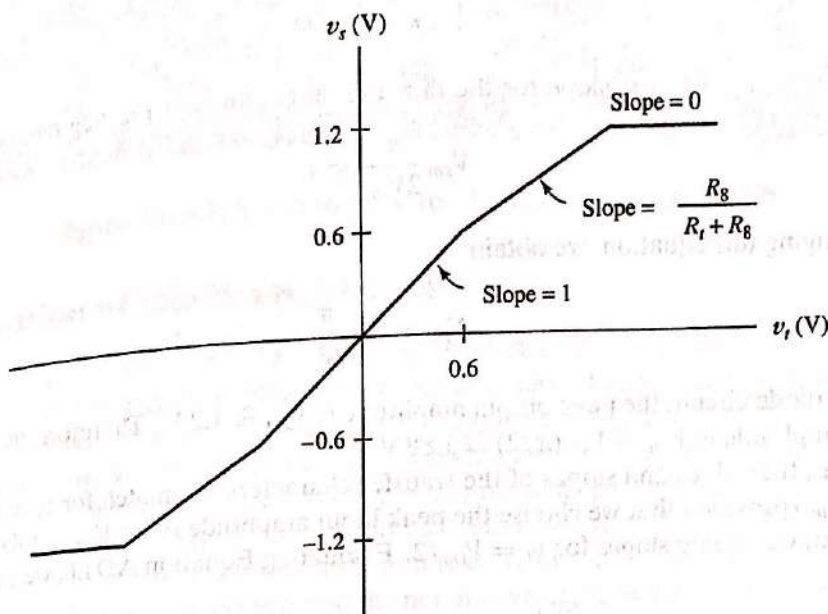
Initially, we assume that the diodes do not conduct until the forward voltage reaches 0.6 V. We also assume a constant voltage of 0.6 V in forward bias. (These values are typical for small-signal diodes such as the 1N4148, which the designer intends to use in this circuit.) Under these assumptions, we have $v_s = v_t$ for $|v_t| < 0.6$ V. This is because none of the diodes conducts for $|v_t| < 0.6$ V. Thus, as indicated in Figure AD1.5b, the slope of the transfer characteristic is unity in this region.

For $0.6 < |v_s| < 1.2$, either D_3 or D_4 is conducting (depending on the polarity of v_s). Because we assume constant forward voltage, the dynamic resistance of the diodes is zero in the forward region. Figure AD1.6 shows the small-signal equivalent circuit for this condition. Thus, the incremental (small-signal) voltage-division ratio of the circuit is

$$\frac{\Delta v_s}{\Delta v_t} = \frac{R_8}{R_t + R_8} \quad (\text{AD1.5})$$



(a) Circuit diagram



(b) Transfer characteristic

Figure AD1.5 Diode wave-shaping circuit.

As indicated in Figure AD1.5b, this is the slope of the transfer characteristic for $0.6 < |v_s| < 1.2$.

Finally, when v_s reaches 1.2 volts, diodes D_5 and D_6 begin to conduct, and the slope of the transfer characteristic becomes zero.

Actually, the diodes turn on gradually. Therefore, the transfer characteristic of the diode circuit tends to be a smooth curve, rather than the straight-line segments shown. Of course, this curvature tends to allow a better match to the desired sinusoidal transfer characteristic.

Selecting Parameter Values for the Wave Shaper

Now we consider how to select the parameters of the diode circuit in order to obtain a good match to the sinusoidal characteristic. In particular, we wish to specify the peak amplitude of the input triangular waveform V_{im} and the resistor values. Our approach

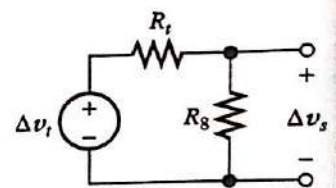


Figure AD1.6 Small-signal equivalent circuit if D_3 (or D_4) is conducting and the other diodes are nonconducting.

is to equate slopes of the diode transfer characteristic to the corresponding slopes of the ideal characteristic.

First, we find an expression for the slope of the ideal characteristic by taking the derivative of Equation AD1.4 with respect to v_t . The result is

$$\frac{dv_s}{dv_t} = V_{sm} \frac{\pi}{2V_{tm}} \cos\left(\frac{\pi}{2} \frac{v_t}{V_{tm}}\right) \quad (\text{AD1.6})$$

Evaluating for $v_t = 0$, we find that

$$\left. \frac{dv_s}{dv_t} \right|_{v_t=0} = V_{sm} \frac{\pi}{2V_{tm}} \quad (\text{AD1.7})$$

However, at $v_t = 0$, the slope for the diode circuit is unity. Equating these slopes, we have

$$V_{sm} \frac{\pi}{2V_{tm}} = 1 \quad (\text{AD1.8})$$

Rearranging this equation, we obtain

$$V_{tm} = V_{sm} \frac{\pi}{2} \quad (\text{AD1.9})$$

For the diode circuit, the peak output amplitude is $V_{sm} \cong 1.2$ V. Therefore, the required input amplitude is $V_{tm} = V_{sm} (\pi/2) \cong 1.88$ V.

Thus, the values and slopes of the transfer characteristics match for $v_t = 0$ and for $v_t = V_{tm}$ (provided that we choose the peak input amplitude to be $V_{tm} \cong 1.88$ V.)

Next, we equate slopes for $v_t = V_{tm}/2$. Evaluating Equation AD1.6, we have

$$\left. \frac{dv_s}{dv_t} \right|_{v_t=V_{tm}/2} = V_{sm} \frac{\pi}{2V_{tm}} \cos(\pi/4) \quad (\text{AD1.10})$$

Equating this to the corresponding slope of the diode transfer characteristic, we obtain

$$\frac{R_8}{R_t + R_8} = V_{sm} \frac{\pi}{2V_{tm}} \cos(\pi/4) \quad (\text{AD1.11})$$

Using Equation AD1.9 to substitute for V_{tm} , we get

$$\frac{R_8}{R_t + R_8} = \cos(\pi/4) \quad (\text{AD1.12})$$

Evaluating and rearranging yields

$$R_8 = 2.414 \times R_t \quad (\text{AD1.13})$$

Equations AD1.9 and AD1.13 provide guidance in selecting the input amplitude V_{tm} and the resistor values for the waveform converter.

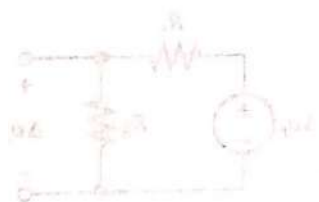


Figure AD1.3: Waveform converter circuit. The circuit consists of a diode in series with a resistor R_8 . The input voltage v_t is applied across the series combination, and the output voltage v_s is taken across the diode.

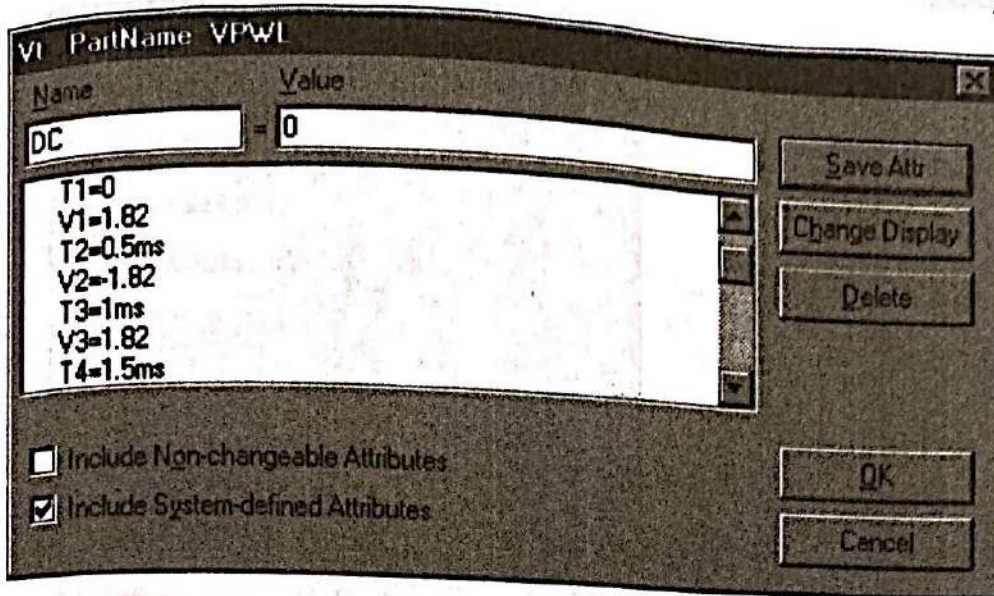


Figure AD1.7 Setup window for the piecewise linear source.

Simulation of the Wave Shaper

Next, we selected values for the wave-shaping circuit and used SPICE to evaluate its performance. The design equations do not specify values for all of the components, and we must pick one of the values by guessing. We started by selecting $R_f = 1 \text{ k}\Omega$, because this will result in reasonable currents (a few milliamperes). Then we tried values for R_f ranging above and below $1 \text{ k}\Omega$, obtaining nearly the same performance for a wide range of values (after optimizing the input amplitude and the value of R_g for each value of R_f). Therefore, we proceed under the assumption that $R_f = 1 \text{ k}\Omega$. Equation AD1.13 yields $R_g = 2.414 \text{ k}\Omega$, so we initially selected the nominal value $R_g = 2.4 \text{ k}\Omega$. Later simulation results showed that $2.7 \text{ k}\Omega$ gives a slightly better performance. So the final value for R_g is $2.7 \text{ k}\Omega$.

Because we anticipated that $V_{os} \cong 1.2 \text{ V}$, we used Equation AD1.9 to select $V_{tm} = 1.88 \text{ V}$ initially. However, later simulation results showed better performance for $V_{tm} = 1.82 \text{ V}$.

We have used a piecewise linear source VPWL for the triangular input source V_i . Double clicking on the source brings up the window shown in Figure AD1.7. Here, we simply specify points on the waveform. For example, at $t = 0$, we specified an amplitude of $+1.82 \text{ V}$; at $t = 0.5 \text{ ms}$, the amplitude is -1.82 V ; at $t = 1 \text{ ms}$, the amplitude is $+1.82$, etc. Connecting these points by straight lines produces a 1-kHz triangular waveform with a peak amplitude of 1.82 V .

Fourier theory shows that a distorted sine wave consists of the sine wave plus distortion components that are sine waves of harmonic frequencies. For example, a distorted 1-kHz sine wave contains distortion components with frequencies of 2 kHz , 3 kHz , 4 kHz , and so forth. A widely used measure of the fidelity of an imperfect sine wave is its total harmonic distortion (THD), which is defined to be the rms value of the distortion as a percentage of the fundamental component. SPICE has the capability to determine THD for periodic waveforms.

You can find the circuit file for Figure AD1.5(a) on the website.

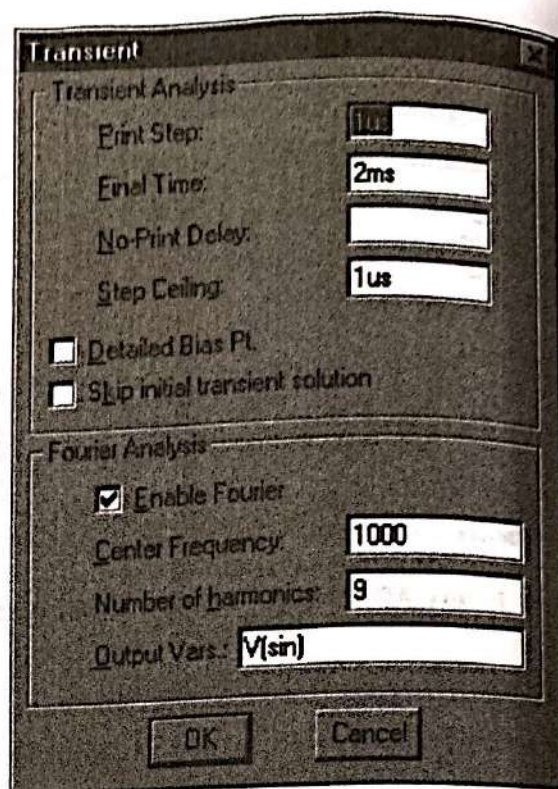


Figure AD1.8
Transient-analysis
setup window.

We have used the **analysis/setup/transient** commands to bring up the window illustrated in Figure AD1.8. We select a final time of 2 ms in order to be able to observe two cycles of the 1-kHz waveforms. We enable the Fourier analysis option, so that the program will determine the THD of the sine wave, $V(\sin)$.

Then we use the **analysis/simulate** command to simulate the circuit. Probe starts automatically after the simulation and displays the waveforms shown in Figure AD1.9.

Next, we return to the Schematics program and use the **analysis/examine output**

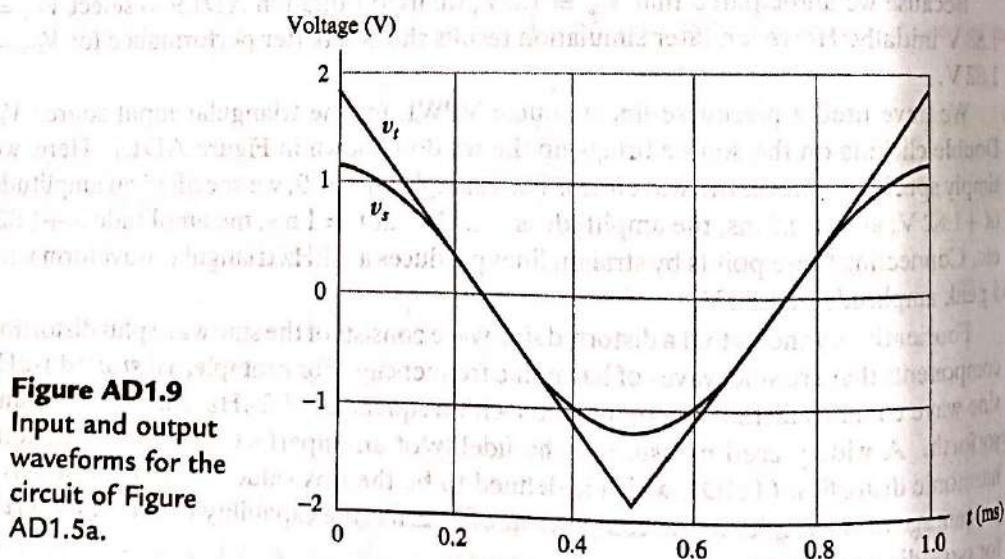


Figure AD1.9
Input and output
waveforms for the
circuit of Figure
AD1.5a.

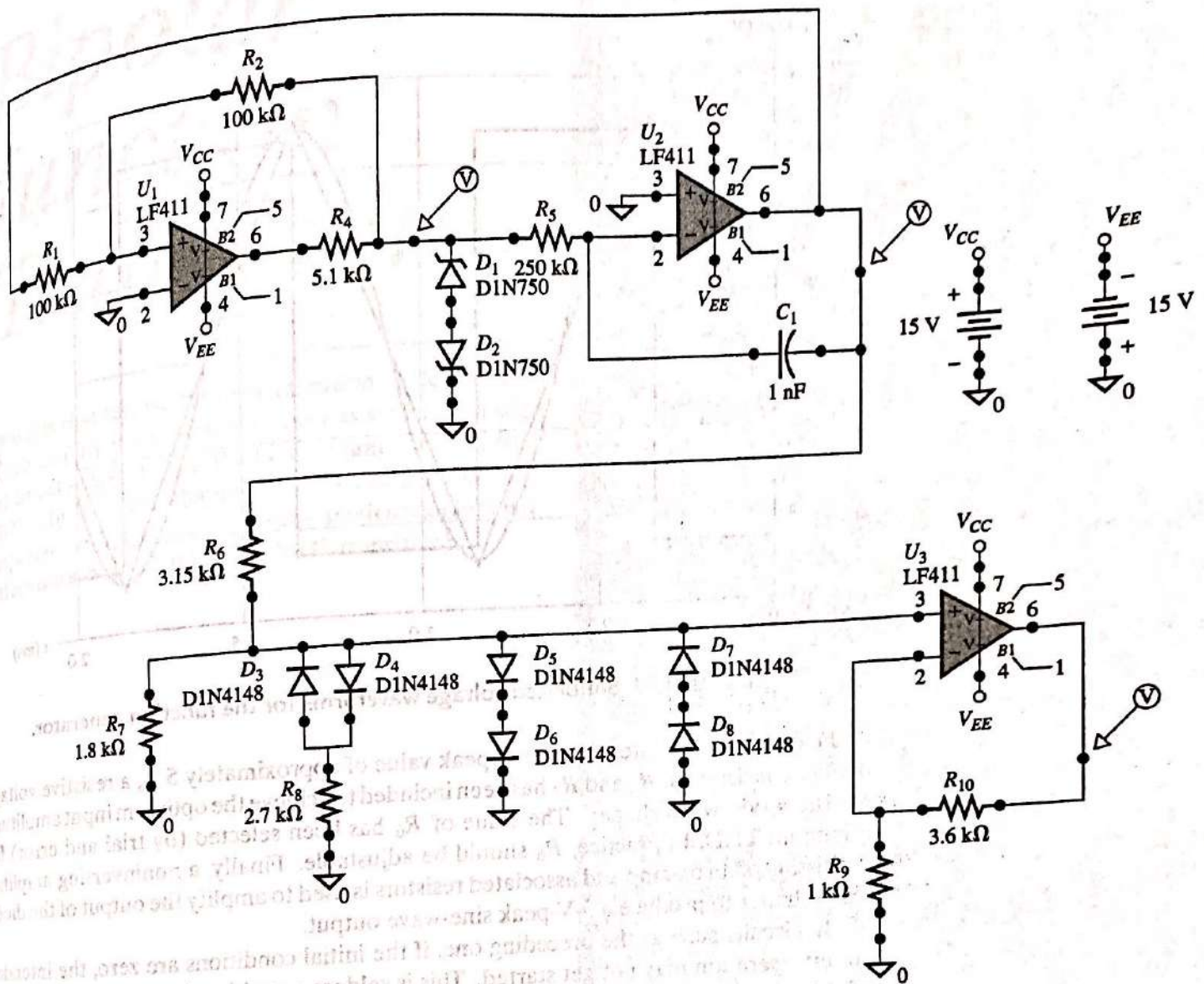


Figure AD1.10 Function generator. (The appearance of this figure is similar to that of the computer display.)

command to examine the output file. We scroll down toward the end of the file, where we find the results of the Fourier analysis, showing that the THD is 0.72% (which is very good for a circuit of this type).

If we change the peak value of the triangular input V_{tm} , we find that the THD increases rapidly. The value of V_{tm} must be controlled to within 1% for close-to-optimum performance. Thus, we include a variable control for the input amplitude to the wave shaper circuit in the final circuit.

The Complete Circuit

Figure AD1.10 shows the completed function generator design. The value of R_5 shown in the figure has been selected to produce a 1-kHz signal. Because the triangular signal

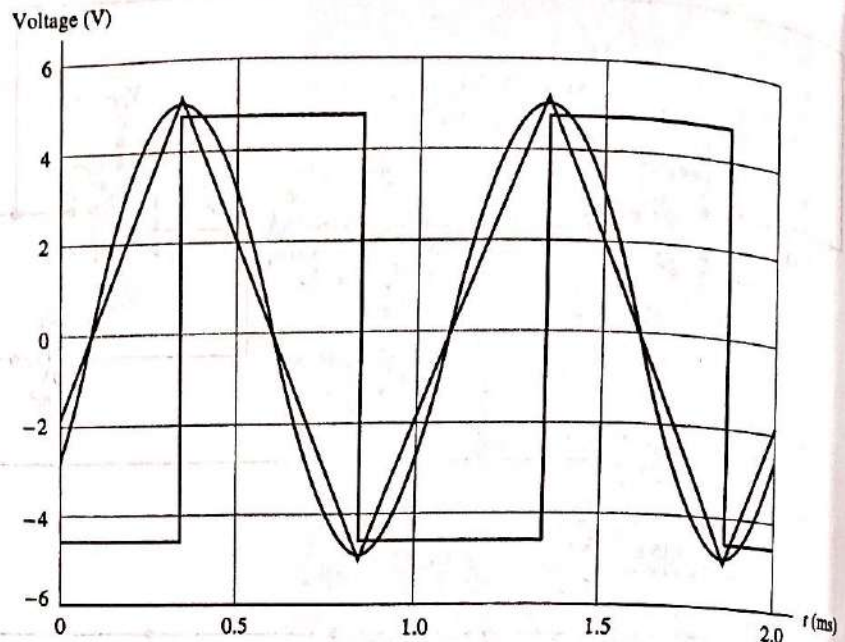


Figure AD1.11 Simulated voltage waveforms for the function generator.

at the output of the integrator has a peak value of approximately 5 V, a resistive voltage divider consisting of R_6 and R_7 has been included to achieve the optimum input amplitude for the diode wave shaper. The value of R_6 has been selected (by trial and error) for minimum THD. In practice, R_6 should be adjustable. Finally, a noninverting amplifier consisting of an op amp and associated resistors is used to amplify the output of the diode wave shaper to produce a 5-V-peak sine-wave output.

In circuits such as the preceding one, if the initial conditions are zero, the intended circuit operation may not get started. This is seldom a problem in real circuits, because offset voltages, bias currents, and so forth provide the initial push to start the sequence. Thus, we have specified an initial voltage for C_1 in the simulation. Anytime an oscillator circuit like this does not work for you in a simulation, try setting up some nonzero initial conditions in the circuit.

Figure AD1.11 shows plots of the simulated output voltages. The result of the Fourier analysis demonstrates that the total harmonic distortion of the sine-wave output is approximately 1%.

Bipolar Junction Transistors

In this chapter, we turn our attention to devices that can amplify input signals and act as switches in digital circuits—specifically, the **bipolar junction transistor (BJT)**. In the next chapter, we discuss another very important device, the **metal–oxide–semiconductor field-effect transistor (MOSFET or MOS transistor)**.

4

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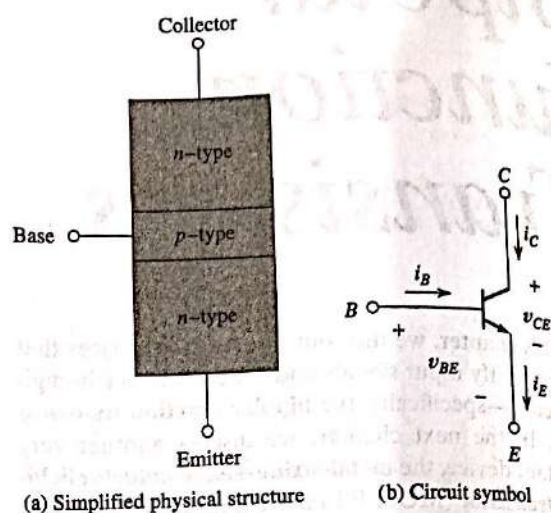


Figure 4.1
The *nnp* BJT.

4.1 BASIC OPERATION OF THE *nnp* BIPOLAR JUNCTION TRANSISTOR

An *nnp* BJT consists of a thin layer of *p*-type material between two layers of *n*-type material, as shown in Figure 4.1a. (The figure is simplified compared with real devices. However, the configuration shown approximates the active portion of actual transistors in ICs.) Two *pn* junctions are formed in the device: the collector–base junction and the emitter–base junction. We will see that the current flowing across one junction affects the current in the other junction. It is this interaction that makes the BJT useful as a switch or as an amplifier.

We call the layers the **emitter**, the **base**, and the **collector**, as shown in Figure 4.1a. The circuit symbol for an *nnp* BJT is shown in Figure 4.1b, as well as the reference directions that we use for the currents and voltages in *nnp* BJTs.

Basic Operation in the Active Region

Let us consider how the BJT currents and voltages are related. An *nnp* transistor with variable voltage sources connected is represented in Figure 4.2. Because the emitter terminal is common to both voltage sources, we say that in this circuit the transistor is in a common-emitter configuration.

A *pn* junction is forward biased by applying voltage with the positive polarity on the *p*-side. In normal operation as an amplifier, the base–emitter junction is forward biased, and the base–collector junction is reverse biased. We refer to this as the **active region** of operation. Operation in this region is accomplished by applying $v_{BE} \cong 0.6 \text{ V}$ to forward bias the base–emitter junction. Then, if we have $v_{CE} > v_{BE}$, the base–collector junction is reverse biased, because the voltage across it is given by $v_{BC} = v_{BE} - v_{CE}$.

The emitter current i_E is the current flowing across the forward biased base–emitter junction, and it depends on v_{BE} in exactly the same way that current depends on voltage

An *nnp* BJT consists of a layer of *p*-type material (the base) between two layers of *n*-type material (collector and emitter).

In the active region, the base–emitter junction is forward biased, and the base–collector junction is reverse biased. When used as amplifiers, BJTs operate in the active region.

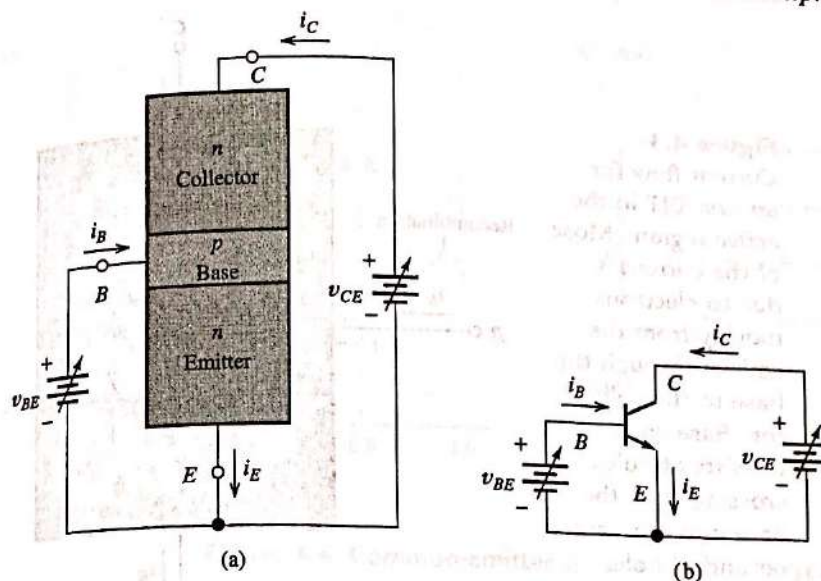


Figure 4.2 An *npn* transistor with variable biasing sources (common-emitter configuration).

for a *pn*-junction diode. In other words, the Shockley equation applies. We introduced the Shockley equation in Chapter 3, and with appropriate changes in notation, it becomes

$$i_E = I_{ES} \left[\exp \left(\frac{v_{BE}}{V_T} \right) - 1 \right] \quad (4.1)$$

Here we have let the emission coefficient n equal unity, because that is the appropriate value for most junction transistors. Typical values for the saturation current I_{ES} range from 10^{-12} to 10^{-17} A, depending on the junction area and other factors. Recall that at a temperature of 300 K, V_T is approximately 26 mV.

The emitter region is doped very heavily compared with the base. Because of the heavier doping, the free-electron concentration in the emitter is much greater than the hole concentration in the base. Therefore, the current i_E crossing the base-emitter junction consists mainly of electrons flowing from the emitter into the base.

The electrons that cross the junction become minority carriers in the base region, and they diffuse away from the emitter junction toward the collector junction. When the electrons reach the depletion region of the collector junction, they are pulled into the collector region by the electric field. (Recall that the electric field in the depletion region points from the *n*-side toward the *p*-side.)

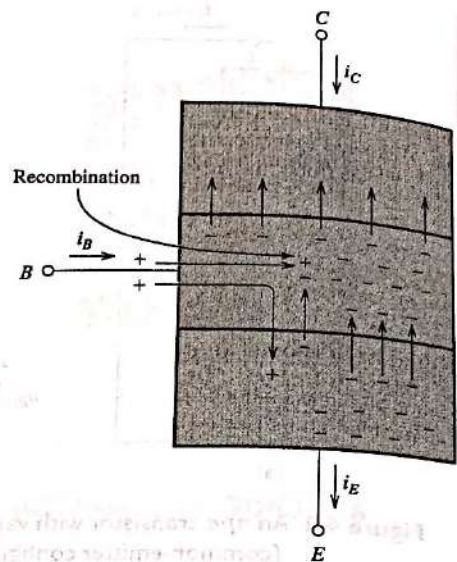
The base region is very thin, and very little recombination occurs in the base. Thus, most of the electrons entering the base are eventually swept into the collector.

A small fraction of the current crossing the base-emitter junction is supplied through the base terminal. There are several reasons for this. First, part of the current crossing the base-emitter junction consists of holes crossing from the base to the emitter, and these holes are resupplied through the base terminal. Another contribution to the base

... the current i_E crossing the base-emitter junction consists mainly of electrons flowing from the emitter into the base.

... most of the electrons entering the base are eventually swept into the collector.

Figure 4.3
Current flow for an *npn* BJT in the active region. Most of the current is due to electrons moving from the emitter through the base to the collector. Base current consists of holes crossing from the base into the emitter and of holes that recombine with electrons in the base.



current is due to electrons that combine with holes in the base region. In a typical BJT, the base current is on the order of 1% of the emitter current. The flow of charge carriers in the *npn* BJT is illustrated in Figure 4.3.

To summarize, applying forward bias to the base-emitter junction causes current to flow across the junction. However, most of this current is supplied by i_C rather than by i_B . In suitable circuits, this effect can amplify a signal applied to the base-emitter junction.

First-Order Common-Emitter Characteristics

Figure 4.4 shows the characteristic curves of a typical BJT. (These curves are somewhat idealized in that only the main features are shown. Later, we consider several secondary effects that result in slight changes in the curves.)

Notice that the input characteristic (i_B versus v_{BE}) is similar to the forward-bias characteristic of a *pn* junction. This is to be expected, because the emitter current is described by the Shockley equation, and the base current is a small fraction of the emitter current. As in a junction diode, the base-to-emitter voltage for a given current decreases with temperature by about 2 mV/K.

The output characteristics show that the collector current is independent of the collector-to-emitter voltage v_{CE} , as long as v_{CE} is greater than about 0.2 V. Let us consider why this is true.

First, assume that v_{CE} is greater than v_{BE} , so that the collector junction is reverse biased. Under this condition, electrons cannot cross from the collector into the base. All electrons that are injected from the emitter into the base must cross the base-emitter junction and travel through the base to the collector.

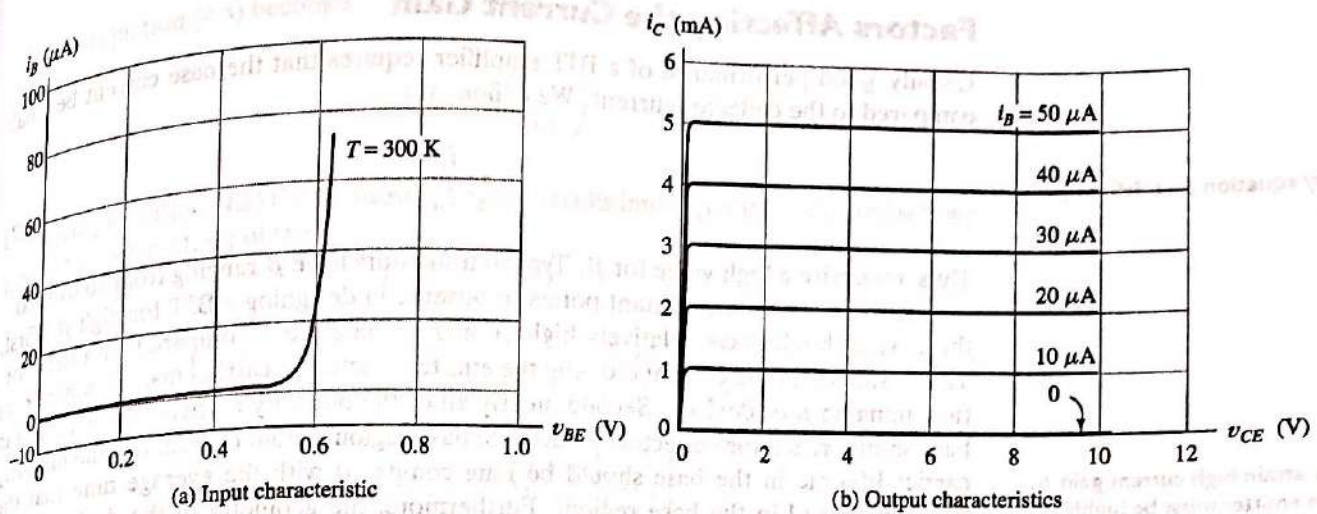


Figure 4.4 Common-emitter characteristics of a typical *npn* BJT.

because of the field in the collector–base depletion region. Thus, the number of electrons flowing into the base region is determined by the voltage applied to the emitter junction. These electrons diffuse to the collector–base depletion region, where they are swept into the collector because of the electric field in the depletion region. Therefore, to a first approximation, the number of electrons flowing into the collector depends only on the degree of forward bias of the emitter junction and is independent of the degree of reverse bias of the collector junction.

For $0.2 < v_{CE} < v_{BE}$, the collector junction is forward biased, but not by more than a few tenths of a volt—not enough to cause significant forward current. Therefore, the collector current is constant for v_{CE} greater than approximately 0.2 V.

Of course, if v_{CE} is reduced toward zero, the collector junction becomes forward biased (assuming that $v_{BE} \cong 0.6$ V). When a *pn* junction is forward biased, we expect to find current flowing out of the *n*-side. Thus, as v_{CE} is reduced to zero, the current i_C becomes smaller and would eventually reverse direction if v_{CE} was reduced below zero.

...to a first approximation, the number of electrons flowing into the collector depends only on the degree of forward bias of the emitter junction and is independent of the degree of reverse bias of the collector junction.

Amplification by the BJT

Refer to Figure 4.4a, and notice that a very small change in the base-to-emitter voltage v_{BE} can result in an appreciable change in the base current i_B , particularly if the base–emitter junction is initially forward biased, so some current (say, $40 \mu\text{A}$) is flowing before the change in v_{BE} is made. Provided that v_{CE} is more than a few tenths of a volt, this change in base current causes a much larger change in the collector current i_C . In suitable circuits, the change in collector current is converted into a much larger voltage change than the initial change in v_{BE} . Thus, the BJT can amplify a signal applied to the base–emitter junction.

Factors Affecting the Current Gain

Usually, good performance of a BJT amplifier requires that the base current be small compared to the collector current. We define

Key equation that defines β .

$$\beta = \frac{i_C}{i_B} \quad (4.2)$$

Thus, we desire a high value for β . Typical transistors have β ranging from 10 to 1000.

To attain high current gain β , the emitter must be highly doped compared with the base, the base must be thin, and recombination in the base region must be minimized.

There are several important points to observe in designing a BJT for high β . First, the device should have relatively high doping in the emitter compared with the base. This ensures that the current crossing the emitter junction is carried mainly by electrons (assuming an *n*pn device). Second, nearly all of the minority carriers injected into the base should reach the collector. Hence, the base region should be thin, and the minority carrier lifetime in the base should be long compared with the average time that the electrons spend in the base region. Furthermore, the geometry of the device should allow the electrons to quickly diffuse to the collector junction, rather than to an external surface where recombination is likely.

Device Equations

Kirchhoff's current law requires that the current flowing out of the BJT is equal to the sum of the currents flowing into it. Thus, referring to Figure 4.2, we have

$$i_E = i_C + i_B \quad (4.3)$$

The BJT parameter α is the ratio of the collector current to the emitter current:

Key equation defining α .

$$\alpha = \frac{i_C}{i_E} \quad (4.4)$$

Values for α range from 0.9 to 0.999, with 0.99 typical. Equation (4.3) indicates that the emitter current is supplied partly through the base terminal and partly through the collector terminal. However, because α is nearly unity, most of the emitter current is supplied by the collector.

Using Equation (4.1) to substitute for i_E in Equation (4.4) and rearranging, we have

$$i_C = \alpha I_{ES} \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \quad (4.5)$$

For v_{BE} greater than a few tenths of a volt, the exponential term inside the brackets is much larger than unity. Then the 1 inside the brackets can be dropped. Also, we define the **scale current** as

$$I_S = \alpha I_{ES} \quad (4.6)$$

and then Equation (4.5) becomes

$$i_C \cong I_s \exp\left(\frac{v_{BE}}{V_T}\right) \quad (4.7)$$

Solving Equation (4.3) for i_C , substituting the results into Equation (4.2), and solving for the base current, we obtain

$$i_B = (1 - \alpha)i_E \quad (4.8)$$

Because α is slightly less than unity, only a very small fraction of the emitter current is supplied by the base. Using Equation (4.1) to substitute for i_E , we get

$$i_B = (1 - \alpha)I_{ES} \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \quad (4.9)$$

Earlier, we defined the parameter β as the ratio of the collector current to the base current. Taking the ratio of Equations (4.4) and (4.8) results in

$$\beta = \frac{i_C}{i_B} = \frac{\alpha}{1 - \alpha} \quad (4.10)$$

Key equation that relates α and β .

Values for β range from about 10 to 1000, and a very common value is $\beta = 100$. We can write

$$i_C = \beta i_B \quad (4.11)$$

Note that because β is large compared to unity, the collector current is an amplified version of the base current.

... because β is large compared to unity, the collector current is an amplified version of the base current.

Example 4.1 Using Device Curves to Determine α and β

Determine the values of α and β for the transistor with the characteristics shown in Figure 4.4.

SOLUTION The value of β can be found by taking the ratio of collector current to base current, provided that v_{CE} is high enough so the collector-base junction is reverse biased. For example, at $v_{CE} = 4$ V and $i_B = 30 \mu\text{A}$, the output characteristics yield $i_C = 3$ mA. Thus,

$$\beta = \frac{i_C}{i_B} = \frac{3 \text{ mA}}{30 \mu\text{A}} = 100$$

(For real devices, slightly different values of β are obtained from different points on the output characteristics.)

Solving Equation 4.10 for α in terms of β , we obtain

$$\alpha = \frac{\beta}{\beta + 1} \quad (4.12)$$

Substituting the value that we found for β , we have $\alpha = 0.99$.

Secondary Effects

So far, we have discussed the basic behavior of the BJT; however, there are several second-order effects that can be important in some applications. Figure 4.5 shows the common-emitter characteristic curves with exaggerated features caused by some of these secondary effects.

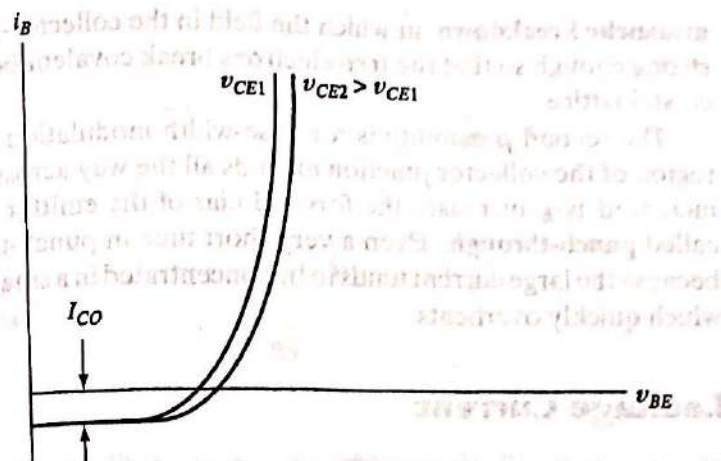
Base-Width Modulation

One feature of the input characteristics is that, rather than a single curve relating i_B and v_{BE} for all values of v_{CE} , there is a family of curves. As v_{CE} becomes larger, the curve for i_B moves lower. Let us consider the reasons for this relationship.

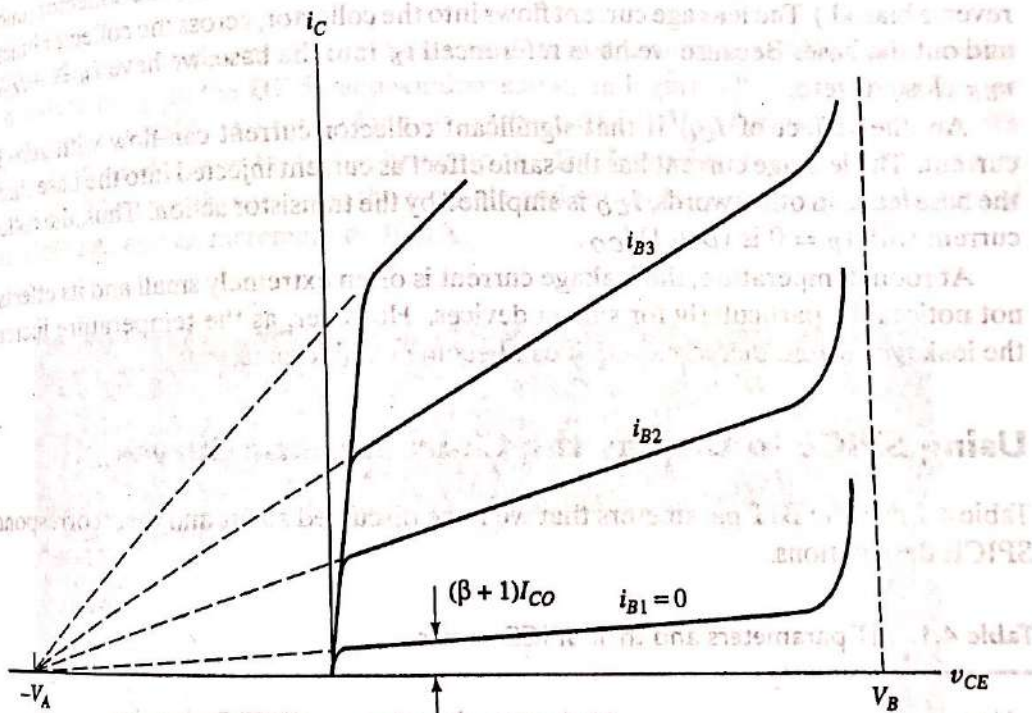
As v_{CE} becomes larger, the reverse bias of the collector junction becomes greater, and the depletion region extends farther into the base. Consequently, the electrons injected from the emitter do not have to diffuse as far before being swept into the collector. The outcome is less recombination in the base region and less base current. The dependence of the base width on v_{CE} is called **base-width modulation**.

Turning to the output characteristic, we see that instead of being horizontal, the curves slope upward for increasing v_{CE} . This is also the result of base-width modulation. As the base becomes narrower and fewer electrons combine with holes, the amount of emitter current must increase to maintain constant base current. (Keep in mind that the output curves are drawn for constant base currents.) Of course, increased emitter current leads to increased collector current.

Assuming constant doping in each region and planar geometry, when the collector characteristics are extended, as shown by the dotted lines in Figure 4.5b, the straight-line extensions all meet at a point on the negative v_{CE} axis. The voltage magnitude at the intersection is called the **Early voltage** and is denoted by V_A .



(a) Input characteristics



(b) Output characteristics

Figure 4.5 Common-emitter characteristics displaying exaggerated secondary effects.

Collector Breakdown

Another effect shown in Figure 4.5b is that the collector current rapidly increases when v_{CE} approaches the breakdown value V_B . Two things can cause this behavior. First is

avalanche breakdown, in which the field in the collector-base depletion region becomes strong enough so that the free electrons break covalent bonds when they collide with the crystal lattice.

The second possibility is for base-width modulation to proceed until the depletion region of the collector junction extends all the way across to the emitter junction. Then, increased v_{CE} increases the forward bias of the emitter junction. This phenomenon is called **punch-through**. Even a very short time in punch-through can destroy the device, because the large current tends to be concentrated in a small region of the emitter junction, which quickly overheats.

Leakage Current

Notice in Figure 4.5a that for $v_{BE} = 0$, the base current is negative. This is caused by the **reverse leakage current** I_{CO} of the collector junction. (I_{CO} can be determined by measuring the collector current with the emitter open circuited and the collector junction reverse biased.) The leakage current flows into the collector, across the collector junction, and out the base. Because we have referenced i_B into the base, we have $i_B \cong -I_{CO}$ for v_{BE} close to zero.

Another effect of I_{CO} is that significant collector current can flow with zero base current. The leakage current has the same effect as current injected into the base through the base lead. In other words, I_{CO} is amplified by the transistor action. Thus, the collector current with $i_B = 0$ is $(\beta + 1)I_{CO}$.

At room temperature, the leakage current is often extremely small and its effects are not noticeable, particularly for silicon devices. However, as the temperature increases, the leakage current increases, and it can become troublesome.

Using SPICE to Display the Characteristic Curves

Table 4.1 lists the BJT parameters that we have discussed so far and their corresponding SPICE designations.

Table 4.1. BJT parameters and their SPICE names.

Name	Mathematical Symbol	SPICE Designation
Common-emitter current gain	β	BF
Scale current	I_s	IS
Early voltage	V_A	VAF

A circuit that can be used in a SPICE simulation to generate the output characteristics of a BJT is illustrated in Figure 4.6. We have used the part **Qbreakn** for the npn BJT. This is called a breakout part by OrCAD and is useful when we want to specify the model parameters for the transistor. To specify these parameters, first we click on the

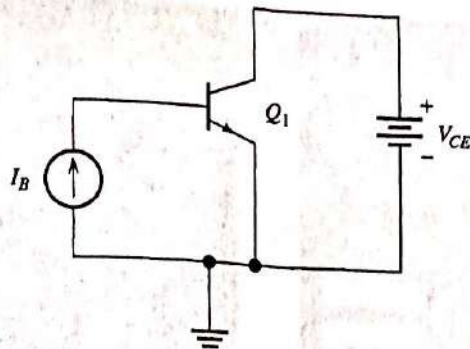


Figure 4.6
Circuit for displaying BJT characteristic curves.

transistor symbol (it turns red), and then we use the **edit/model/edit instance model** command to bring up the window shown in Figure 4.7. Here we have specified $\beta = 100$, $I_S = 10^{-14}$ A, and $V_A = 50$ V. Later, we will learn how to specify additional parameters for the transistor.

Next, we return to the main Schematics window and use the **analysis/setup/dc sweep** commands to bring up the **DC Sweep** window shown in Figure 4.8a. We choose V_{CE} as the main sweep variable and set up for a sweep from 0 to 10 V in 0.01-V increments. We click on the **Nested Sweep** button to bring up the **DC Nested Sweep** window shown in Figure 4.8b. Then we choose i_B as the variable and set up for a start value of 0, an end value of $50 \mu\text{A}$, and an increment of $10 \mu\text{A}$.

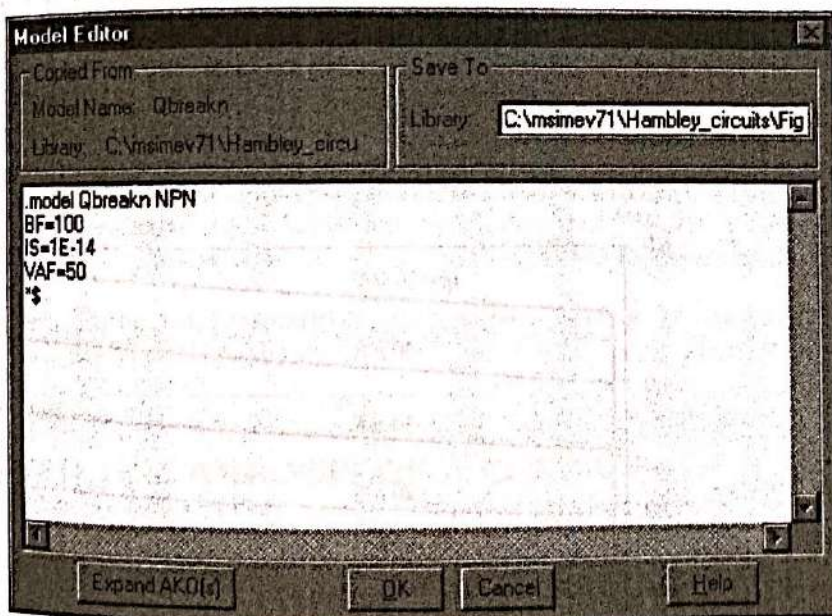


Figure 4.7 Model editor window.

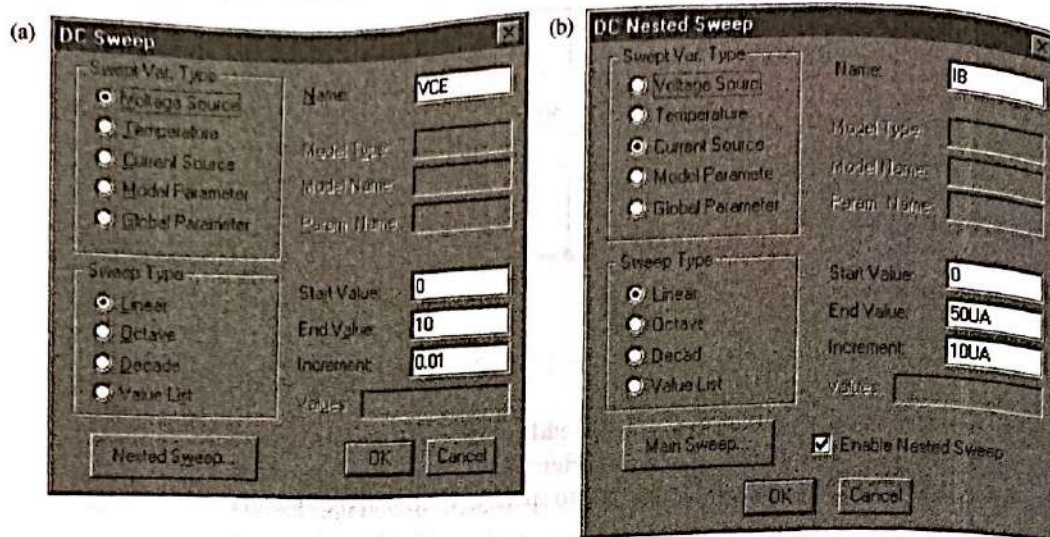


Figure 4.8 Dc-sweep setup windows.

Next, we return to the main Schematic window and use the **analysis/simulate** command to begin the simulation, after which Probe automatically starts. We use the **trace/add** command to bring up the window from which we can select the variable(s) to be plotted. We choose to plot the collector current $I_C(Q1)$, and the resulting display of the collector characteristics is shown in Figure 4.9.

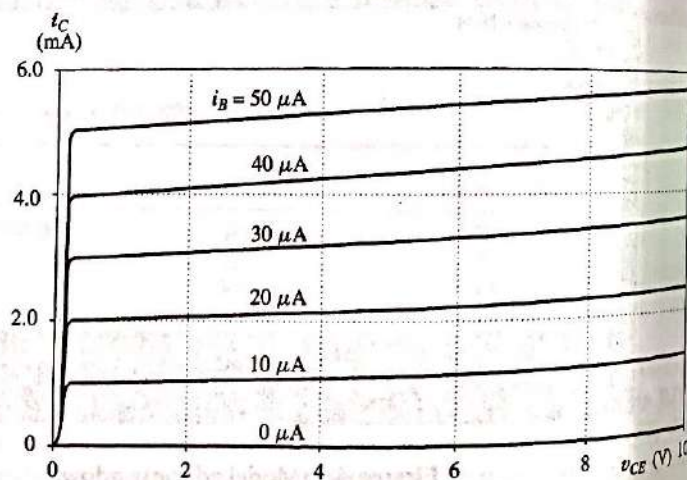


Figure 4.9 Collector characteristics.

EXERCISE

4.1 A certain transistor has $\beta = 50$, $I_{ES} = 10^{-14}$ A, $v_{CE} = 5$ V, and $i_E = 10$ mA. Assume that $V_T = 0.026$ V. Find v_{BE} , v_{BC} , i_B , i_C , and α .

Answer $v_{BE} = 0.718$ V, $v_{BC} = -4.28$ V, $i_B = 0.196$ mA, $i_C = 9.80$ mA, $\alpha = 0.980$.

EXERCISE

4.2 Compute the corresponding values of β if $\alpha = 0.9$, 0.99 , and 0.999 .

Answer $\beta = 9$, 99 , and 999 , respectively.

EXERCISE

4.3 A certain transistor operated with forward bias of the base-emitter junction and reverse bias of the base-collector junction (i.e., operation is in the active region) has $i_C = 9.5$ mA and $i_E = 10$ mA. Find the values of i_B , α , and β .

Answer $i_B = 0.5$ mA, $\alpha = 0.95$, $\beta = 19$.

EXERCISE

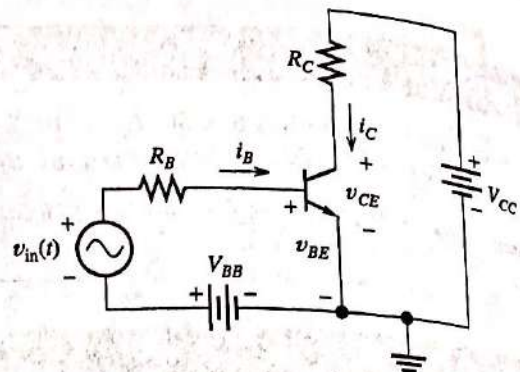
4.4 Neglecting second-order effects, sketch the common-emitter output characteristics of an *npn* small-signal silicon transistor, given that $\beta = 200$. Allow i_B to range from 0 to 50 μ A in 10 - μ A steps.

Answer The output characteristics are identical to Figure 4.4b, except that the values on the i_C axis must be doubled.

4.2 LOAD-LINE ANALYSIS OF A COMMON-EMITTER AMPLIFIER

A simple amplifier circuit is shown in Figure 4.10. The power-supply voltages V_{BB} and V_{CC} bias the device at an operating point for which the amplification of the input signal $v_{in}(t)$ is possible. In this section, we will see that an amplified version of the input signal voltage appears between the collector and ground.

Figure 4.10
Common-emitter
amplifier.



Analysis of the Input Circuit

We can analyze this circuit by using load-line techniques. For example, if we apply Kirchhoff's voltage law to the loop consisting of V_{BB} , $v_{in}(t)$, R_B , and the base-emitter junction, we obtain

$$V_{BB} + v_{in}(t) = R_B i_B(t) + v_{BE}(t) \quad (4.13)$$

A plot of Equation (4.13) is shown as the load line on the input characteristics of the transistor in Figure 4.11a. To establish the load line, we must locate two points. If we assume that $i_B = 0$, then Equation (4.13) yields $v_{BE} = V_{BB} + v_{in}$. This establishes the point where the load line intersects the voltage axis. Similarly, assuming that $v_{BE} = 0$ results in $i_B = (V_{BB} + v_{in})/R_B$, which establishes the load-line intercept on the current axis. The load line is shown as the solid line in Figure 4.11a.

Equation (4.13) represents the constraint placed on the values of i_B and v_{BE} by the external circuit. In addition, i_B and v_{BE} must fall on the device characteristic. The values that satisfy both constraints are the values at the intersection of the load line and the device characteristic.

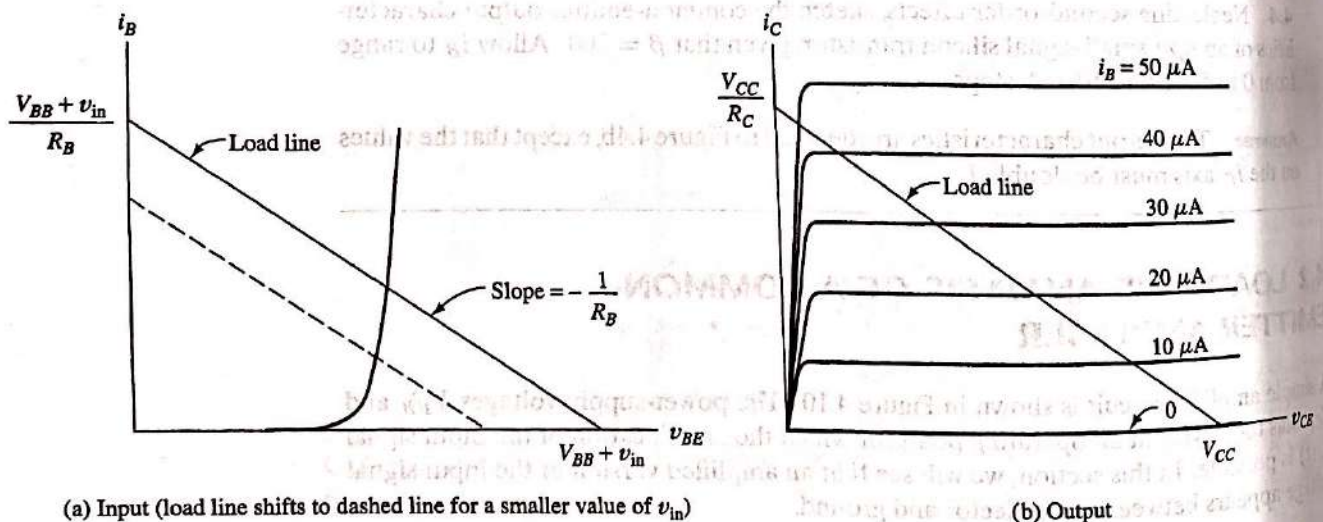


Figure 4.11 Load-line analysis of the amplifier of Figure 4.10.

The slope of the load line is $-1/R_B$. Thus, the load line shifts position, but maintains a constant direction, as v_{in} changes in value. For example, the dashed load line in Figure 4.11a is for a smaller value of v_{in} than that for the solid load line.

The quiescent operating point, or Q -point, corresponds to $v_{in}(t) = 0$. Thus, as the ac input signal $v_{in}(t)$ changes in value with time, the instantaneous operating point swings above and below the Q -point value. Values of i_B can be found from the intersection of the load line with the input characteristic for each value of v_{in} .

Analysis of the Output Circuit

After the input circuit has been analyzed to find values of i_B , a load-line analysis of the output circuit is possible. Referring to Figure 4.10, we can write a voltage equation for the loop through V_{CC} , R_C , and the transistor from collector to emitter. Thus, we have

$$V_{CC} = R_C i_C + v_{CE} \quad (4.14)$$

which is plotted on the output characteristics of the transistor in Figure 4.11b.

Now, with the values of i_B that we have already found by analyzing the input circuit, we can locate the intersection of the corresponding output curve with the load line to find values for i_C and v_{CE} . Thus, as v_{in} swings through a range of values, i_B changes, and the instantaneous operating point swings up and down the load line on the output characteristics. Usually, the ac component of v_{CE} is much larger in amplitude than $v_{in}(t)$, and amplification has taken place.

Examination of Figure 4.11a shows that as $v_{in}(t)$ swings positive, the value of i_B increases (i.e., the intersection of the load line with the input characteristic moves upward). This, in turn, causes the instantaneous operating point to move upward on the output load line, and v_{CE} decreases in value. Thus, a swing in the positive direction for v_{in} results in a (much larger) swing in the negative direction for v_{CE} . Therefore, as well as being amplified, the signal is inverted. In other words, we have an inverting amplifier.

Example 4.2 Graphical Determination of Q -Point and Peak Signal Swings

Suppose that the circuit of Figure 4.10 has $V_{CC} = 10\text{ V}$, $V_{BB} = 1.6\text{ V}$, $R_B = 40\text{ k}\Omega$, and $R_C = 2\text{ k}\Omega$. The input signal is a 0.4-V peak, 1-kHz sinusoid given by $v_{in}(t) = 0.4 \sin(2000\pi t)$. The common-emitter characteristics for the transistor are shown in Figures 4.12a and b. Find the maximum, minimum, and Q -point values for v_{CE} .

SOLUTION First, we must find values for i_B . The load lines for $v_{in} = 0$ (to find the Q -point), $v_{in} = 0.4$ (positive extreme), and $v_{in} = -0.4$ (negative extreme) are shown in Figure 4.12a. The values for the base current are found at the intersections of the load lines with the input characteristic. The (approximate) values are $I_{B\max} \cong 35\text{ }\mu\text{A}$, $I_{BQ} \cong 25\text{ }\mu\text{A}$, and $I_{B\min} \cong 15\text{ }\mu\text{A}$.

Next, the load line is constructed on the output characteristic, as shown in Figure 4.12b. The intersection of the output load line with the characteristic for $I_{BQ} \cong 25\text{ }\mu\text{A}$ establishes the Q -point on the output characteristics. The values are

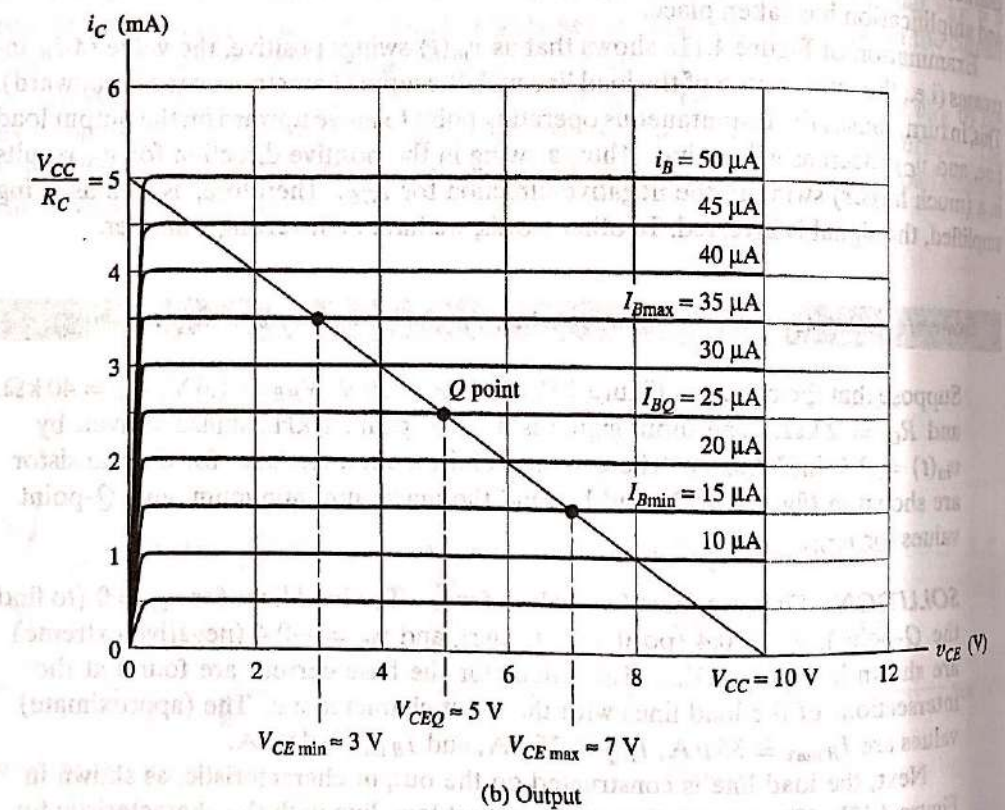
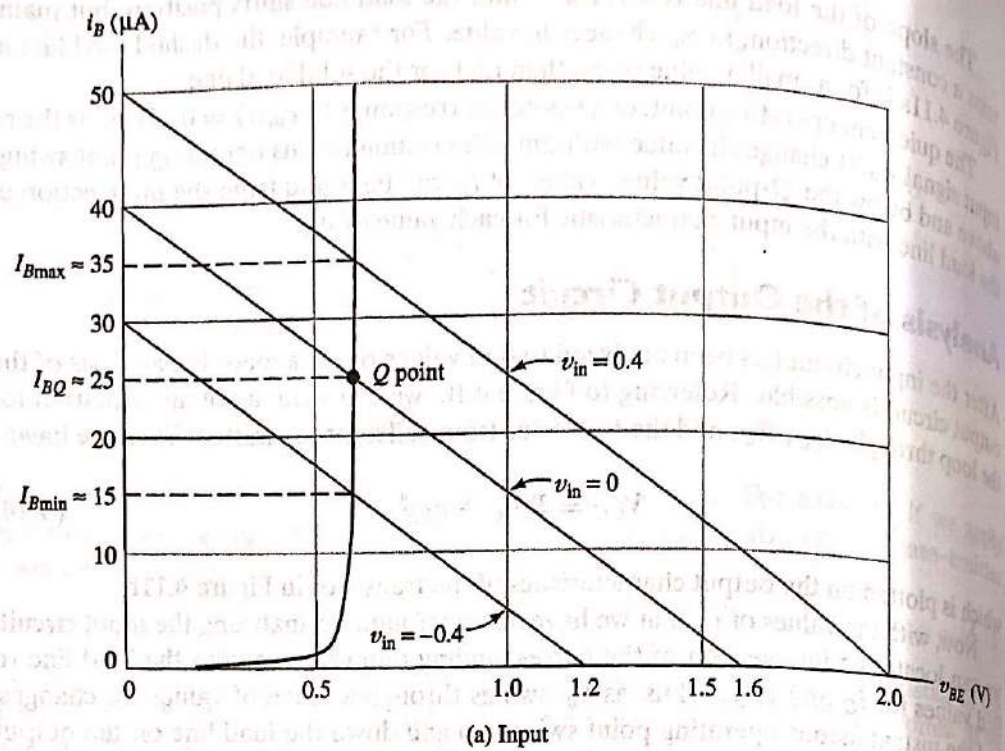


Figure 4.12 Load-line analysis for Example 4.2.

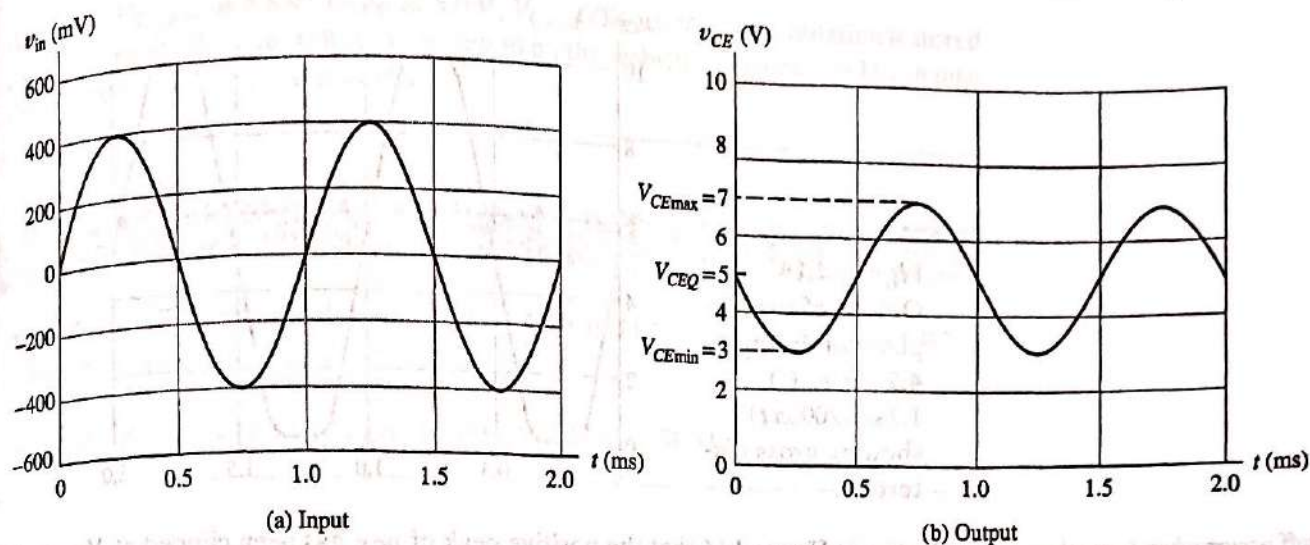


Figure 4.13 Voltage waveforms for the amplifier of Figure 4.10. See Example 4.2.

$I_{CQ} = 2.5 \text{ mA}$ and $V_{CEQ} = 5 \text{ V}$. Similarly, the intersection of the load line with the characteristic for $I_{B \max} \cong 35 \mu\text{A}$ yields $V_{CE \min} \cong 3 \text{ V}$. The opposite extreme is $I_{B \min} \cong 15 \mu\text{A}$, resulting in $V_{CE \max} \cong 7 \text{ V}$.

If more points are found as v_{in} varies with time, we can eventually plot the v_{CE} waveform against time. The waveforms for $v_{in}(t)$ and $v_{CE}(t)$ are illustrated in Figure 4.13. Notice that the ac component of $v_{CE}(t)$ is inverted compared with the input signal.

The peak-to-peak value of the input voltage is 0.8 V , and the peak-to-peak value of the ac component of v_{CE} is 4 V . Thus, the voltage gain magnitude is 5 (i.e., the ac component of v_{CE} is five times larger in amplitude than v_{in}). Usually, we would state the gain as -5 to emphasize the fact that the amplifier inverts the input signal.

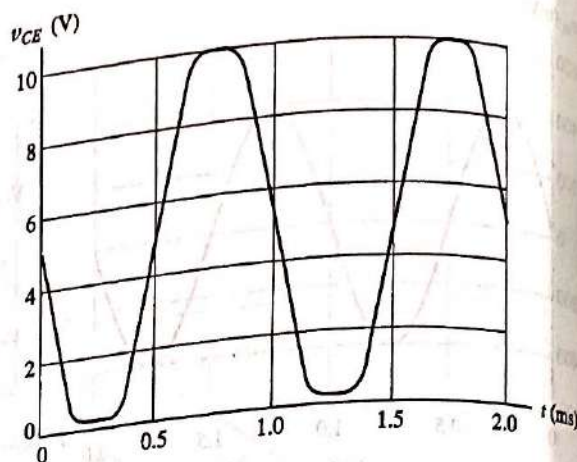
A PSpice circuit file for this example can be found on the website. The file is name is Fig4.10. You can run the simulation to verify the results found in the example and to examine what happens when various parameters are changed. The transistor model parameters are $\beta = \text{BF} = 100$ and $I_s = \text{IS} = 2 \times 10^{-13} \text{ A}$.

Distortion

It is not apparent in the waveforms of Figure 4.13, but unlike the input signal, the output signal is not a precise sine wave. The amplifier is slightly nonlinear, because of curvature and nonuniform spacing of the transistor characteristics. Therefore, as well as being amplified and inverted, the signal is distorted. Of course, distortion is not usually desirable. Figure 4.14 shows the output of the amplifier of Example 4.2 if the input signal is increased in amplitude to 1.2 V peak. The distortion is obvious.

Distortion occurs in BJT amplifiers due to nonlinearity of the input characteristic and nonuniform spacing of the output characteristics. Clipping occurs if the BJT swing reaches saturation or cutoff.

Figure 4.14
Output of the amplifier of Example 4.2 for $v_{in}(t) = 1.2 \sin(2000\pi t)$ showing gross distortion.



Cutoff occurs when i_C reaches zero.

Saturation occurs when v_{CE} reaches approximately 0.2 V.

Reasonably linear amplification occurs only if the signal swing remains in the active region, between saturation and cutoff on the load line.

Notice in Figure 4.14 that the positive peak of v_{CE} has been clipped at $V_{CC} = 10$ V. Clipping occurs when i_B and i_C have been reduced to zero by the negative peaks of the input signal and the instantaneous operating point moves down to the voltage-axis intercept of the output load line. When this happens, we say that the transistor has been driven into **cutoff**.

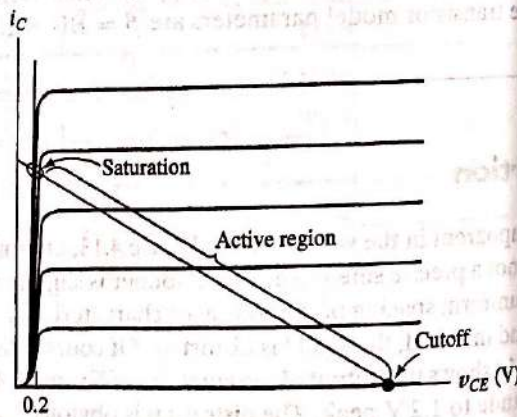
The negative-going peak of the output waveform in Figure 4.14 is clipped at $v_{CE} \approx 0.2$ V. This occurs because i_B becomes large enough so that the circuit's operation is driven into the region at the upper end of the output load line, where the characteristic curves are crowded together. We call this the **saturation region**.

Reasonably linear amplification occurs only if the signal swing remains in the **active region**, between saturation and cutoff on the load line. An output load line is shown in Figure 4.15, including labels for the cutoff, saturation, and active regions.

EXERCISE

4.5 Repeat Example 4.2 if $v_{in}(t) = 0.8 \sin(2000\pi t)$. Find the values of $V_{CE\max}$, V_{CEQ} , and $V_{CE\min}$. Check your answers using DesignLab. The transistor model parameters are $\beta = \beta_F = 100$ and $I_S = 2 \times 10^{-13}$ A.

Figure 4.15
Amplification occurs in the active region. Clipping occurs when the instantaneous operating point enters saturation or cutoff. In saturation, $v_{CE} \approx 0.2$ V.



Answer $V_{CE\max} \cong 8.8\text{ V}$, $V_{CEQ} \cong 5.0\text{ V}$, $V_{CE\min} \cong 1.0\text{ V}$. The simulation is stored in the file named Fig4.10, which can be found on the website. You will need to change the source amplitude for this exercise.

EXERCISE

4.6 Repeat Example 4.2 if $v_{in}(t) = 0.8 \sin(2000\pi t)$ and $V_{BB} = 1.2\text{ V}$. Find the values of $V_{CE\max}$, V_{CEQ} , and $V_{CE\min}$.

Answer $V_{CE\max} \cong 9.8\text{ V}$, $V_{CEQ} \cong 7.0\text{ V}$, and $V_{CE\min} \cong 3.0\text{ V}$.

4.3 THE *pnp* BIPOLAR JUNCTION TRANSISTOR

So far, we have concentrated on the *nnp* BJT, but another useful device results if the base is a layer of *n*-type material between *p*-type emitter and collector regions. For proper operation as an amplifier, the polarities of the dc voltages applied to the *pnp* device must be opposite to those of the *nnp* device. Furthermore, currents flow in opposite directions. Aside from the differences in voltage polarity and current direction, the two types of devices are highly similar.

A diagram of the structure of a *pnp* BJT and the circuit symbol are shown in Figure 4.16. Notice that the arrow on the emitter of the *pnp*-transistor symbol points into the device, which is the normal direction of the emitter current. We have selected the

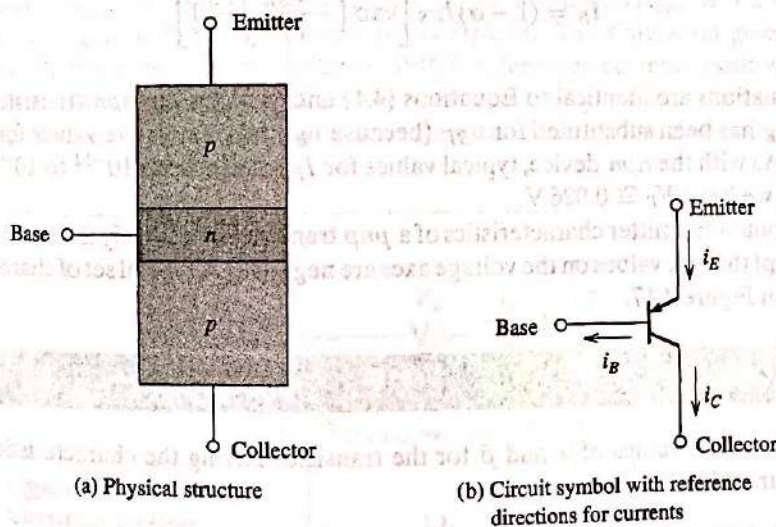


Figure 4.16 The *pnp* BJT.

As a rule SPICE references currents into transistor terminals.

Key equations for either *nnp* or *pnnp* transistors.

reference directions for the currents so that they agree with the actual direction of current flow for the *pnnp* in the active region. For example, current flows *out* of the collector for a *pnnp*. (Recall, however, that current flows *into* the collector for an *nnp*.) As a rule, SPICE references currents into transistor terminals. Keep this in mind when you find an algebraic sign of a current in a SPICE simulation that is opposite to what you expected. Usually, in circuit diagrams we orient *pnnp* transistors with the emitter at the top and *nnp* transistors with the emitter at the bottom. Then current flows from top to bottom in both devices.

For the *pnnp* transistor, we can write the following equations, which are exactly the same as for the *nnp* transistor:

$$i_C = \alpha i_E \quad (4.15)$$

$$i_B = (1 - \alpha) i_E \quad (4.16)$$

$$i_C = \beta i_B \quad (4.17)$$

and

$$i_E = i_C + i_B \quad (4.18)$$

Equations (4.15) through (4.17) are valid only if the base-emitter junction is forward biased (i.e., if v_{BE} is negative for a *pnnp*) and the collector-base junction is reverse biased (if v_{BC} is positive for a *pnnp*). As with the *nnp* transistor, typical values are $\alpha \cong 0.99$ and $\beta \cong 100$.

For the *pnnp* transistor in the active region, we have

$$i_E = I_{ES} \left[\exp \left(\frac{-v_{BE}}{V_T} \right) - 1 \right] \quad (4.19)$$

and

$$i_B = (1 - \alpha) I_{ES} \left[\exp \left(\frac{-v_{BE}}{V_T} \right) - 1 \right] \quad (4.20)$$

Except for voltage polarities and current directions, *pnnp* BJTs are very similar to *nnp* BJTs.

These equations are identical to Equations (4.1) and (4.9) for the *nnp* transistor, except that $-v_{BE}$ has been substituted for v_{BE} (because v_{BE} takes negative values for the *pnnp* device). As with the *nnp* device, typical values for I_{ES} range from 10^{-12} to 10^{-17} A, and at 300 K, we have $V_T \cong 0.026$ V.

The common-emitter characteristics of a *pnnp* transistor are exactly the same as for the *nnp*, except that the values on the voltage axes are negative. A typical set of characteristics is shown in Figure 4.17.

EXERCISE

4.7 Find the values of α and β for the transistor having the characteristics shown in Figure 4.17.

Answer $\alpha = 0.980$, $\beta = 50$.

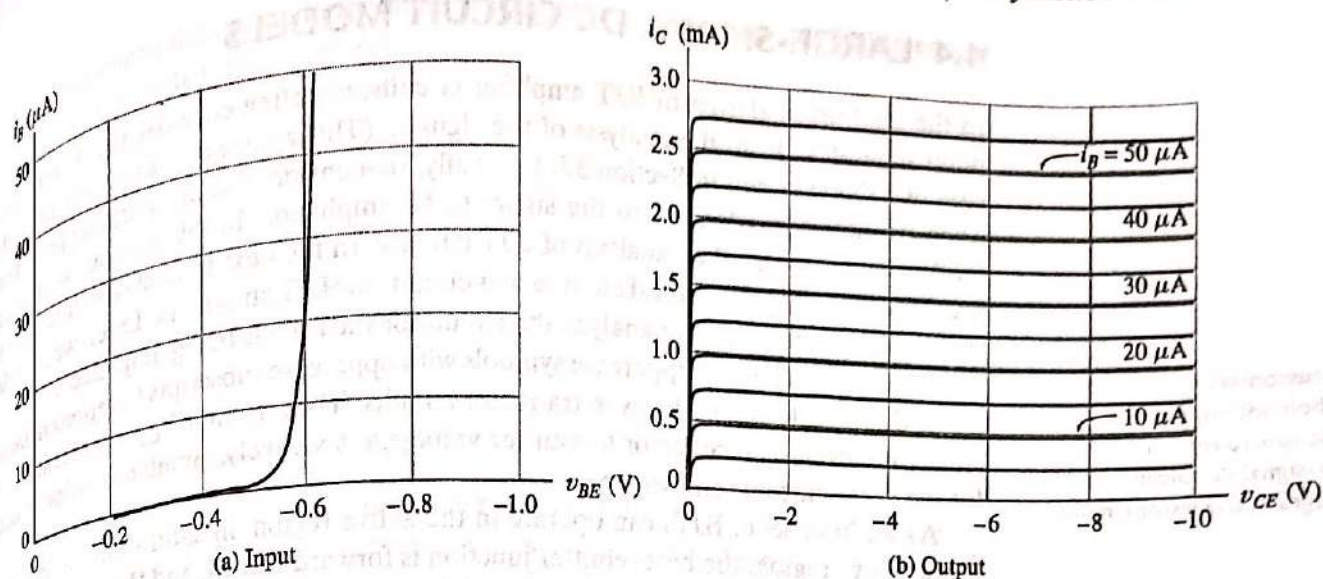


Figure 4.17 Common-emitter characteristics for a *pn*p BJT.

EXERCISE

4.8 Use load-line analysis to find the maximum, minimum, and Q -point values of i_B and $v_O(t)$ for the amplifier circuit shown in Figure 4.18. Use the characteristics shown in Figure 4.17. Does this *pn*p common-emitter amplifier invert the signal? Check your answers by simulating the circuit from $t = 0$ to $t = 2$ ms via a SPICE transient analysis. The transistor parameters are $\beta = \text{BF} = 50$ and $I_S = \text{IS} = 10^{-13}$ A.

Answer $I_{B \max} \cong 48 \mu\text{A}$, $I_{BQ} \cong 24 \mu\text{A}$, $I_{B \min} \cong 5 \mu\text{A}$, $V_{O \max} \cong 7.2 \text{ V}$, $V_{OQ} \cong 3.6 \text{ V}$, $V_{O \min} \cong 0.75 \text{ V}$. The circuit file is Fig4_18. The simulation gives negative values for the base currents because SPICE references currents positive into the transistor. The output signal, of course, is inverted. [If you are in doubt about this, sketch the $v_{in}(t)$, $i_B(t)$, and $v_O(t)$ waveforms to scale against time, or look at the waveforms in the simulation.]

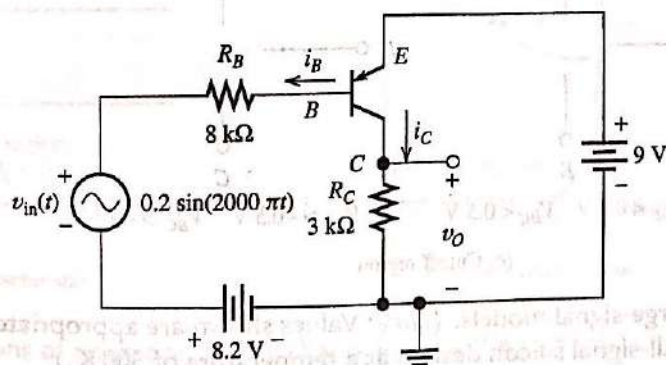


Figure 4.18
Common-emitter
amplifier for Ex-
ercise 4.8.

4.4 LARGE-SIGNAL DC CIRCUIT MODELS

In the analysis or design of BJT amplifier circuits, we often consider the dc operating point separately from the analysis of the signals. (This approach was illustrated in the case of a diode circuit in Section 3.8.) Usually, we consider the dc operating point first. Then we turn our attention to the signal to be amplified. In this section, we present models for large-signal dc analysis of BJT circuits. In the next section, we show how to use these models to design and analyze bias circuits for BJT amplifiers. Later, we consider small-signal models used to analyze the circuit for the signals being amplified.

It is customary to use uppercase symbols with uppercase subscripts to represent large-signal dc currents and voltages in transistor circuits.

It is customary to use uppercase symbols with uppercase subscripts to represent large-signal dc currents and voltages in transistor circuits. Thus, I_C and V_{CE} represent the dc collector current and collector-to-emitter voltage, respectively. Similar notation is used for the other currents and voltages.

As we have seen, BJTs can operate in the active region, in saturation, or in cutoff. In the active region, the base-emitter junction is forward biased, and the base-collector junction is reverse biased. (Actually, the active region includes forward bias of the collector junction by a few tenths of a volt.)

Active-Region Model

Circuit models for BJTs in the active region are shown in Figure 4.19a. A current-controlled current source models the dependence of the collector current on the base

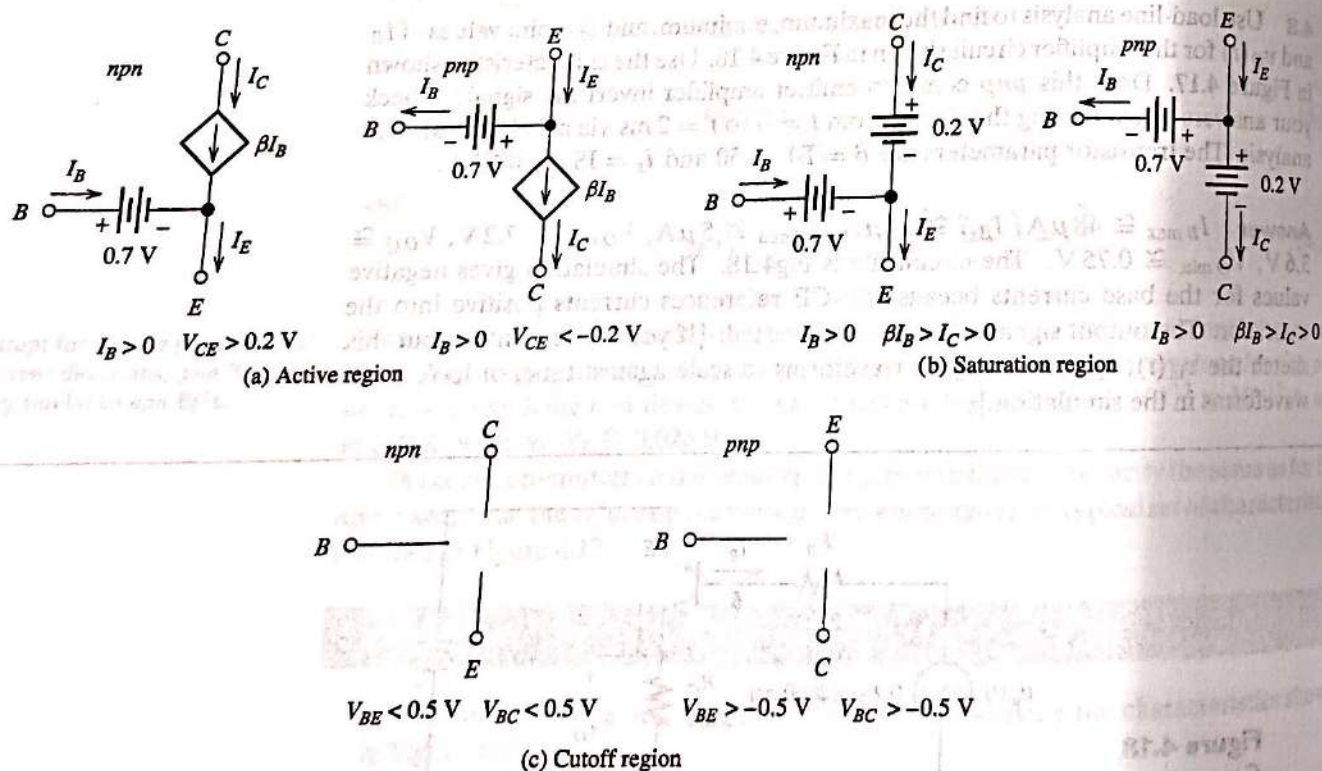


Figure 4.19 BJT large-signal models. (Note: Values shown are appropriate for typical small-signal silicon devices at a temperature of 300 K.)

current. The constraints given in the figure for I_B and V_{CE} must be satisfied to ensure the validity of the active-region model.

Let us relate the active-region model to the device characteristics. Figure 4.20 shows the characteristic curves of an *nnp* transistor. The base current I_B is positive and $V_{BE} \cong 0.7$ V for forward bias of the base-to-emitter junction, as shown in Figure 4.20b. Notice in Figure 4.20a that V_{CE} must be greater than about 0.2 V to ensure that the BJT operates in the active region (i.e., above the *knees* of the characteristic curves).

Similarly, for the *pnp* BJT, we must have $I_B > 0$ and $V_{CE} < -0.2$ V for validity of the active-region model. (As usual, we assume that I_B is referenced positive out of the base for the *pnp* BJT.)

Saturation-Region Model

The BJT models for the saturation region are shown in Figure 4.19b. In the saturation region, both junctions are forward biased. Examination of the collector characteristics in Figure 4.20a shows that $V_{CE} \cong 0.2$ V for an *nnp* transistor in saturation. Thus, the model for the saturation region includes a 0.2-V source between collector and emitter. As in the active region, I_B is positive. Also, we see in Figure 4.20a that, for operation below the knee of the collector characteristic, the constraint is $\beta I_B > I_C > 0$.

Cutoff-Region Model

In cutoff, both junctions are reverse biased, and no current flows in the device. Thus, the model consists of open circuits among all three terminals, as shown in Figure 4.19c. (Actually, if small forward-bias voltages of up to about 0.5 V are applied, the currents are often negligible, and we still use the cutoff-region model.) The constraints on the voltages for the BJT to be in the cutoff region are shown in the figure.

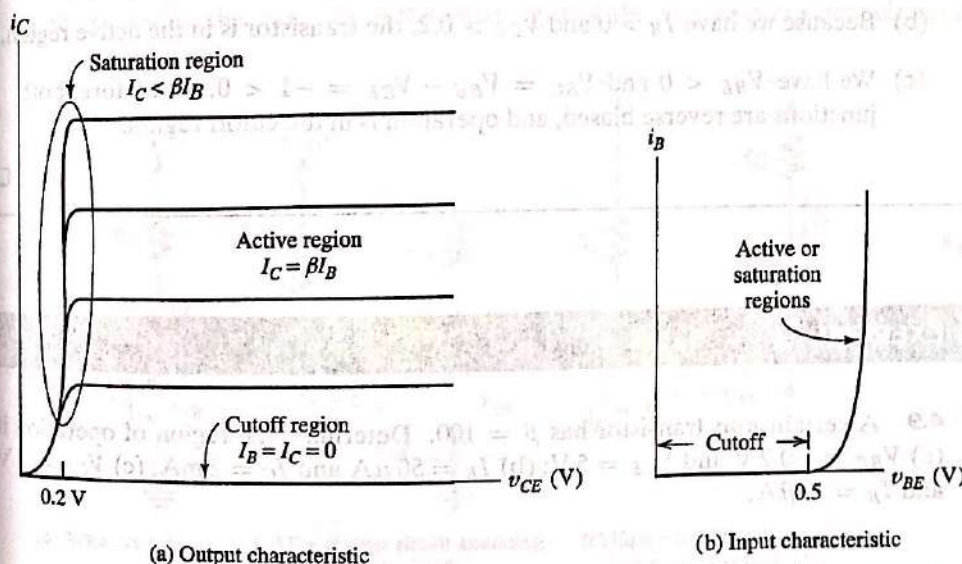


Figure 4.20 Regions of operation on the characteristics of an *nnp* BJT.

Inverted Mode

When the collector–base junction is reverse biased and the base–emitter junction is forward biased, we say that the transistor is operating in the **forward mode**, or **normal mode**. Sometimes we encounter situations in which the base–collector junction is forward biased and the base–emitter junction is reverse biased. This is the opposite of the normal situation, and we say that the transistor is operating in **inverted mode**, or **reverse mode**. In principle, operation in inverted mode is the same as in the normal mode, but with the collector and emitter interchanged. Most devices are not symmetrical, so α and β take different values for inverted mode than for the normal mode. For now, we concentrate our attention on the circuit's operation in the saturation, cutoff, and normal-mode active regions.

Example 4.3 Determination of BJT Operating Region

A given *npn* transistor has $\beta = 100$. Determine the region of operation if (a) $I_B = 50 \mu\text{A}$ and $I_C = 3 \text{ mA}$; (b) $I_B = 50 \mu\text{A}$ and $V_{CE} = 5 \text{ V}$; (c) $V_{BE} = -2 \text{ V}$ and $V_{CE} = -1 \text{ V}$.

SOLUTION

- (a) Because I_B and I_C are positive, the transistor is in either the active or saturation region. The constraint for saturation, namely, $\beta I_B > I_C$ is met, so the device is in saturation.
- (b) Because we have $I_B > 0$ and $V_{CE} > 0.2$, the transistor is in the active region.
- (c) We have $V_{BE} < 0$ and $V_{BC} = V_{BE} - V_{CE} = -1 < 0$. Therefore, both junctions are reverse biased, and operation is in the cutoff region.

EXERCISE

4.9 A certain *npn* transistor has $\beta = 100$. Determine the region of operation if (a) $V_{BE} = -0.2 \text{ V}$ and $V_{CE} = 5 \text{ V}$; (b) $I_B = 50 \mu\text{A}$ and $I_C = 2 \text{ mA}$; (c) $V_{CE} = 5 \text{ V}$ and $I_B = 50 \mu\text{A}$.

Answer (a) cutoff; (b) saturation; (c) active.

4.5 LARGE-SIGNAL DC ANALYSIS OF BJT CIRCUITS

In Section 4.4, we presented large-signal dc models for the BJT. In this section, we use those models to analyze circuits.

In the dc analysis of BJT circuits, we first assume that the operation of the transistor is in a particular region (i.e., active, cutoff, or saturation). Then we use the appropriate model for the BJT and solve the circuit. Next, we check to see if the solution satisfies the constraints for the region assumed. If so, the analysis is complete. If not, we assume operation in a different region, repeating until a valid solution is found. (This is very similar to the analysis of diode circuits using the ideal-diode model.)

This approach is particularly useful in the analysis and design of bias circuits for BJT amplifiers. The objective of a bias circuit is to place the operating point in the active region, so that the signals can be amplified. Because BJTs show considerable variation of parameters—particularly β —from unit to unit and with temperature, it is important for the bias point to be independent of these variations.

The next several examples illustrate the techniques for the large-signal analysis of BJT circuits and provide several observations that are useful in bias-circuit design.

Step 1: Assume an operating region for the BJT.
 Step 2: Solve the circuit to find I_C , I_B , and V_{CE} .
 Step 3: Check to see if the values found in Step 2 are consistent with the assumed operating state. If so the solution is complete; otherwise return to Step 1.

The objective of a bias circuit is to place the operating point in the active region, so that the signals can be amplified.

Example 4.4 The Fixed-Base Bias Circuit

The dc bias circuit shown in Figure 4.21a has $R_B = 200 \text{ k}\Omega$, $R_C = 1 \text{ k}\Omega$, and $V_{CC} = 15 \text{ V}$. The transistor has $\beta = 100$. Solve for I_C and V_{CE} . Check the analysis with SPICE, using a transistor model having $\text{BF} = 100$ and $\text{IS} = 10^{-13} \text{ A}$.

SOLUTION We will eventually see that the transistor operates in the active region, but we start by assuming that the transistor is cut off to illustrate how to test the initial guess of the operating region. Because we assume operation in cutoff, the model for the transistor is shown in Figure 4.19c, and the equivalent circuit is

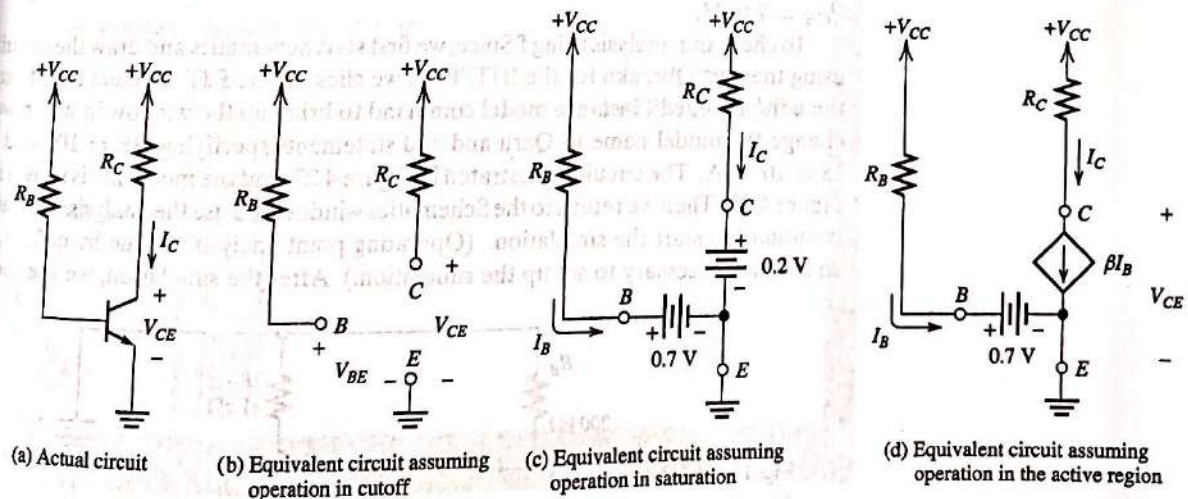


Figure 4.21 Bias circuit of Examples 4.4 and 4.5.

shown in Figure 4.21b. We reason that $I_B = 0$ and that there is zero voltage drop across R_B . Hence, we conclude that $V_{BE} = 15\text{ V}$. However, in cutoff, we must have $V_{BE} < 0.5$ for an *npn* transistor. Therefore, we conclude that the cutoff assumption is invalid.

Next, let us assume that the transistor is in saturation. The transistor model is shown in Figure 4.19b, and the equivalent circuit is shown in Figure 4.21c, from which we obtain

$$I_C = \frac{V_{CC} - 0.2}{R_C} = 14.8\text{ mA}$$

and

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\text{ }\mu\text{A}$$

Checking the conditions required for saturation, we find that $I_B > 0$ is met, but $\beta I_B > I_C$ is not met. Therefore, we conclude that the transistor is not in saturation.

Finally, if we assume that the transistor operates in the active region, we use the BJT model of Figure 4.19a, and the equivalent circuit is shown in Figure 4.21d, from which we get

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\text{ }\mu\text{A}$$

and

$$I_C = \beta I_B = 7.15\text{ mA}$$

Finally,

$$V_{CE} = V_{CC} - R_C I_C = 7.85\text{ V}$$

The requirements for the active region are $V_{CE} > 0.2\text{ V}$ and $I_B > 0$, which are met. Thus, the transistor operates in the active region with $I_C = 7.15\text{ mA}$ and $V_{CE} = 7.85\text{ V}$.

To check our analysis using PSpice, we first start Schematics and draw the circuit using the part Qbreakn for the BJT. Then we click on the BJT to select it and use the **edit/model/edit instance model** command to bring up the window in which we change the model name to Qarh and add statements specifying $\text{BF} = 100$ and $\text{IS} = 10^{-13}\text{ A}$. The circuit is illustrated in Figure 4.22, and the model file is shown in Figure 4.23. Then we return to the Schematics window and use the **analysis/simulate** command to start the simulation. (Operating point analysis is done by default, so it is not necessary to set up the simulation.) After the simulation, we use the

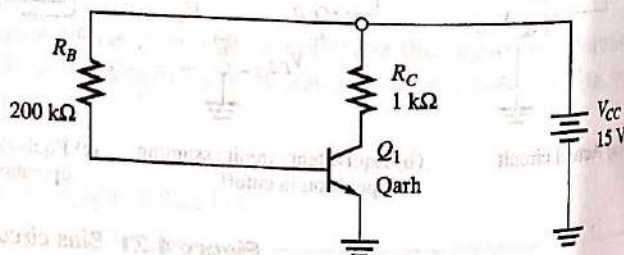


Figure 4.22
Circuit for
Example 4.4.

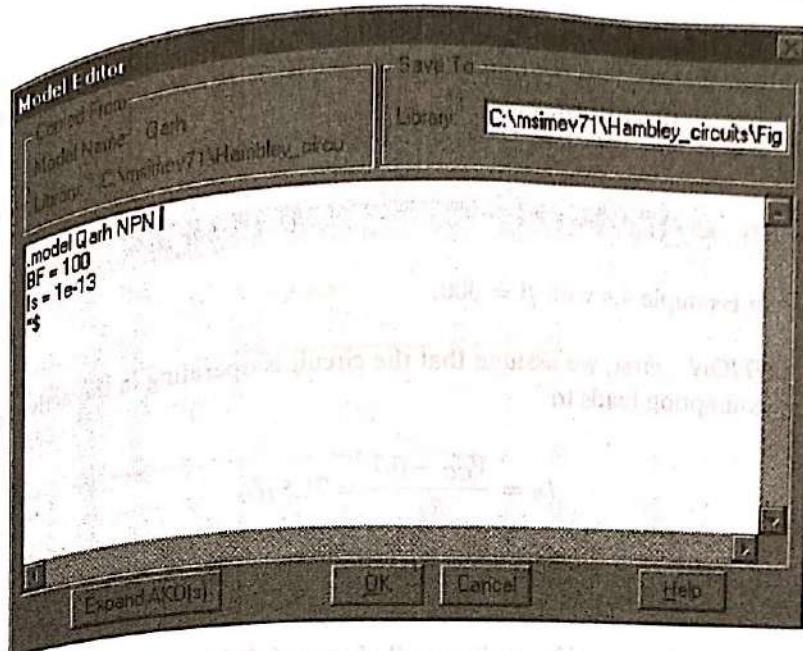


Figure 4.23 Model-editor window.

analysis/examine output command to bring up a window containing the output file. Scrolling down the file eventually reveals the information displayed in Figure 4.24. We see that the simulation yields $I_C = 7.18 \text{ mA}$ and $V_{CE} = 7.82$, which are very close to the values that we obtained earlier. (The slight discrepancy is due to the fact

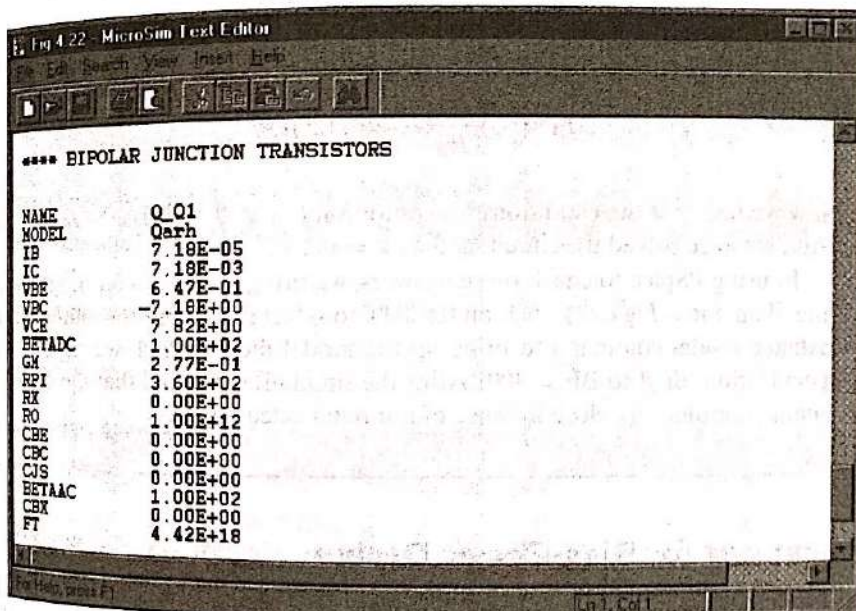


Figure 4.24 SPICE results for the circuit of Figure 4.22.

that we assumed $V_{BE} = 0.7\text{ V}$, which is not exact for this transistor in this circuit. Because resistors typically have tolerances of $\pm 5\%$, the differences in the values would not be of concern in design.)

Example 4.5 The Fixed-Base Bias Circuit with Higher Beta

Repeat Example 4.4 with $\beta = 300$.

SOLUTION First, we assume that the circuit is operating in the active region. This assumption leads to

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\text{ }\mu\text{A}$$

$$I_C = \beta I_B = 21.45\text{ mA}$$

and

$$V_{CE} = V_{CC} - R_C I_C = -6.45\text{ V}$$

One of the requirements for the active region is $V_{CE} > 0.2\text{ V}$, which is not met. Thus, the transistor is not operating in the active region.

Next, we assume that the transistor is in saturation. This assumption leads to

$$I_C = \frac{V_{CC} - 0.2}{R_C} = 14.8\text{ mA}$$

and

$$I_B = \frac{V_{CC} - 0.7}{R_B} = 71.5\text{ }\mu\text{A}$$

Now we find that the conditions for saturation ($I_B > 0$ and $\beta I_B > I_C$) are met. Thus, we have solved the circuit, and $V_{CE} = 0.2\text{ V}$.

In using PSpice to check these answers, we bring up the circuit in Schematics (the file name is Fig4.22), click on the BJT to select it, and use the **edit/model/edit instance model** command to bring up the model file, in which we change the specification for β to $\text{BF} = 300$. After the simulation, we find that the output file contains results very close to those of our hand calculations.

Implications for Bias-Circuit Design

It is instructive to consider the load-line constructions shown in Figure 4.25 for the last two examples. For $\beta = 100$, the operating point is approximately in the center of the load line. On the other hand, for $\beta = 300$, the operating point has moved up into saturation.

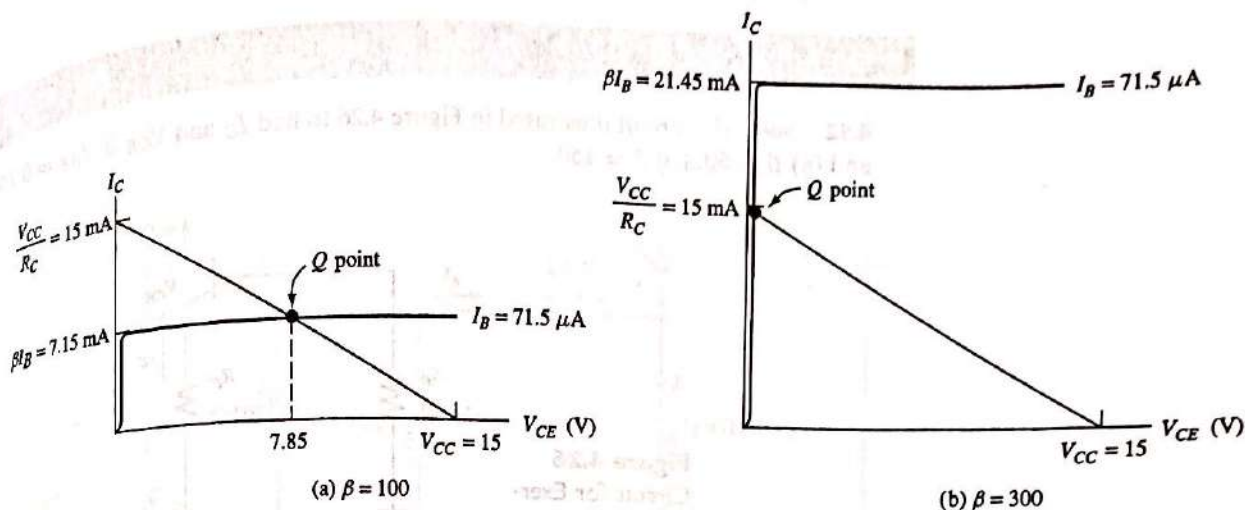


Figure 4.25 Load lines for Examples 4.4 and 4.5.

To use this circuit as an amplifier, we need a Q -point in the active region, where changes in base current cause the instantaneous operating point to move up and down the load line. In saturation, the operating point does not move significantly for small changes in base current, and amplification is not attained. Thus, a suitable Q -point is achieved for $\beta = 100$, but not for $\beta = 300$. Because unit-to-unit variations in β are often of this magnitude, the circuit we are examining is not suitable as an amplifier bias circuit for mass production. (We could consider adjusting R_B to compensate for unit-to-unit variations in β , but this is usually not practical.)

Sometimes such a circuit (Figure 4.21a) is called a **fixed-base bias circuit** because the base current is fixed by V_{CC} and R_B . Thus, the base current does not adjust for changes in β . (Notice that if we want a circuit that achieves a particular operating point on the collector load line, the base current must change when β changes.)

EXERCISE

4.10 Repeat Example 4.4 for (a) $\beta = 50$; (b) $\beta = 250$.

Answer (a) $I_C = 3.575 \text{ mA}$, $V_{CE} = 11.43 \text{ V}$; (b) $I_C = 14.8 \text{ mA}$, $V_{CE} = 0.2 \text{ V}$.

EXERCISE

4.11 Assume that $R_C = 5 \text{ k}\Omega$, $V_{BE} = 0.7 \text{ V}$, and $V_{CC} = 20 \text{ V}$ in the circuit of Figure 4.21a. Solve for the value of R_B needed to place the operating point exactly in the middle of the output load line for (a) $\beta = 100$; (b) $\beta = 300$.

Answer (a) $R_B = 965 \text{ k}\Omega$; (b) $R_B = 2.90 \text{ M}\Omega$.

EXERCISE

4.12 Solve the circuit illustrated in Figure 4.26 to find I_C and V_{CE} if $V_{BE} = 0.7\text{ V}$ and (a) $\beta = 50$; (b) $\beta = 150$.

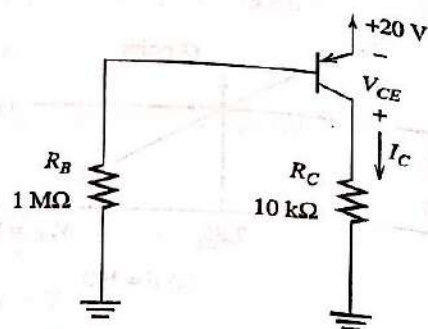


Figure 4.26
Circuit for Exercise 4.12.

Answer (a) $I_C = 0.965\text{ mA}$, $V_{CE} = -10.35\text{ V}$; (b) $I_C = 1.98\text{ mA}$, $V_{CE} = -0.2\text{ V}$.
(The transistor is in saturation.)

In the next example, we consider a circuit that achieves an emitter current that is relatively independent of β .

Example 4.6 A Bias Circuit with Two Voltage Sources

Solve for I_C and V_{CE} in the circuit of Figure 4.27a for $V_{CC} = 15\text{ V}$, $V_{BB} = 5\text{ V}$, $R_C = 2\text{ k}\Omega$, $R_E = 2\text{ k}\Omega$, and $\beta = 100$. Repeat for $\beta = 300$.

SOLUTION We assume that the transistor is in the active region and use the equivalent circuit shown in Figure 4.27b. Writing a voltage equation through V_{BB} , the base-emitter junction, and R_E , we have

$$V_{BB} = 0.7 + I_E R_E$$

This equation can be solved for the emitter current as follows:

$$I_E = \frac{V_{BB} - 0.7}{R_E} = 2.15\text{ mA}$$

Notice that the emitter current does not depend on the value of β .

Substituting $I_C = \beta I_B$ in the equation

$$I_E = I_B + I_C$$

we have

$$I_E = (\beta + 1)I_B$$

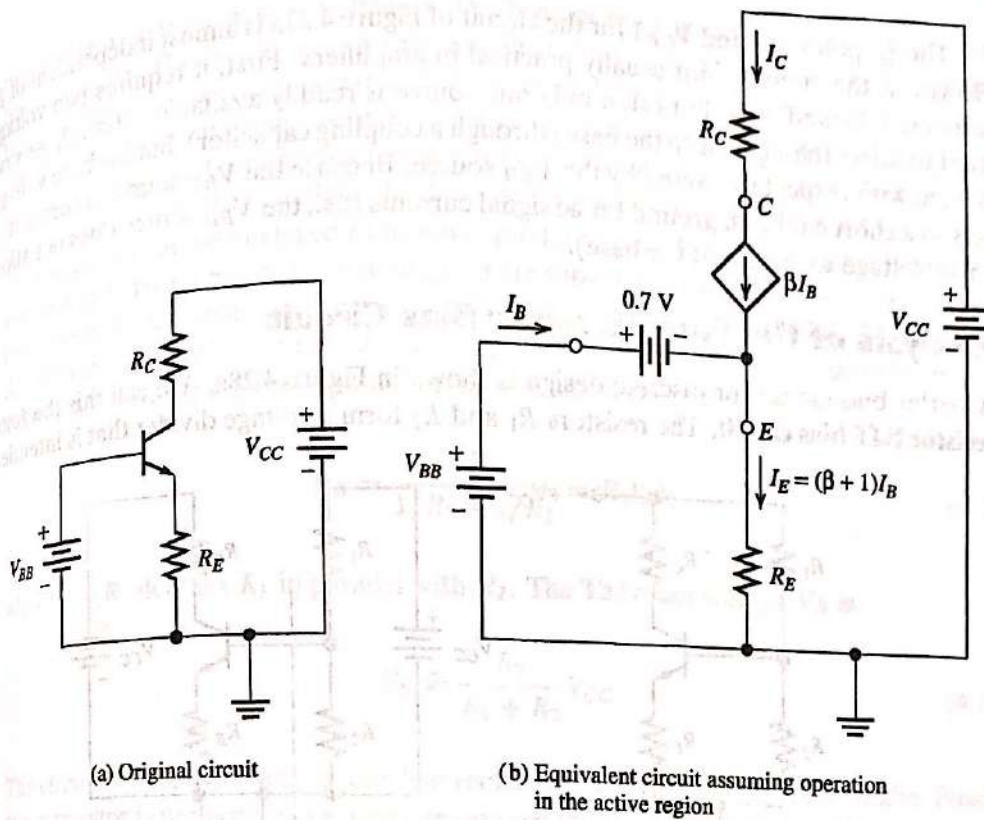


Figure 4.27 Circuit for Example 4.6.

Solving the equation for the base current, we obtain

$$I_B = \frac{I_E}{(\beta + 1)}$$

Once the base current is known, we can compute the collector current by using $I_C = \beta I_B$. Then we can write a voltage equation around the collector loop to find V_{CE} :

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

Substituting values, we obtain the results given in Table 4.1. Notice that I_B is lower for the transistor with higher β and I_C is nearly constant.

Table 4.2. Results for the circuit of Example 4.6.

β	I_B	I_C	V_{CE}
100	$21.3 \mu\text{A}$	2.13 mA	6.44 V
300	$7.14 \mu\text{A}$	2.14 mA	6.42 V

□

The Q -point (I_C and V_{CE}) for the circuit of Figure 4.27a is almost independent of β . However, the circuit is not usually practical in amplifiers. First, it requires two voltage sources, V_{CC} and V_{BB} , but often only one source is readily available. Second, we may want to inject the signal into the base (through a coupling capacitor), but the base voltage is fixed with respect to ground by the V_{BB} source. Because the V_{BB} source is constant, it acts as a short circuit to ground for ac signal currents (i.e., the V_{BB} source does not allow an ac voltage to appear at the base).

Analysis of the Four-Resistor Bias Circuit

A better bias circuit for discrete design is shown in Figure 4.28a. We call this the **four-resistor BJT bias circuit**. The resistors R_1 and R_2 form a voltage divider that is intended

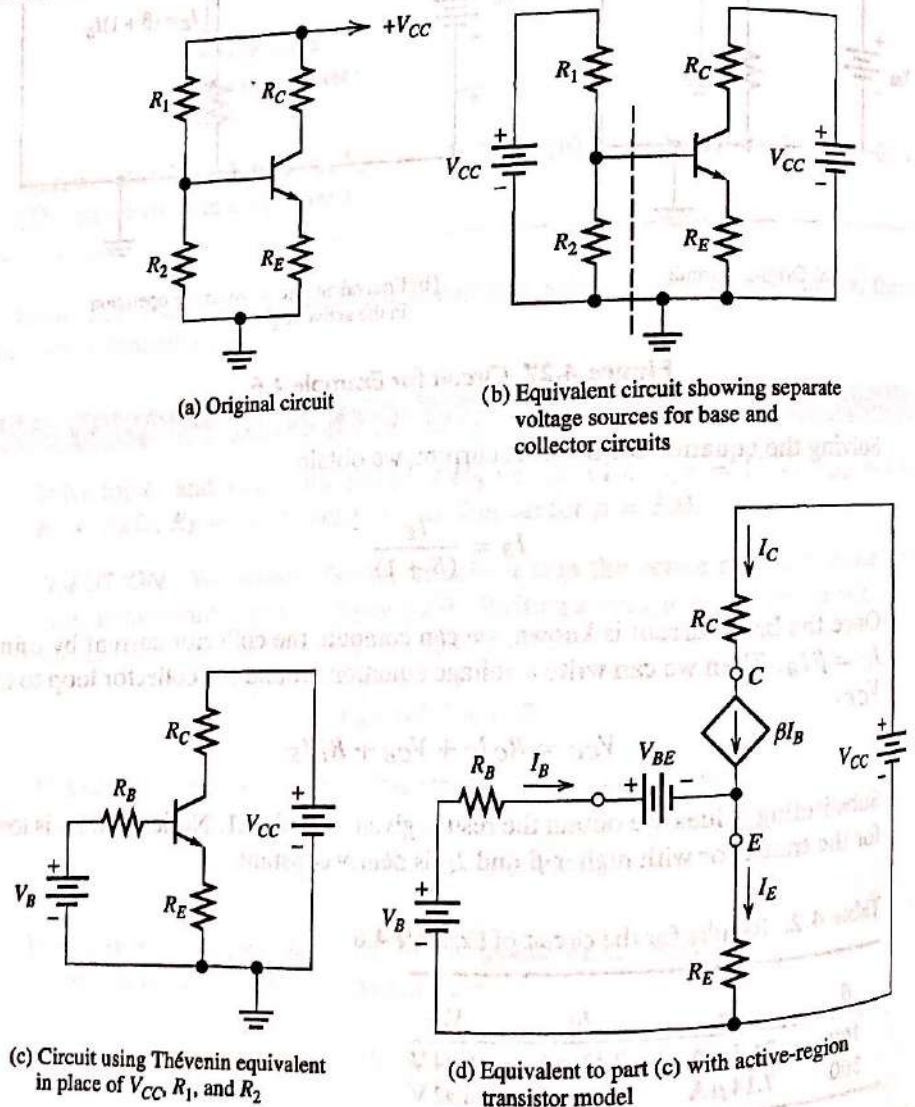


Figure 4.28 Four-resistor bias circuit.

to provide a nearly constant voltage at the base of the transistor (independent of the transistor's β). This is achieved by selecting the values of R_1 and R_2 so that the currents through them are large compared with the expected base current. As we saw in Example 4.6, constant base voltage results in nearly constant values for I_C and V_{CE} . Because the base is not directly connected to the supply or ground in the four-resistor bias circuit, it is possible to couple an ac signal to the base through a coupling capacitor.

The circuit can be analyzed as follows. First, the circuit is redrawn, as illustrated in Figure 4.28b. Two separate voltage supplies are shown as an aid in the analysis to follow, but otherwise the circuits in parts (a) and (b) of the figure are identical. Next, we find the Thévenin equivalent of the circuit to the left of the dashed line in Figure 4.28b. The Thévenin resistance R_B is the parallel combination of R_1 and R_2 , given by

$$R_B = \frac{1}{1/R_1 + 1/R_2} = R_1 || R_2 \quad (4.21)$$

where $R_1 || R_2$ denotes R_1 in parallel with R_2 . The Thévenin voltage V_B is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} \quad (4.22)$$

The circuit with the Thévenin equivalent replacement is displayed in Figure 4.28c. Finally, the transistor is replaced by its active-region model, as shown in Figure 4.28d.

Now we can write a voltage equation around the base loop of Figure 4.28d, resulting in

$$V_B = R_B I_B + V_{BE} + R_E I_E \quad (4.23)$$

Of course, for small-signal silicon transistors at room temperature, we have $V_{BE} \cong 0.7$ V. Now, we can substitute

$$I_E = (\beta + 1) I_B$$

and solve to find that

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E} \quad (4.24)$$

Once I_B is known, I_C and I_E can easily be found. Then we can write a voltage equation around the collector loop of Figure 4.28d and solve for V_{CE} . This yields

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E \quad (4.25)$$

Example 4.7 The Four-Resistor Bias Circuit

Find the values of I_C and V_{CE} in the circuit of Figure 4.29 for $\beta = 100$ and $\beta = 300$. Assume that $V_{BE} = 0.7$ V.

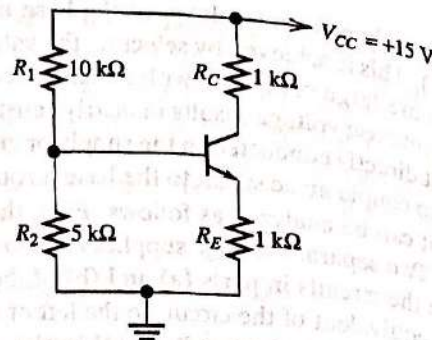


Figure 4.29
Circuit for
Example 4.7.

SOLUTION Substituting into Equations (4.21) and (4.22), we find that

$$R_B = \frac{1}{1/R_1 + 1/R_2} = 3.33 \text{ k}\Omega$$

and

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = 5 \text{ V}$$

Then, substituting into Equation (4.24) and using $\beta = 100$, we have

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} = 41.2 \text{ }\mu\text{A}$$

For $\beta = 300$, we find that $I_B = 14.1 \text{ }\mu\text{A}$. Notice that the base current is significantly smaller for the higher β .

Now we can compute the collector current by using $I_C = \beta I_B$. For $\beta = 100$, we find that $I_C = 4.12 \text{ mA}$, and for $\beta = 300$, we have $I_C = 4.24 \text{ mA}$. Thus, for a 3:1 change in β , the collector current changes by less than 3%. The emitter current is given by $I_E = I_C + I_B$. The results are $I_E = 4.16 \text{ mA}$ for $\beta = 100$ and $I_E = 4.25 \text{ mA}$ for $\beta = 300$.

Finally, Equation (4.25) can be used to find V_{CE} . The results are $V_{CE} = 6.72 \text{ V}$ for $\beta = 100$ and $V_{CE} = 6.51 \text{ V}$ for $\beta = 300$.

EXERCISE

4.13 Repeat Example 4.7 for $R_1 = 100 \text{ k}\Omega$ and $R_2 = 50 \text{ k}\Omega$. Compute the ratio of I_C for $\beta = 300$ to I_C for $\beta = 100$, and compare it with the ratio of the currents found in Example 4.7. Comment. Use a SPICE simulation to verify your answers. Assume that $I_s = 10^{-14} \text{ A}$.

Answer For $\beta = 100$, $I_C = 3.20 \text{ mA}$ and $V_{CE} = 8.57 \text{ V}$; for $\beta = 300$, $I_C = 3.86 \text{ mA}$ and $V_{CE} = 7.27 \text{ V}$. The ratio of the collector currents is 1.21. On the other hand, in the example, the ratio of the collector currents is only 1.029. Larger values of R_1 and R_2 lead to larger changes in I_C with changes in β .

Discrete Bias-Circuit Design

The four-resistor circuit of Figure 4.28a is commonly used for biasing BJTs in discrete amplifiers. Let us briefly consider the design of this type of bias circuit. The principal goal of bias-circuit design is to achieve nearly identical operating points for the BJTs, even though the BJT parameters may vary significantly from unit to unit. For example, β may vary by a factor of three or more between units. Furthermore, some circuits are required to function over a wide range of temperature, which can cause significant variations in β and V_{BE} .

We found that I_C and V_{CE} are nearly independent of β in the circuit of Example 4.7. This is achieved by selecting values for R_1 and R_2 that provide a nearly constant voltage to the base. As the values of R_1 and R_2 become larger, the Q -point exhibits larger changes with β . (This can be seen by comparing the results of Exercise 4.13 with those of Example 4.7.)

For the voltage divider to provide a nearly constant base voltage for different values of base current, the resistances R_1 and R_2 should be small. However, this leads to large currents, possible overheating, and the need for a larger, more expensive power supply. Thus, we also wish to make R_1 and R_2 as large as possible. As a general rule, a good compromise is to choose R_2 so that the current through it is 10 to 20 times the largest base current expected.

Equation (4.24) shows that the base current is proportional to the difference between V_B and V_{BE} . Recall that V_{BE} decreases in value by about 2 mV/K as the temperature increases. Furthermore, resistor tolerances cause V_B to vary. If we design so that the difference between V_B and V_{BE} is very small, these variations could result in troublesome changes in the Q -point. Therefore, we should design so that V_B is much larger than the changes expected in V_{BE} and V_B due to temperature or resistor tolerances.

Often, we choose V_B to be about one-third of the supply voltage, which is usually large enough to ensure a sufficiently stable Q -point. Usually, V_B is much larger than V_{BE} , so that the drop across R_E is approximately equal to V_B . A rule in common use is to design so that one-third of the supply voltage is dropped across R_C , one-third across the transistor (V_{CE}), and one-third across R_E .

The principal goal of bias-circuit design is to achieve nearly identical operating points for the BJTs, even though the BJT parameters may vary significantly from unit to unit.

As a general rule, a good compromise is to choose R_2 so that the current through it is 10 to 20 times the largest base current expected.

... we should design so that V_B is much larger than the changes expected in V_{BE} and V_B due to temperature or resistor tolerances.

... design so that one-third of the supply voltage is dropped across R_C , one-third across the transistor (V_{CE}), and one-third across R_E .

EXERCISE

4.14 In the four-resistor bias network, does I_{CQ} increase, decrease, or stay about the same for a (small) increase in the value of (a) R_C ; (b) R_E ; (c) R_1 ; (d) R_2 ; (e) β ?

Answer (a) same; (b) decrease; (c) decrease; (d) increase; (e) increase.

EXERCISE

4.15 In the four-resistor bias network, does V_{CEQ} increase, decrease, or stay about the same for a (small) increase in the value of (a) R_C ; (b) R_1 ; (c) R_2 ; (d) β ?

Answer (a) decrease; (b) increase; (c) decrease; (d) decrease.

Current sources and direct coupling are commonly used in biasing IC amplifiers.

Current Sources in Integrated-Circuit Biasing

The four-resistor bias circuit is fine for discrete circuits in which resistors are practical components. However, in integrated circuits, resistors consume excessive chip area, and other methods must be used for biasing. We will see later that transistors and a few resistors can be used to form current sources that are useful in biasing IC amplifiers. We will illustrate this idea with an example containing current sources.

Example 4.8 A Bias Circuit Containing Current Sources

Consider the circuit shown in Figure 4.30. Assume that the transistors Q_1 and Q_2 have identical characteristics. (This is a reasonable assumption for properly designed integrated circuits, but not for discrete circuits.) All of the transistors operate in the active region and have $I_s = 10^{-13}$ A and $\beta = 100$. Solve for the collector currents and V_o .

SOLUTION Transistors Q_1 and Q_2 have identical base-to-emitter voltages (because their emitters are connected together and their bases are connected to ground). Therefore, we have

$$I_{E1} = I_{E2}$$

Also, the sum of the emitter currents must equal 2 mA:

$$I_{E1} + I_{E2} = 2 \text{ mA}$$

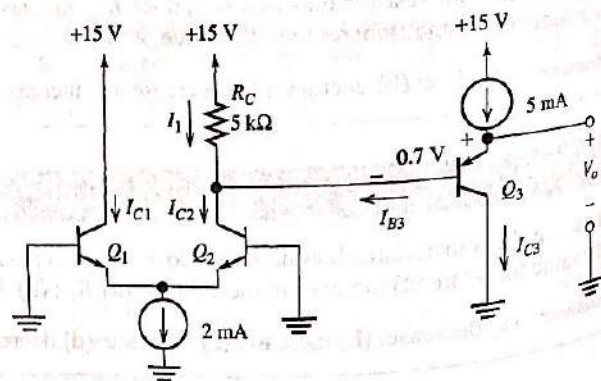
Thus, we have $I_{E1} = I_{E2} = 1 \text{ mA}$. Then we can compute the base currents and the collector currents:

$$I_{B1} = I_{B2} = \frac{I_{E2}}{\beta + 1} = 9.9 \mu\text{A}$$

and

$$I_{C1} = I_{C2} = \beta I_{B2} = 0.99 \text{ mA}$$

Figure 4.30
Current sources
are useful in
biasing IC
amplifiers



Next, we observe that the emitter current of Q_3 is 5 mA. Thus, we have

$$I_{B3} = \frac{I_{E3}}{\beta + 1} = 49.5 \mu\text{A}$$

and

$$I_{C3} = \beta I_{B3} = 4.95 \text{ mA}$$

Next, we can find the current through R_C :

$$I_1 = I_{C2} - I_{B3} = 0.941 \text{ mA}$$

Finally, we can write a voltage equation for the loop consisting of the 15-V source, R_C , the base-emitter of Q_3 , and V_o . The result is

$$V_o = 0.7 - I_1 R_C + 15 = 10.3 \text{ V}$$

This circuit is representative of bias circuits in ICs. □

Of course, we can easily analyze a circuit like Figure 4.30 using SPICE. However, we tend to think about the circuit more when we hand analyze it and therefore gain a better understanding of its operation. To optimize your learning when using SPICE, think about what the results should be, simulate the circuit, and then compare the results with your expectations.

To optimize your learning when using SPICE, think about what the results should be, simulate the circuit, and then compare the results with your expectations.

EXERCISE

4.16 Determine the voltage at the top end of the 2-mA current source shown in Figure 4.30.

Answer $V_{2\text{mA}} = -0.7 \text{ V}$.

EXERCISE

4.17 Analyze the circuit of Figure 4.30, assuming that the junction area of Q_2 is twice as large as that of Q_1 , so that we have $I_{E2} = 2I_{E1}$. The BJTs have $\beta = 100$ and $|V_{BE}| = 0.7 \text{ V}$.

Answer $I_{C1} = 0.660 \text{ mA}$, $I_{C2} = 1.32 \text{ mA}$, and $V_o = 9.35 \text{ V}$.

EXERCISE

4.18 Assuming that both transistors have $\beta = 100$ and $|V_{BE}| = 0.7 \text{ V}$, determine the value of V_o in the circuit of Figure 4.31.

Answer $V_o = -2.68 \text{ V}$.

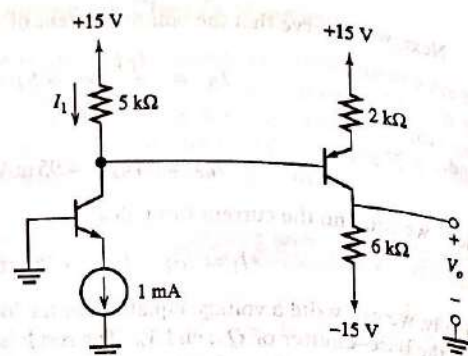


Figure 4.31
Circuit for
Exercise 4.18.

4.6 SMALL-SIGNAL EQUIVALENT CIRCUITS

Signal Notation

Now we turn our attention to the signal currents and voltages in BJT amplifier circuits. First, we establish the notation used for currents and voltages. We denote the total currents and voltages by lowercase symbols with uppercase subscripts. Thus, $i_B(t)$ is the total base current as a function of time.

The Q -point currents and voltages are denoted by uppercase symbols with uppercase subscripts. Hence, I_{BQ} is the dc base current when the input signal is zero.

Finally, we denote the changes in currents and voltages from the Q -point (due to the input signal being amplified) by lowercase symbols with lowercase subscripts. Thus, $i_b(t)$ denotes the signal component of the base current. Because the total base current is the sum of the Q -point value and the signal component, we can write

$$i_B(t) = I_{BQ} + i_b(t) \quad (4.26)$$

These quantities are illustrated in Figure 4.32. Similarly, we can write

$$v_{BE}(t) = V_{BEQ} + v_{be}(t) \quad (4.27)$$

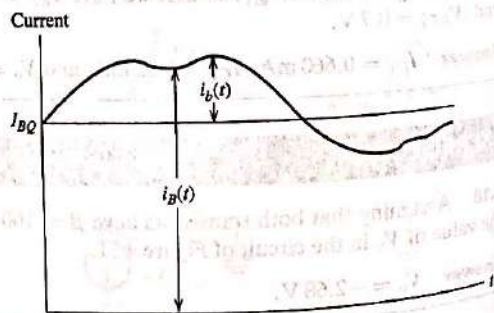


Figure 4.32
Illustration of the
 Q -point base cur-
rent I_{BQ} , signal
current $i_b(t)$, and
total current $i_B(t)$.

Small-Signal Current-Voltage Relationships

Q -points are established by bias circuits, as discussed in the preceding section. Now we consider how the (small) signal components are related in the BJT. The base current is given in terms of the base-to-emitter voltage by Equation 4.9, which is repeated here for convenience:

$$i_B = (1 - \alpha) I_{ES} \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \quad (4.28)$$

We are concerned with the circuit's operation in the active region, for which the 1 inside the brackets is negligible and can be dropped. Then, using Equations (4.26) and (4.27) to substitute for i_B and v_{BE} in Equation (4.28), we obtain

$$I_{BQ} + i_b(t) = (1 - \alpha) I_{ES} \exp\left(\frac{V_{BEQ} + v_{be}(t)}{V_T}\right) \quad (4.29)$$

which can be written as

$$I_{BQ} + i_b(t) = (1 - \alpha) I_{ES} \exp\left(\frac{V_{BEQ}}{V_T}\right) \exp\left(\frac{v_{be}(t)}{V_T}\right) \quad (4.30)$$

Equation (4.28) also relates the Q -point values, so we can write

$$I_{BQ} = (1 - \alpha) I_{ES} \exp\left(\frac{V_{BEQ}}{V_T}\right) \quad (4.31)$$

Substituting this into Equation 4.30, we have

$$I_{BQ} + i_b(t) = I_{BQ} \exp\left(\frac{v_{be}(t)}{V_T}\right) \quad (4.32)$$

We are interested in small signals for which the magnitude of $v_{be}(t)$ is much smaller in magnitude than V_T at all times. [Thus, $v_{be}(t)$ is confined to be a few millivolts or less in magnitude.]

For $|x| \ll 1$, the following approximation holds:

$$\exp(x) \cong 1 + x \quad (4.33)$$

Hence, Equation (4.32) can be expressed as

$$I_{BQ} + i_b(t) \cong I_{BQ} \left(1 + \frac{v_{be}(t)}{V_T} \right) \quad (4.34)$$

If we subtract I_{BQ} from both sides and define $r_\pi = V_T/I_{BQ}$, we have

$$i_b(t) = \frac{v_{be}(t)}{r_\pi} \quad (4.35)$$

Thus, for small-signal variations around the Q -point, the base-emitter junction of the transistor appears to be a resistance given by

$$r_{\pi} = \frac{V_T}{I_{BQ}} \quad (4.36)$$

Substituting $I_{BQ} = I_{CQ}/\beta$, we have an alternative formula:

$$r_{\pi} = \frac{\beta V_T}{I_{CQ}} \quad (4.37)$$

At room temperature, $V_T \cong 0.026$ V. A typical value of β is 100, and a typical bias current for a small-signal amplifier is $I_{CQ} = 1$ mA. These values yield $r_{\pi} = 2600 \Omega$. The collector current is β times the base current:

$$i_c(t) = \beta i_b(t) \quad (4.38)$$

But each current is the sum of the Q -point value and the signal component, so we have

$$I_{CQ} + i_c(t) = \beta I_{BQ} + \beta i_b(t) \quad (4.39)$$

Consequently, the signal components are related by

$$i_c(t) = \beta i_b(t) \quad (4.40)$$

Small-Signal Equivalent Circuits for the BJT

Equations (4.35) and (4.40) relate the small-signal currents and voltages in a BJT. It is convenient to represent the BJT by the **small-signal equivalent circuit** illustrated in Figure 4.33a. Notice that the equivalent circuit embodies the relationships developed earlier: $i_b(t) = v_{be}(t)/r_{\pi}$ and $i_c(t) = \beta i_b(t)$.

If we use the first relationship to substitute for $i_b(t)$ in the second, we obtain

$$i_c(t) = \frac{\beta}{r_{\pi}} v_{be}(t) \quad (4.41)$$

We define the **transconductance** of the BJT as

$$g_m = \frac{\beta}{r_{\pi}} \quad (4.41)$$

If we use Equation 4.37 to substitute for r_{π} , we obtain

$$g_m = \frac{I_{CQ}}{V_T} \quad (4.42)$$

In terms of r_{π} and g_m , the relationships between the BJT small-signal currents and voltages are

$$v_{be}(t) = r_{\pi} i_b(t) \text{ and } i_c(t) = g_m v_{be}(t)$$

These relationships are represented by the BJT equivalent circuit shown in Figure 4.33a.

The small-signal equivalent circuit for a BJT consists of a resistance r_{π} and a current source βi_b (or $g_m v_{be}$).

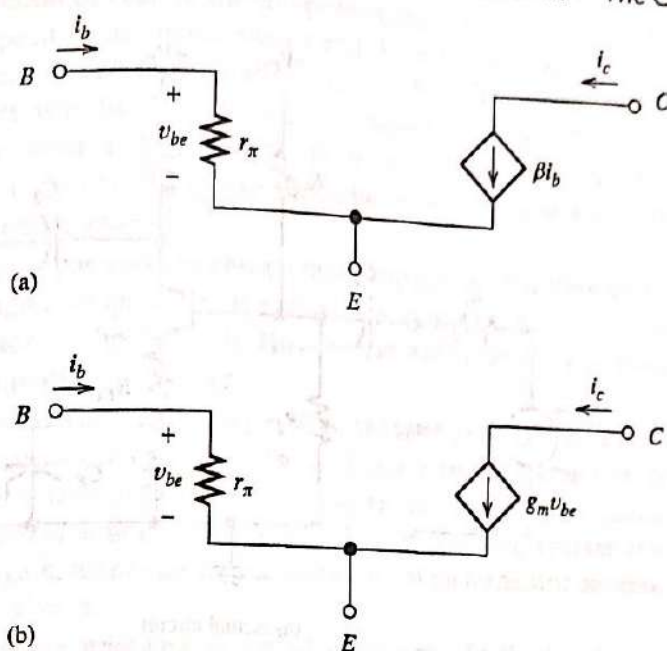


Figure 4.33
Small-signal equivalent circuits for the BJT.

It turns out that the *pnp* transistor has exactly the same small-signal equivalent circuits as the *npn*—even the reference directions for the *signal* currents are the same. The resistance r_π is given by Equation (4.37) and the transconductance g_m is given by Equation (4.42) for both types of transistors. (We assume that I_{CQ} is referenced out of the collector of the *pnp*, so it has a positive value.) In the next several sections, we will find that these small-signal equivalent circuits are very useful in the analysis of BJT amplifier circuits.

Given the Q -point collector current I_{CQ} and β , we can compute the small-signal parameters: $r_\pi = \beta V_T / I_{CQ}$ and $g_m = I_{CQ} / V_T$.

EXERCISE

4.19 At room temperature, a certain transistor has $\beta = 100$. Compute the values of g_m and r_π for $I_{CQ} = 10$ mA. Repeat for $I_{CQ} = 1$ mA.

Answer For $I_{CQ} = 10$ mA, we have $g_m = 385$ mS and $r_\pi = 260 \Omega$. For $I_{CQ} = 1$ mA, we have $g_m = 38.5$ mS and $r_\pi = 2600 \Omega$.

4.7 THE COMMON-EMITTER AMPLIFIER

In this and the next section, we discuss several important single-stage BJT amplifier circuits. Ultimately, we want to understand these circuits so that we can design and use multistage integrated amplifiers. However, interaction between the stages of direct-coupled IC amplifiers complicates their analysis and design. Thus, to simplify our discussion at this point, we examine single-stage BJT amplifiers in the context of discrete circuits.

We will learn how to analyze amplifier circuits to find their gain, input resistance, and output resistance by means of the small-signal equivalent circuit. In this section, we illustrate this procedure for the **common-emitter amplifier** shown in Figure 4.34a.

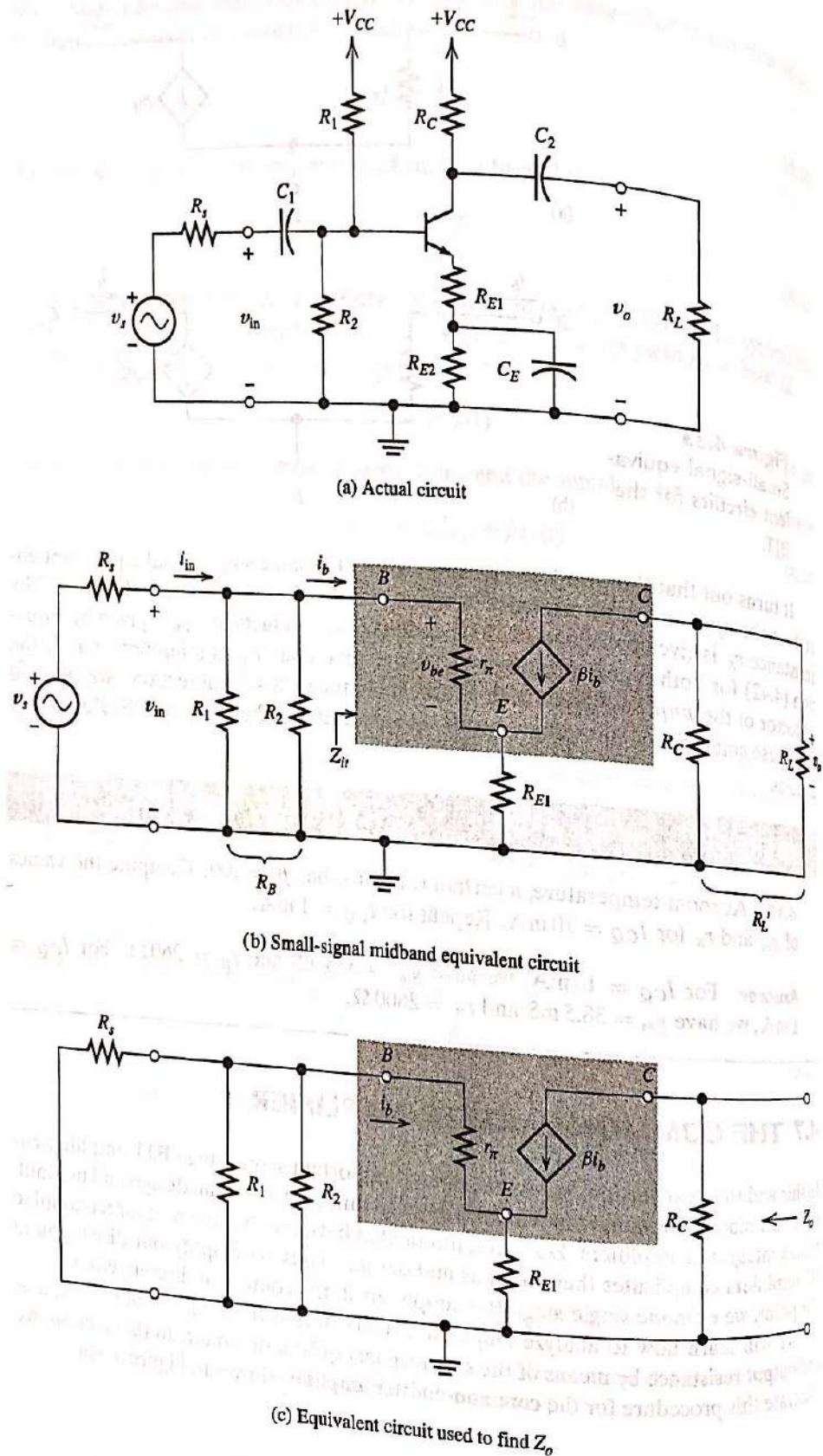


Figure 4.34 Common-emitter amplifier.

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Let us consider the function of each of the components shown in the figure. Notice that for dc currents, the capacitors are open circuits and the resistors R_{E1} and R_{E2} are in series. We denote the series equivalent as $R_E = R_{E1} + R_{E2}$. The resistors R_1 , R_2 , R_E , and R_C form the four-resistor biasing network. The capacitor C_1 couples the signal source to the base of the transistor, and C_2 couples the amplified signal at the collector to the load R_L . The capacitor C_E is called a **bypass capacitor**; it provides a low-impedance path for the ac emitter current to ground.

The coupling and bypass capacitors are chosen large enough so that they have very low ac impedances at the signal frequencies. For simplicity in our initial small-signal ac analysis, we treat the capacitors as short circuits. However, at sufficiently low frequencies, the capacitors reduce the gain of the amplifier.

Sometimes we will use this circuit with $R_{E1} = 0$ so that the emitter is directly connected to ground for ac signals. Because the bypass capacitor grounds the emitter for ac signals, the emitter terminal is common to the input source and to the load. This is the origin of the name *common-emitter* amplifier. We will see that choosing a nonzero value for R_{E1} reduces the voltage gain, makes the gain less dependent on transistor parameters, and increases the input impedance.

Our analysis is valid for the **midband region** of frequency. In the **low-frequency region**, the effects of the coupling and bypass capacitors must be considered. In the **high-frequency region**, a more complex transistor model must be used that includes the frequency limitations of the transistor. We treat the high-frequency response of this circuit in Chapter 8.

The Small-Signal Equivalent Circuit

Before we analyze the amplifier, it is very helpful to draw its small-signal ac equivalent circuit. This is illustrated in Figure 4.34b. The coupling capacitors have been replaced by short circuits, and the transistor has been replaced by its small-signal equivalent, which was discussed in the preceding section.

The dc power supply is replaced by a short circuit. This is appropriate because no ac voltage can appear across an ideal dc voltage source that is assumed to have zero internal impedance.

Carefully compare the actual circuit of Figure 4.34a with the small-signal ac equivalent shown in Figure 4.34b. Observe that the signal source is connected directly to the base terminal because C_1 has been treated as a short circuit. Similarly, the lower end of R_{E1} is connected directly to ground, and the load is connected to the collector.

Notice that the top end of R_1 connects to the supply in the original circuit, but R_1 is connected from base to ground in the equivalent circuit, because the power-supply voltage is treated as a short circuit to ground for ac signals. Notice also that R_1 ends up in parallel with R_2 . Similarly, R_C and R_L are in parallel. It is convenient to define R_B as the parallel combination of R_1 and R_2 .

$$R_B = R_1 || R_2 = \frac{1}{1/R_1 + 1/R_2} \quad (4.43)$$

The dc power supply is replaced by a short circuit.

In a midband analysis, the coupling and bypass capacitors are treated as short circuits.

BJT amplifier circuits can be analyzed by drawing the small-signal equivalent circuit and applying circuit laws. Important amplifier characteristics are voltage gain, current gain, input impedance, and output impedance.

Similarly, R'_L is the parallel combination of R_C and R_L :

$$R'_L = R_L || R_C = \frac{1}{1/R_L + 1/R_C} \quad (4.44)$$

These parallel combinations are indicated in Figure 4.34b.

Voltage Gain

Now we analyze the equivalent circuit to find an expression for the voltage gain of the amplifier. Notice that the current through R_{E1} is equal to $i_e = (\beta + 1)i_b$. The input voltage is

$$v_{in} = v_{be} = r_\pi i_b + R_{E1}(\beta + 1)i_b \quad (4.45)$$

The output voltage is produced by the collector current flowing through R'_L :

$$v_o = -R'_L \beta i_b \quad (4.46)$$

The minus sign is necessary because of the reference directions for the current and voltage—the current flows out of the positive voltage reference. Dividing the respective sides of Equation (4.46) by those of Equation (4.45) gives the voltage gain:

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R'_L}{r_\pi + (\beta + 1)R_{E1}} \quad (4.47)$$

Notice that the gain is negative, showing that the common-emitter amplifier is inverting. The voltage gain magnitude can be quite large—several hundred is not unusual.

Sometimes we want to design circuits for which the gain is almost independent of the transistor parameters. If we select R_{E1} large enough so that $(\beta + 1)R_{E1} \gg r_\pi$, Equation (4.47) becomes

$$A_v \cong -\frac{\beta R'_L}{(\beta + 1)R_{E1}}$$

Since we usually have $\beta \gg 1$, the gain expression reduces to

$$A_v \cong -\frac{R'_L}{R_{E1}}$$

Thus, if we have $(\beta + 1)R_{E1} \gg r_\pi$ and $\beta \gg 1$, the voltage gain is nearly independent of the transistor parameters.

The expression for gain given in Equation (4.47) is with the load connected. In Chapter 1, we found the open-circuit voltage gain useful for characterizing amplifiers. With R_L replaced by an open circuit, the voltage gain becomes

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi + (\beta + 1)R_{E1}} \quad (4.48)$$

The voltage gain of the CE amplifier is nearly independent of β if $(\beta + 1)R_{E1}$ is much greater than r_π .

Input Impedance

Another important amplifier specification is the input impedance, which is the impedance seen looking into the input terminals. First, from Equation 4.45, we can find the input impedance seen looking into the base terminal of the transistor. We have

$$Z_{it} = \frac{v_{in}}{i_b} = r_{\pi} + (\beta + 1)R_{E1} \quad (4.49)$$

Then the input impedance seen by the source is the parallel combination of R_B and Z_{it} :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_B + 1/Z_{it}} \quad (4.50)$$

(In this case, the input impedance is a pure resistance. Therefore, we can find the input impedance by dividing the *instantaneous* voltage v_{in} by the *instantaneous* current i_{in} . Of course, if there were capacitances or inductances in the equivalent circuit, it would be necessary to obtain the impedance as the ratio of the phasor voltage to the phasor current.)

Current Gain and Power Gain

The current gain A_i can be found by the use of Equation (2.3). With appropriate changes in notation, the equation is

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} \quad (4.51)$$

The power gain G of the amplifier is the product of the current gain and the voltage gain (assuming that the input and load impedances are purely resistive):

$$G = A_i A_v \quad (4.52)$$

Output Impedance

The output impedance is the impedance seen looking back from the load terminals with the source voltage v_s set to zero. This situation is illustrated in Figure 4.34c. With v_s set to zero, there is no driving source for the base circuit, so i_b is zero. Therefore, the controlled source βi_b produces zero current and appears as an open circuit. Thus, the impedance seen from the output terminals is simply R_C :

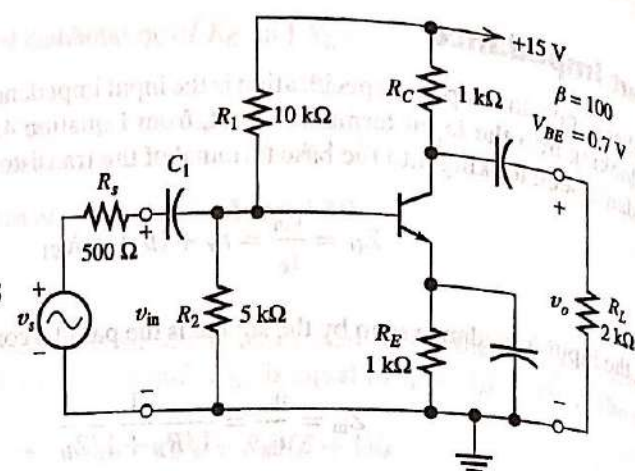
$$Z_o = R_C \quad (4.53)$$

The output impedance is the impedance seen looking back from the load terminals with the source voltage v_s set to zero.

Example 4.9 Calculation of Common-Emitter Amplifier Performance

- (a) Find A_v , A_{vo} , Z_{in} , A_i , G , and Z_o for the amplifier shown in Figure 4.35.

Figure 4.35
Common-emitter amplifier of Example 4.9.



- (b) Then, if $v_i(t) = 0.001 \sin(\omega t)$ V, find an expression for $v_o(t)$.
 (c) Finally, repeat part (a) if the emitter resistor R_E is split into $R_{E1} = 100 \Omega$ and $R_{E2} = 900 \Omega$, with the bypass capacitor in parallel with R_{E2} .

SOLUTION First, we need to find I_{CQ} , so that we can compute the value of r_π . Thus, we start by analyzing the dc conditions in the circuit. Only the dc supply, the transistor, and the resistors R_1 , R_2 , R_C , and R_E need to be considered in the bias-point analysis. The capacitors, the signal source, and the load resistance have no effect on the Q -point.

The dc circuit was shown earlier in Figure 4.29 and was analyzed in Example 4.7. For $\beta = 100$, the resulting Q -point was found to be $I_{CQ} = 4.12$ mA and $V_{CE} = 6.72$ V. Thus, we have

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 631 \Omega$$

Using Equations (4.43) and (4.44), we find that

$$R_B = \frac{1}{1/R_1 + 1/R_2} = 3.33 \text{ k}\Omega$$

and

$$R'_L = \frac{1}{1/R_L + 1/R_C} = 667 \Omega$$

- (a) Now we are ready to determine the gains and impedances. Equations (4.47) through (4.53) yield

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R'_L}{r_\pi} = -106$$

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi} = -158$$

$$Z_{it} = r_{\pi}$$

$$Z_{in} = \frac{1}{1/R_B + 1/Z_{it}} = 531 \Omega$$

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} = -28.1$$

$$G = A_i A_v = 2980$$

$$Z_o = R_C = 1 \text{ k}\Omega$$

and

Notice that A_v is somewhat smaller in magnitude than A_{vo} . This is due to loading of the amplifier by R_L , as discussed in Chapter 1. The power gain is quite large for the common-emitter amplifier, and primarily for this reason, it is a commonly used configuration.

- (b) The source voltage divides between the internal source resistance and the input impedance of the amplifier. Thus, we can write

$$v_{in} = v_s \frac{Z_{in}}{Z_{in} + R_s} = 0.515 v_s$$

Now, with the load connected, we have

$$v_o = A_v v_{in} = -54.6 v_s$$

But we are given that $v_s(t) = \sin(\omega t) \text{ mV}$, so we obtain

$$v_o(t) = -54.6 \sin(\omega t) \text{ mV}$$

Notice that the phase of $v_o(t)$ is inverted compared with that of $v_s(t)$.

- (c) When R_E is split into two parts, the bias point and r_{π} remain the same as before, and we have

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R'_L}{r_{\pi} + (\beta + 1)R_{E1}} = -6.21$$

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_{\pi} + (\beta + 1)R_{E1}} = -9.31$$

$$Z_{it} = r_{\pi} + (\beta + 1)R_{E1} = 10.7 \text{ k}\Omega$$

$$Z_{in} = \frac{1}{1/R_B + 1/Z_{it}} = 2.54 \text{ k}\Omega$$

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} = -7.89$$

$$G = A_i A_v = 49.0$$

$$Z_o = R_C = 1 \text{ k}\Omega$$

and

Notice that having part of the emitter bias resistance unbypassed reduces the gain and increases the input impedance dramatically.

The common-emitter amplifier is inverting. Its voltage and current gains are both potentially larger than unity (100 is typical). Input and output impedance magnitudes are moderate compared with those of other BJT and FET amplifier configurations.

□

EXERCISE

4.20 Repeat parts (a) and (b) of Example 4.9 if $\beta = 300$. [Hint: Do not forget that the Q -point changes (slightly) when β changes.]

Answer $A_v = -109$, $A_{vo} = -164$, $Z_{in} = 1185 \Omega$, $A_i = -64.5$, $G = 7030$, $Z_o = 1 \text{ k}\Omega$, $v_o(t) = -76.7 \sin(\omega t) \text{ mV}$.

4.8 THE EMITTER FOLLOWER

The circuit diagram of another important BJT amplifier called an **emitter follower** is shown in Figure 4.36a. The resistors R_1 , R_2 , and R_E form the biasing circuit. The collector resistor R_C (used in the common-emitter amplifier) is not needed in this circuit. Thus, we have a version of the four-resistor biasing circuit with $R_C = 0$. The analysis of this bias circuit is very similar to the examples we considered in Section 4.5.

The input signal is applied to the base through the coupling capacitor C_1 . The output signal is coupled from the emitter to the load by the coupling capacitor C_2 .

Small-Signal Equivalent Circuit

The ac small-signal equivalent circuit is shown in Figure 4.36b. As before, we replace the capacitors and power supply with short circuits. The transistor is replaced by its small-signal equivalent.

Notice that the collector terminal is connected directly to ground in the equivalent circuit. The transistor equivalent circuit is oriented with the collector at the bottom in Figure 4.36b, but it is electrically the same as the transistor equivalent circuit we have used before. Because the collector is connected to ground, this circuit is sometimes called a **common-collector amplifier**.

The ability to draw the small-signal equivalents of BJT circuits is important in the analysis and design of electronic circuits. Carefully compare the small-signal equivalent in Figure 4.36b with the original circuit. Better still, draw the small-signal equivalent circuit on your own, starting from the original circuit.

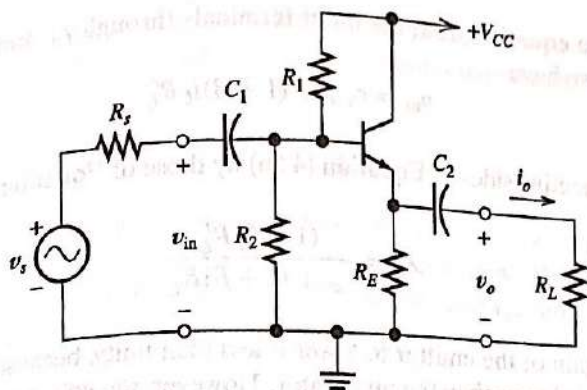
Notice that R_1 and R_2 are in parallel in the equivalent circuit. We denote the combination by R_B . Also, R_E and R_L are in parallel, and we denote the combination by R'_L . Mathematically, we have

$$R_B = R_1 || R_2 = \frac{1}{1/R_1 + 1/R_2} \quad (4.54)$$

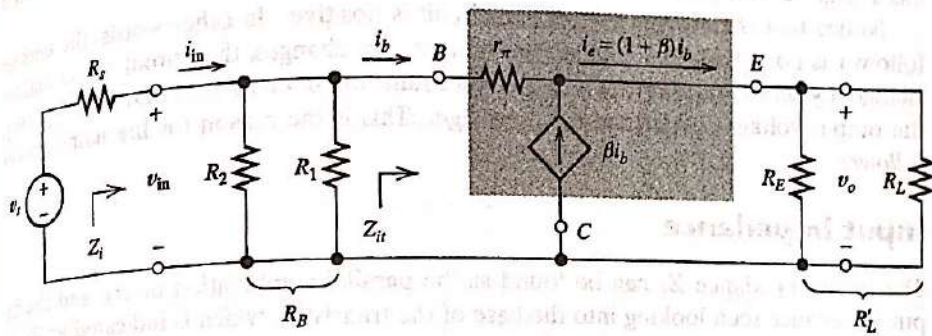
and

$$R'_L = R_E || R_L = \frac{1}{1/R_E + 1/R_L} \quad (4.55)$$

The ability to draw the small-signal equivalents for BJT circuits is important in the analysis and design of electronic circuits.



(a) Actual circuit



(b) Small-signal midband equivalent circuit

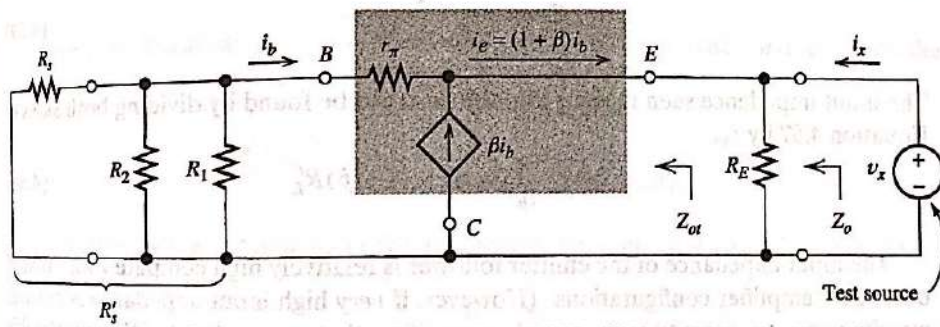

 (c) Equivalent circuit used to find output impedance Z_o

Figure 4.36 Emitter follower.

Voltage Gain

Next, we find the voltage gain of the emitter follower. The current flowing through R_L is $i_e = i_b + \beta i_b$. Thus, the output voltage is given by

$$v_o = (1 + \beta) R_L' i_b \quad (4.56)$$

Writing a voltage equation from the input terminals through r_π and then through the load to ground, we have

$$v_{in} = r_\pi i_b + (1 + \beta) i_b R'_L \quad (4.57)$$

Dividing the respective sides of Equation (4.56) by those of Equation (4.57) results in

$$A_v = \frac{(1 + \beta) R'_L}{r_\pi + (1 + \beta) R'_L} \quad (4.58)$$

The voltage gain of the emitter follower is typically slightly less than unity.

The voltage gain of the emitter follower is less than unity, because the denominator of the expression is larger than the numerator. However, the voltage gain is usually only slightly less than unity. An amplifier with voltage gain less than unity can be useful if it has a large current gain.

Notice that the voltage gain of this circuit is positive. In other words, the emitter follower is noninverting. Thus, if the input voltage changes, the output at the emitter changes by almost the same amount and in the same direction as the input. Consequently, the output voltage follows the input voltage. This is the reason for the name *emitter follower*.

Input Impedance

The input impedance Z_i can be found as the parallel combination of R_B and the input impedance seen looking into the base of the transistor, which is indicated as Z_{it} in Figure 4.36b. Thus, we can write

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} \quad (4.59)$$

The input impedance seen looking into the base can be found by dividing both sides of Equation 4.57 by i_b :

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + (1 + \beta) R'_L \quad (4.60)$$

The input impedance of the emitter follower is relatively high compared with that of other BJT amplifier configurations.

The input impedance of the emitter follower is relatively high compared with that of other BJT amplifier configurations. (However, if very high input impedance is needed, we often have to resort to more complex amplifiers that use feedback. We consider this approach later. In the next chapter, we will see that field-effect transistors are capable of providing much higher input impedance than BJTs.) Once we have found the voltage gain and input impedance of the emitter follower, the current gain and power gain can be found by the use of Equations (1.4) and (1.6).

Output Impedance

The output impedance of an amplifier is the Thévenin impedance seen from the output terminals. To find the output impedance of the emitter follower, we remove the load resistance, zero the signal source, and look back into the output terminals of the equivalent

circuit. This is shown in Figure 4.36c. We have attached a test source v_x that delivers a current i_x to the impedance we want to find. The output impedance is

$$Z_o = \frac{v_x}{i_x} \quad (4.61)$$

Here again, the impedance can be found as the ratio of instantaneous time-varying quantities, because the circuit is purely resistive. Otherwise, we should use phasors.) To find this ratio, we write equations involving v_x and i_x . For example, summing currents at the top end of R_E , we have

$$i_b + \beta i_b + i_x = \frac{v_x}{R_E} \quad (4.62)$$

We must eliminate i_b from this equation before we can find the desired expression for the output impedance. We do not want any circuit variables, such as i_b , in the result—only transistor parameters and resistor values. Thus, we need to write another circuit equation. First, we denote the parallel combination of R_s , R_1 , and R_2 as

$$R'_s = \frac{1}{1/R_s + 1/R_1 + 1/R_2} \quad (4.63)$$

The additional equation that is needed can now be obtained by applying Kirchhoff's voltage law to the loop consisting of v_x , r_π , and R'_s :

$$v_x + r_\pi i_b + R'_s i_b = 0 \quad (4.64)$$

If we solve Equation (4.64) for i_b , substitute into Equation (4.62), and rearrange the result, we obtain the output impedance:

$$Z_o = \frac{v_x}{i_x} = \frac{1}{(1 + \beta)/(R'_s + r_\pi) + (1/R_E)} \quad (4.65)$$

This equation can be recognized as the parallel combination of R_E and the impedance

$$Z_{ot} = \frac{R'_s + r_\pi}{(1 + \beta)} \quad (4.66)$$

(Z_{ot} is the impedance seen looking into the emitter of the transistor, as indicated in Figure 4.36c.) The output impedance of the emitter follower tends to be smaller than that of other BJT amplifier configurations.

The output impedance of the emitter follower tends to be smaller than that of other BJT amplifier configurations.

Example 4.10 Calculation of Emitter-Follower Performance

Compute the voltage gain, input impedance, current gain, power gain, and output impedance of the emitter-follower amplifier displayed in Figure 4.37a.

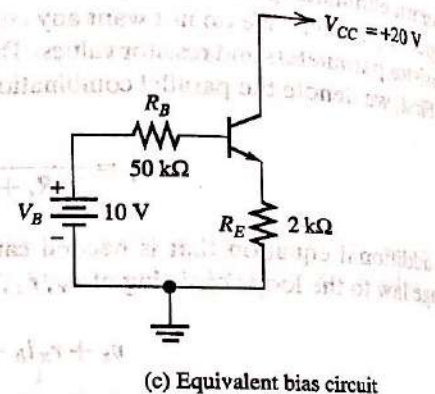
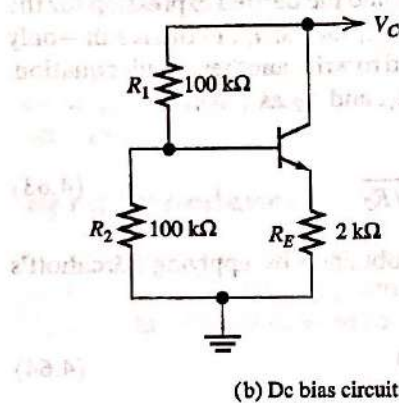
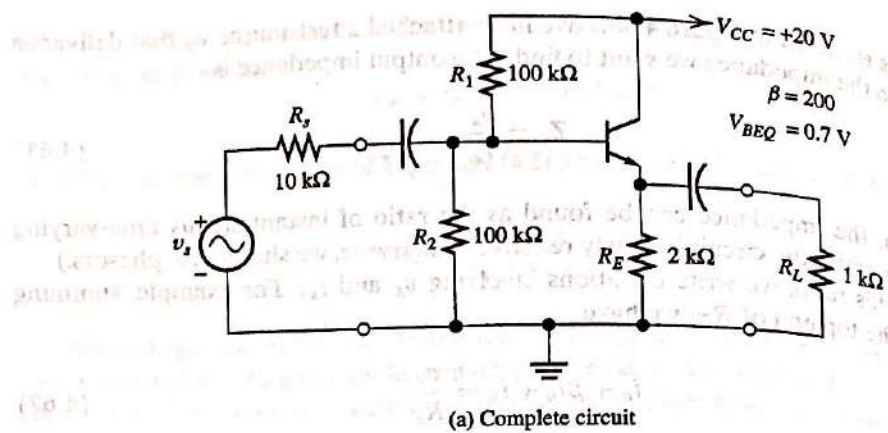


Figure 4.37 Emitter follower of Example 4.10.

First, we must find the bias point, so that the value of r_π can be calculated.

SOLUTION First, we must find the bias point, so that the value of r_π can be calculated. The dc circuit is shown in Figure 4.37b. Because the coupling capacitors act as open circuits for dc, R_s and R_L do not appear in the dc bias circuit.

Replacing the base bias circuit by its Thévenin equivalent, we obtain the equivalent circuit shown in Figure 4.37c. Now, if we assume that the circuit is operating in the active region, we can write the following voltage equation around the base loop:

$$V_B = R_B I_{BQ} + V_{BEQ} + R_E (1 + \beta) I_{BQ}$$

Substituting values, we find that $I_{BQ} = 20.6 \mu\text{A}$. Hence, we obtain

$$I_{CQ} = \beta I_{BQ} = 4.12 \text{ mA}$$

and

$$V_{CEQ} = V_{CC} - I_{EQ} R_E = 11.7 \text{ V}$$

Because V_{CEQ} is greater than 0.2 V and I_{BQ} is positive, the transistor is operating in the active region, and we have

$$r_{\pi} = \frac{\beta V_T}{I_{CQ}} = 1260 \Omega$$

Now that we have established that the transistor operates in the active region and have found the value of r_{π} , we can proceed to determine the amplifier gains and impedances. Substituting values into Equations (4.54) and (4.55), we find that

$$R_B = \frac{1}{1/R_1 + 1/R_2} = 50 \text{ k}\Omega$$

and

$$R'_L = \frac{1}{1/R_L + 1/R_E} = 667 \Omega$$

Equation (4.58) gives the voltage gain:

$$A_v = \frac{(1 + \beta)R'_L}{r_{\pi} + (1 + \beta)R'_L} = 0.991$$

Equations (4.59) and (4.60) give the input impedance:

$$Z_{it} = \frac{v_{in}}{i_b} = r_{\pi} + (1 + \beta)R'_L = 135 \text{ k}\Omega$$

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} = 36.5 \text{ k}\Omega$$

Equations (4.63) and (4.65) yield

$$R'_s = \frac{1}{1/R_s + 1/R_1 + 1/R_2} = 8.33 \text{ k}\Omega$$

and

$$Z_o = \frac{v_x}{i_x} = \frac{1}{(1 + \beta)/(R'_s + r_{\pi}) + (1/R_E)} = 46.6 \Omega$$

The current gain is

$$A_i = A_v \frac{Z_i}{R_L} = 36.2$$

The power gain is

$$G = A_v A_i = 35.8$$

Notice that even though the voltage gain is less than unity, the current gain is large (compared with unity). Thus, the output power is larger than the input power, and the circuit is effective as an amplifier. $\square$

We use an emitter follower if high input impedance or low output impedance is needed.

In general, the output impedance of the emitter follower is much lower and the input impedance higher than the corresponding impedances in other single-stage BJT amplifiers. Consequently, we use an emitter follower if high input impedance or low output impedance is needed.

If the emitter follower is cascaded with common-emitter stages, amplifiers with many useful combinations of parameters are possible. Furthermore, there are several other useful amplifier configurations that employ the BJT. In Chapter 7, we study additional circuit configurations and consider the design of multistage amplifiers.

EXERCISE

4.21 Repeat Example 4.10 for $\beta = 300$. Compare the results with those of the example.

Answer $A_v = 0.991$, $Z_i = 40.1 \text{ k}\Omega$, $Z_o = 33.2 \Omega$, $A_i = 39.7$, $G = 39.4$.

Before we leave the important topic of small-signal equivalent-circuit analysis, we review the technique and provide a few observations that you may find helpful.

Drawing the Small-Signal Equivalent Circuit

Our first step is to draw the small-signal equivalent circuit by making the following changes to the original circuit:

1. Replace the dc power-supply voltage sources by short circuits.
2. Replace any dc current sources we encounter with open circuits. (This is appropriate because dc current sources force a constant current—with no ac signal component—to flow.)
3. Replace the coupling and bypass capacitors with short circuits, when a midband analysis is desired. However, if we want to find expressions for gains or impedances as a function of frequency, or if we wish to perform a transient analysis, the capacitors should be included in the equivalent circuit (and we should use phasors to represent currents and voltages in the ac analysis).
4. Replace inductors that have very high ac signal impedances with open circuits in the small-signal equivalent circuit. (Sometimes, in providing a dc connection, we choose inductors so that their inductance is large enough to produce very high impedance for the ac signal. Usually, this technique is practical only in circuits intended to operate at high frequencies.)
5. Replace the transistor with its equivalent circuit. If the circuit has several transistors, use subscripts to distinguish the currents and parameters of different transistors.

Double-check your equivalent circuit before writing equations.

You may find it advantageous to take several steps in drawing small-signal equivalent circuits. First, make the necessary changes, and then, if desired, redraw the circuit to simplify the layout. It pays to be careful in drawing the equivalent circuit: analyzing an incorrect equivalent circuit is time and effort wasted. Double-check your equivalent circuit before writing equations.

Identifying the Circuit Variables of Interest

Once the small-signal equivalent circuit is finished, we turn our attention to finding expressions for the gains and impedances that are of interest. First, identify the pertinent currents and voltages, and label them on the equivalent circuit. For example, in finding the voltage gain, the pertinent variables are the input voltage v_{in} and the output voltage v_o . On the other hand, for the input impedance, we are concerned with v_{in} and the input current i_{in} .

Finding the Output Resistance

The output resistance is the Thévenin resistance of the amplifier. To find the output resistance, we remove the load, set the values of independent signal sources to zero, and look back into the output terminals to find the resistance. Setting the independent signal sources to zero amounts to replacing voltage sources with short circuits and current sources with open circuits. Dependent sources, such as the controlled current source of the transistor equivalent, are not set to zero—the controlled source models the effect of the transistor.

Often, it is convenient to attach a test voltage source v_x to the output terminals, as we did in Figure 4.36c, to find the output resistance of the emitter follower. The output resistance is the ratio of v_x to i_x .

Writing the Circuit Equations

After drawing the small-signal equivalent circuit and identifying the pertinent current or voltage variables, we use circuit analysis to write the equations. Often, it is necessary to include additional currents or voltages in the equations. For example, in finding the output resistance of the emitter follower, we wanted to find the ratio of v_x to i_x , but in writing the Equations (4.62) and (4.64), we included an additional current i_b .

After writing a suitable set of circuit equations, we use substitution to eliminate the unwanted currents and voltages, until we have an equation relating the two variables of interest. For example, we solved Equation (4.64) for i_b and then substituted the result into Equation (4.62) to obtain a single equation relating v_x and i_x , from which we found the output resistance.

If the circuit is fairly complex, it is a good idea to make sure that a proper set of circuit equations has been written before any algebra is used to eliminate the unwanted variables. Suppose that we count the unwanted variables and denote the number as N . Because one equation is needed to eliminate each unwanted variable, and because we need to end up with an equation relating the two variables of interest, we need a total of $N + 1$ independent equations. Make sure that the equations are not dependent—sometimes we can write the same equation in different forms without realizing it.

Finding and Checking the Desired Expression

Once a sufficient number of independent equations have been written, straightforward algebraic techniques are used to eliminate the unwanted circuit variables and find the desired expression. If, in this process, substitution results in cancellation of all of the terms, so that we have $0 = 0$, then we have written dependent equations, and we must return to writing additional circuit equations.

Dependent sources, such as the controlled current source of the transistor equivalent, are not set to zero—the controlled source models the effect of the transistor.

Checking Units

After we have found an expression for the gain or impedance, it is a good idea to check to see whether the units of the expression are correct. Voltage or current gain should be unitless. Input or output impedance should have units of ohms. In case the units do not check as expected, we should look for errors in writing the original equations or algebraic errors.

Small-signal equivalent circuit analysis is not as troublesome as it might seem from this discussion. We have tried to mention all of the common problems encountered with the technique so that you will not waste too much time if they come up.

The Common-Base Amplifier

The common-base amplifier is noninverting and potentially has high voltage gain. The current gain is less than unity. The input impedance is low and the output impedance is moderate, compared with the corresponding impedances of other BJT amplifiers.

Figure 4.38 shows another BJT amplifier known as a **common-base amplifier**. The common-base amplifier is noninverting and potentially has high voltage gain. The current gain is less than unity. The input impedance is low and the output impedance is moderate, compared with the corresponding impedances of other BJT amplifiers.

EXERCISE

4.22 Consider the common-base amplifier shown in Figure 4.38. Derive expressions for the voltage gain, input resistance, and output resistance in terms of β , r_π , and the resistor values.

Answer $A_v = \beta R'_L / r_\pi$, where $R'_L = R_L \parallel R_C$; $R_{in} = R_E \parallel [r_\pi / (\beta + 1)]$; $R_o = R_C$.

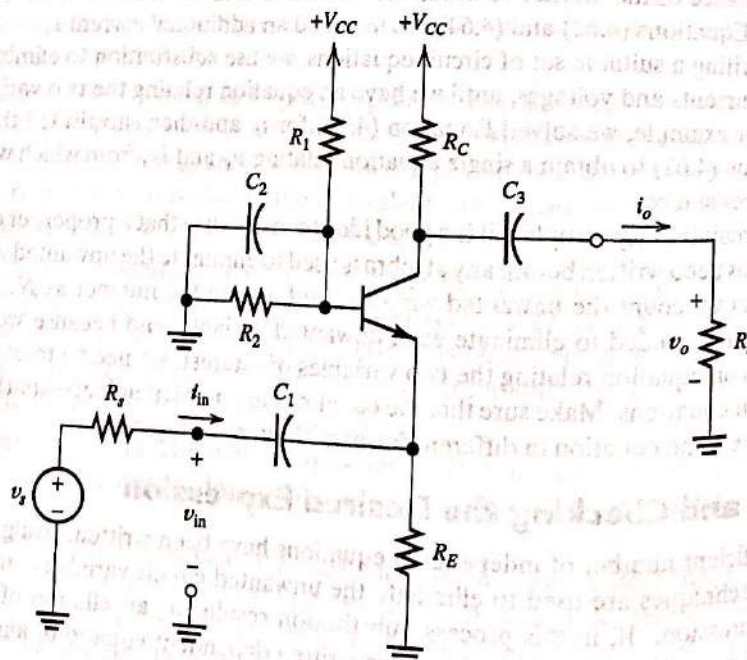


Figure 4.38 Common-base amplifier.

EXERCISE

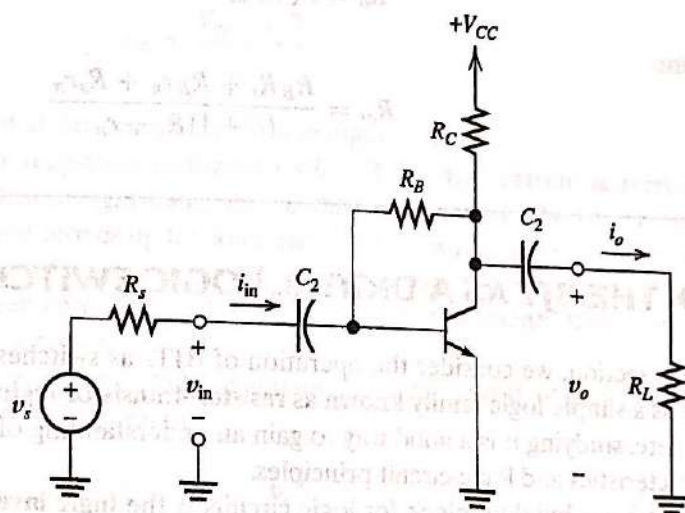
4.23 Evaluate the expressions found in Exercise 4.22 if $R_s = 100\ \Omega$, $R_E = 5\ \text{k}\Omega$, $R_2 = 50\ \text{k}\Omega$, $R_1 = 100\ \text{k}\Omega$, $R_C = 5\ \text{k}\Omega$, $R_L = 1\ \text{k}\Omega$, $V_{CC} = 15\ \text{V}$, $V_{BE} = 0.7\ \text{V}$, and $\beta = 100$. Find the output voltage if $v_s = \sin(\omega t)\ \text{mV}$. Also, evaluate the current gain and power gain. (Hint: First, the Q -point must be found, so that r_π can be evaluated.)

Answer $I_{CQ} = 0.799\ \text{mA}$, $r_\pi = 3254\ \Omega$, $A_v = 25.6$, $R_i = 32.0\ \Omega$, $R_o = 5\ \text{k}\Omega$, $v_o(t) = 6.21 \sin(\omega t)\ \text{mV}$, $A_i = 0.819$, $G = 21.0$.

EXERCISE

4.24 A variation of the common-emitter amplifier is shown in Figure 4.39. Draw the small-signal equivalent circuit and derive an expression for the voltage gain.

Figure 4.39
Variation of
the common-
emitter ampli-
fier.



Answer The small-signal equivalent circuit is illustrated in Figure 4.40. Its voltage gain is

$$A_v = \frac{v_o}{v_{in}} = \frac{R'_L(r_\pi - \beta R_B)}{r_\pi(R'_L + R_B)}$$

EXERCISE

4.25 Derive expressions for the input resistance and output resistance for the circuit of Figure 4.39.

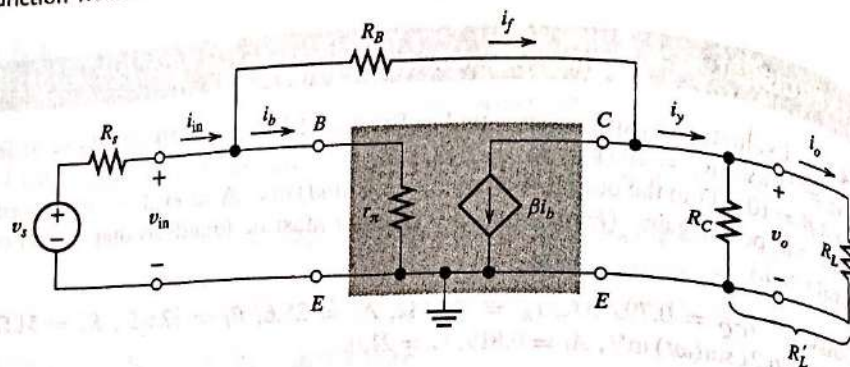


Figure 4.40 Small-signal equivalent circuit for the amplifier of Figure 4.39.

Answer

$$R_{in} = \frac{(R_B + R'_L)r_\pi}{r_\pi + R_B + (\beta + 1)R'_L}$$

$$R_o = R_C || R_{ot}$$

where

$$R_{ot} = \frac{R_B R_s + R_B r_\pi + R_s r_\pi}{(\beta + 1)R_s + r_\pi}$$

4.9 THE BJT AS A DIGITAL LOGIC SWITCH

In this section, we consider the operation of BJTs as switches in logic circuits. We will discuss a simple logic family known as **resistor-transistor logic** (RTL). Although RTL is obsolete, studying it is a good way to gain an understanding of important BJT switching characteristics and logic-circuit principles.

The basic building block for logic circuits is the **logic inverter**. An RTL inverter is displayed in Figure 4.41. If the input voltage V_{in} is zero, the BJT operates in cutoff. Then if the load current i_o is also zero, no current flows through the **pull-up resistor** R_C , and the output voltage V_o is equal to the supply voltage V_{CC} . Thus, if the input is low, the output is high, as is expected for a logic inverter.

If a load that consists of driven gates and that sinks current is connected, a drop occurs across the pull-up resistor, and the output voltage is reduced. However, provided that the loading is not too great, the output voltage will still be recognized as a logic high by the driven gates.

The intended operation of the circuit is for the transistor to be in the saturation region when the input voltage is in the logic high range. Then the output voltage is the saturation voltage of the transistor, which is typically 0.1 to 0.2 V. This voltage is accepted as a logic low by the driven gates. Thus, the circuit functions as a logic inverter, provided that the circuit values are properly selected and the loading is not too great.

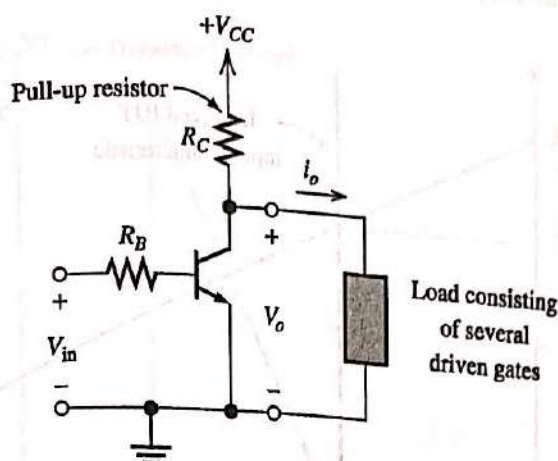


Figure 4.41
RTL inverter.

A load-line analysis of the inverter under no-load conditions ($i_o = 0$) is shown in Figure 4.42. The input characteristic has been idealized. (The idealized input characteristic has zero base current for v_{BE} less than 0.7 V, and it is vertical in the forward-bias region.) The load line for the input circuit is also shown. As long as V_{in} is less than 0.7 V, the base current is zero. If V_{in} is greater than 0.7 V, the base current is given by

$$i_B = \frac{V_{in} - 0.7}{R_B} \quad (4.67)$$

which is the value indicated at the operating point in Figure 4.42a.

The output load line is displayed in Figure 4.42b. If the base current is zero, the operating point is at the lower right-hand end of the load line. As the base current increases, the operating point moves up the load line. For sufficiently large base currents, the operating point is in the saturation region. The intended operation of the RTL logic inverter is to switch between cutoff and saturation. (On the other hand, BJT amplifier circuits operate in the active region.)

Next, we construct the input-output characteristic of the RTL inverter under no-load conditions. The output voltage is given by

$$V_o = V_{CC} - R_C i_C \quad (4.68)$$

In the active region, we have

$$i_C = \beta i_B \quad (4.69)$$

Using Equation (4.67) to substitute for i_B in Equation (4.69), we obtain

$$i_C = \beta \frac{V_{in} - 0.7}{R_B} \quad (4.70)$$

Using Equation (4.70) to substitute for i_C in Equation (4.68) yields

$$V_o = V_{CC} - R_C \beta \frac{V_{in} - 0.7}{R_B} \quad (4.71)$$

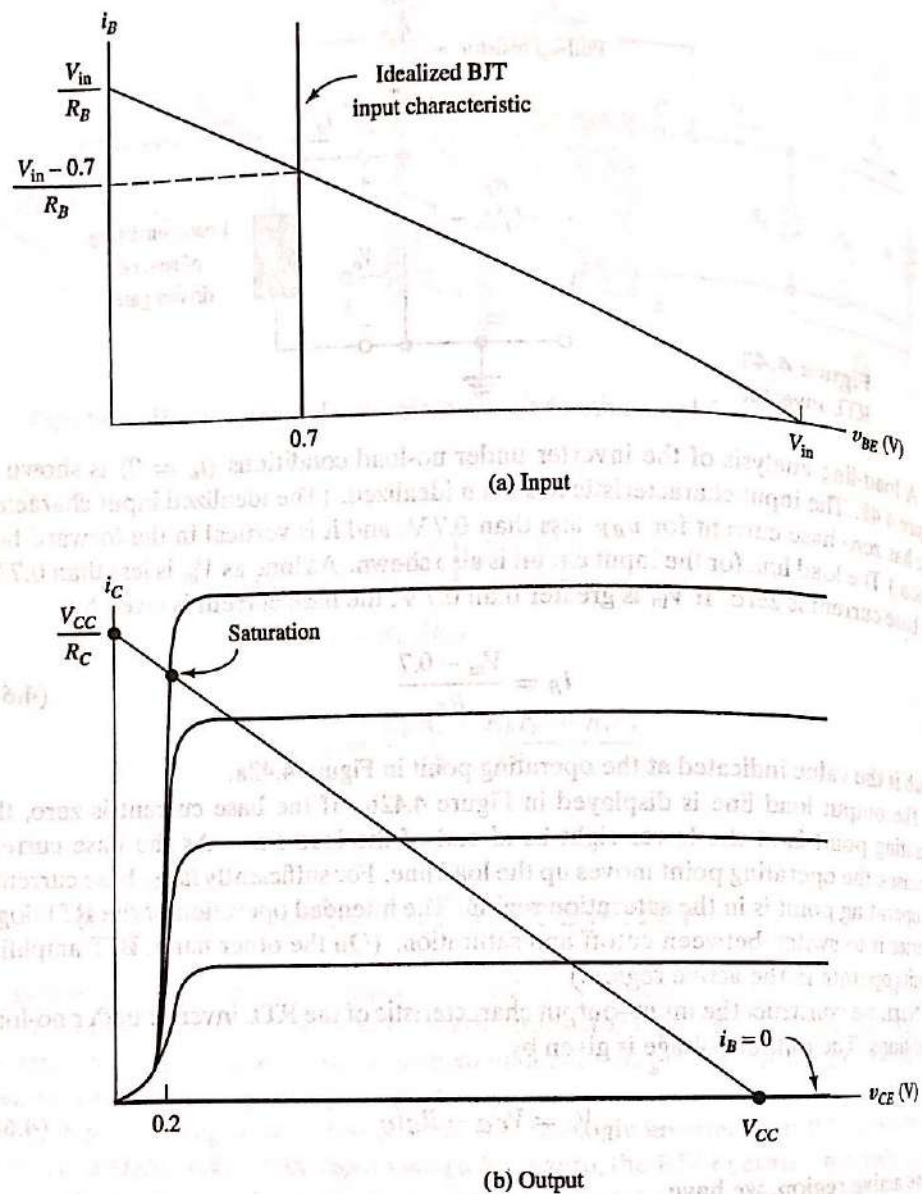


Figure 4.42 Load-line analysis of RTL inverter under no-load conditions.

which is valid in the active region. If Equation (4.71) yields a value less than 0.2 V , the transistor is in saturation, and we have

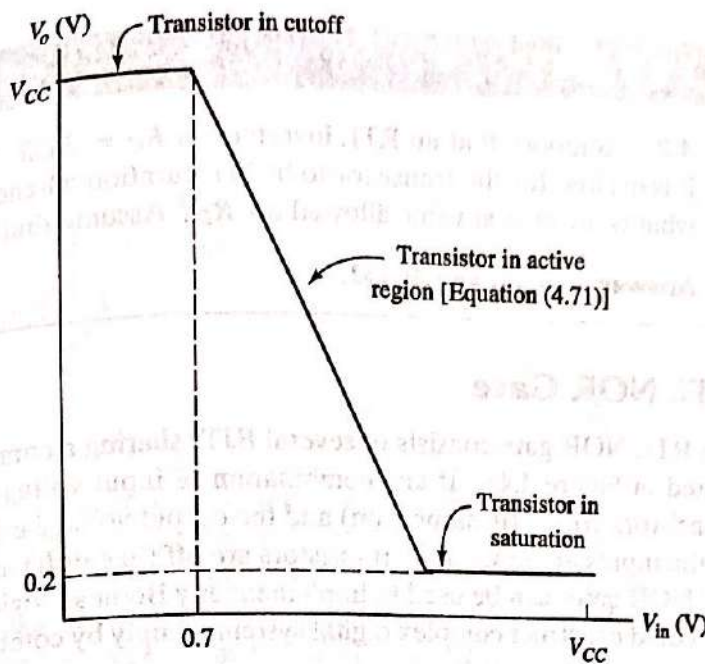
$$V_o = 0.2 \quad (4.72)$$

Finally, if V_{in} is less than 0.7 V , the operation is in cutoff, and we obtain

$$V_o = V_{CC} \quad (4.73)$$

Equations (4.71), (4.72), and (4.73) are plotted in Figure 4.43.

Figure 4.43
Transfer characteristic for RTL inverter under no-load conditions.



EXERCISE

4.26 Plot the input-output characteristic to scale for an RTL inverter with $V_{CC} = 3\text{ V}$, $R_C = 2\text{ k}\Omega$, $R_B = 5\text{ k}\Omega$, and $\beta = 100$. Repeat for $\beta = 10$. Check your answers using a dc sweep in SPICE. Assume that $I_s = 10^{-13}\text{ A}$ for the simulation.

Answer See Figure 4.44.

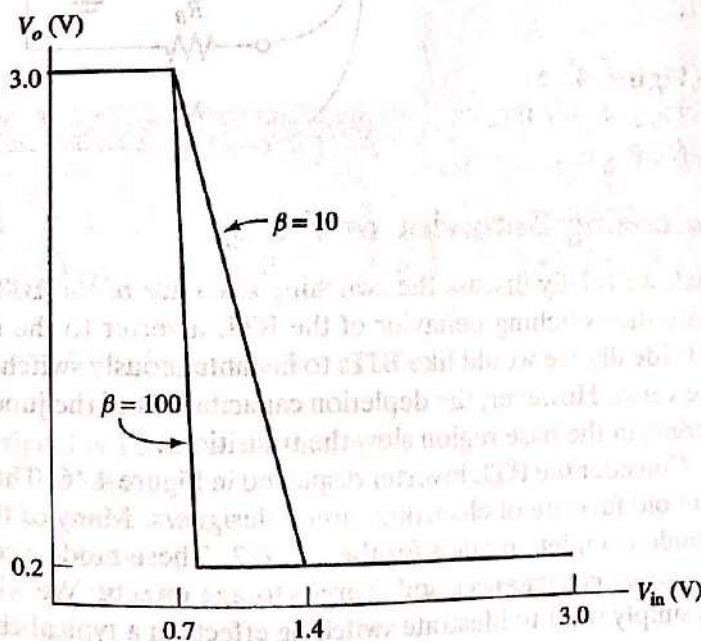


Figure 4.44
Plots for Exercise 4.26.

EXERCISE

4.27 Suppose that an RTL inverter has $R_C = 2\text{ k}\Omega$, $V_{CC} = 10\text{ V}$, and $\beta = 50$. If it is desired for the transistor to be in saturation whenever V_{in} is greater than 1.5 V , what is the largest value allowed for R_B ? Assume that $V_{BE} = 0.7\text{ V}$.

Answer $R_{B\text{ max}} = 8.16\text{ k}\Omega$.

RTL NOR Gate

Logic inverters and NOR gates can be constructed with BJTs and resistors.

An RTL NOR gate consists of several BJTs sharing a common pull-up resistor, as illustrated in Figure 4.45. If any combination of input voltages is high, the corresponding transistors are on (in saturation) and the output voltage is low. On the other hand, if all of the inputs are low, all the transistors are off (in cutoff) and the output is high.

NOR gates can be used to implement any Boolean logic function. Thus, in principle, we could construct complex digital systems simply by combining these basic circuits.

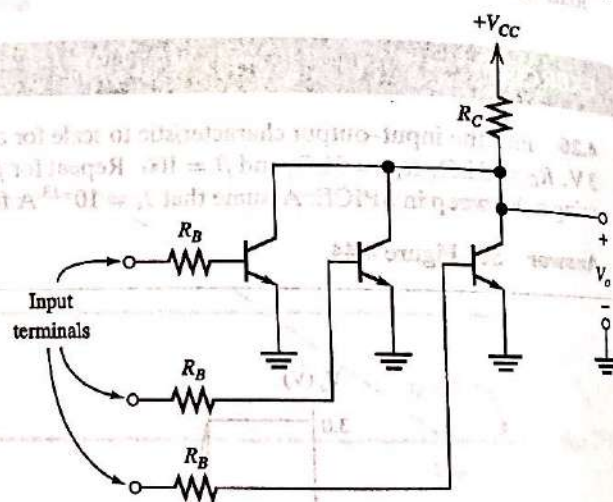


Figure 4.45
Three-input RTL
NOR gate.

Switching Behavior of the BJT

Next, we briefly discuss the switching behavior of the BJT. Our primary objective is to relate the switching behavior of the RTL inverter to the internal device physics of the BJT. Ideally, we would like BJTs to instantaneously switch from saturation to cutoff and vice versa. However, the depletion capacitances of the junctions and storage of minority carriers in the base region slow the transitions.

Consider the RTL inverter displayed in Figure 4.46. The transistor is a 2N2222, which is an old favorite of electronic circuit designers. Many of the student versions of SPICE include complete models for the 2N2222. These models contain parameters to account for device capacitances and charge-storage effects. We will not elaborate at this point; we simply want to illustrate switching effects in a typical circuit.

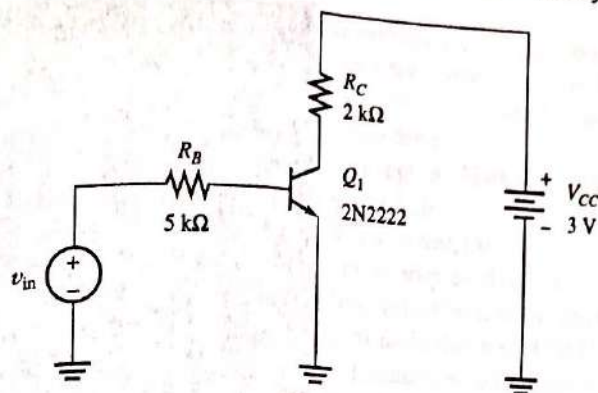


Figure 4.46
RTL inverter.

We have chosen a pulse (the part name is VPULSE) for the input signal v_{in} . We double click on the input source to bring up the window illustrated in Figure 4.47, in which we specify the parameters shown. This results in a 3-V rectangular input pulse. Next, we use the **analysis/setup/transient** command to bring up the window displayed in Figure 4.48, and we set up the parameters for the analysis as shown. Finally, using the **analysis/simulate** command causes the simulation to be executed, after which Probe starts and displays the waveforms illustrated in Figure 4.49a. Using the **trace/add** command, we can also obtain the plots of i_B and v_{BE} displayed in Figure 4.49b.

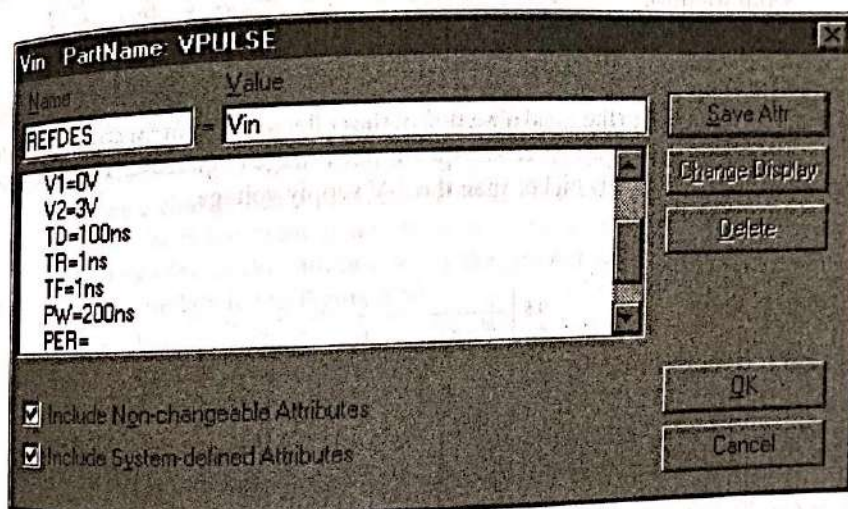


Figure 4.47 Setup window for V_{in} .

As mentioned, the input signal is a 3-V rectangular pulse. Initially, the input voltage is zero, and the transistor is in the cutoff region. Therefore, the base current is zero, the collector current is zero, and the output voltage v_o is 3 V. At $t = 100$ ns, v_{in} rises rapidly to 3 V. The immediate effect is to cause i_B to rapidly increase. This is illustrated in Figure 4.49b. The current flowing into the base charges the junction depletion capacitances, raising the base-to-emitter voltage.

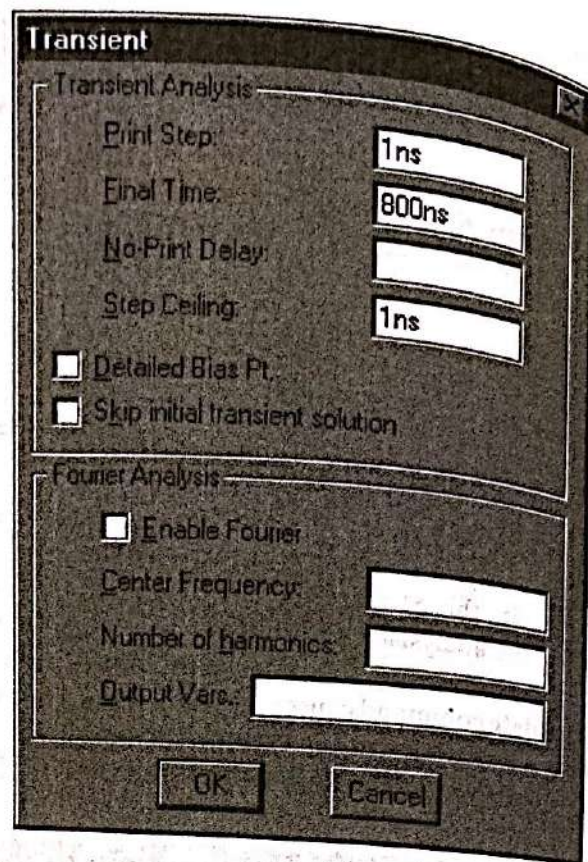


Figure 4.48
Transient-analysis
setup window.

Part of the base current flows through the collector junction capacitance and out the collector lead (opposite to the usual direction of the collector current for an *n*pn transistor in the active region). This current causes the output voltage to increase. Thus, the output voltage actually goes slightly higher than the 3-V supply voltage.

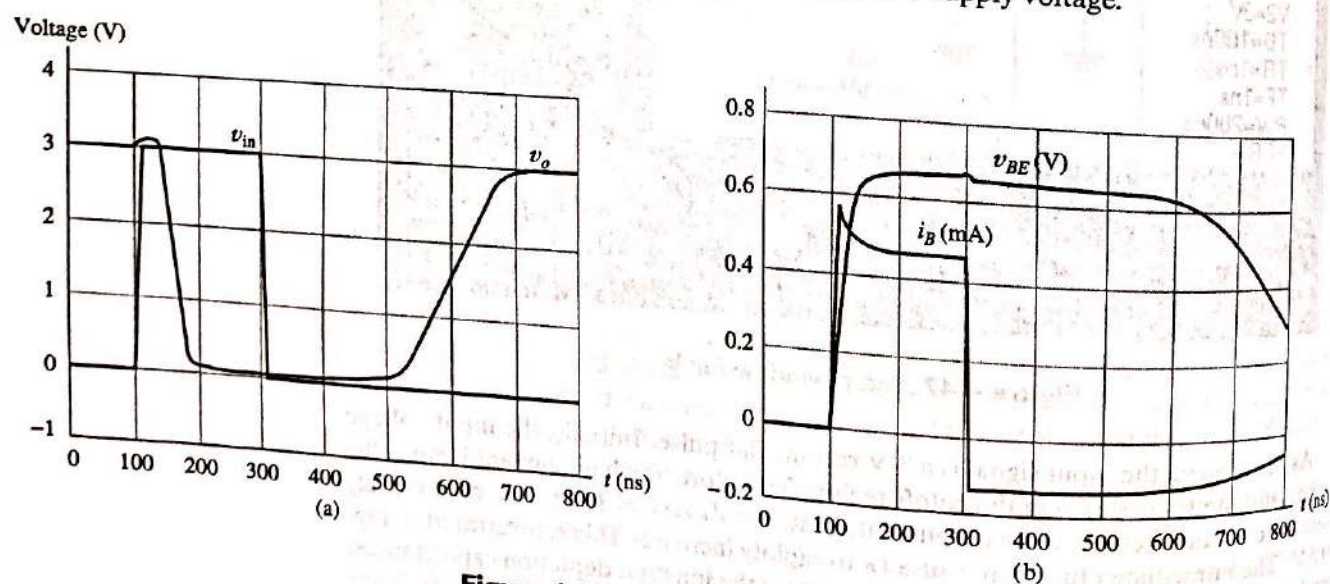


Figure 4.49 RTL inverter waveforms.

Shortly after the beginning of the input pulse, the base voltage rises high enough to forward bias the emitter junction. Then electrons cross from the emitter into the base. These electrons diffuse toward the collector junction. Thus, conventional current begins to flow into the collector, and the collector voltage v_o starts to drop.

At about $t = 190$ ns, the transistor enters the saturation region. Then the collector voltage becomes (approximately) constant, at a few tenths of a volt.

The input voltage v_{in} switches back to zero at $t = 300$ ns. However, the output voltage remains low until approximately $t = 520$ ns, due to excess minority carriers (electrons) stored in the base region. When the transistor is driven into saturation, both junctions are forward biased, so a high concentration of electrons builds up in the base. Until these electrons have been removed from the base, forward current continues to flow across the junctions. Notice that the base current actually reverses direction at the end of the input pulse. This is due to stored charge flowing out of the base terminal.

At about $t = 520$ ns, most of the excess charge in the base has been removed, and the collector current begins to fall, causing the output voltage to rise. However, the output voltage rises gradually because of the junction capacitances. The transistor eventually returns to the cutoff state.

As expected, the circuit acts as a logic inverter. When the input is low, the output eventually becomes high. Similarly, when the input is high, the output eventually becomes low. Because of charge-storage effects, changes in the output do not occur immediately when the input changes. Of course, in many applications it is desirable for the switching delays to be as short as possible.

Switching-Interval Definitions

Often, BJT data sheets give specifications for switching time intervals for test circuits similar to the RTL inverter. We define the *start* of a logic transition as the point at which 10% of the voltage change has occurred. For example, the start of the leading edge of the 3-volt input pulse is the point at which the input pulse reaches 0.3 V. Similarly, the start of the leading edge of the output pulse is the point at which v_o has fallen to 2.7 V. These start points are labeled in Figure 4.50.

Similarly, we define the *end* of a logic transition as the point at which 90% of the voltage change has occurred. Data sheets for BJTs intended for switching applications often specify the following switching intervals:

- t_d is the **delay time**, measured from the start of the leading edge of the input to the start of the leading edge of the output. (See Figure 4.50.)
- t_r is the **rise time**, measured from the start point to the end point of the leading edge of the output pulse. For example, in Figure 4.50, t_r is the interval between the 2.7-V point and the 0.3-V point on the leading edge of the output pulse. (Notice that the *rise* time is defined for the leading edge of the output pulse, even though this is a *negative-going* edge.)
- t_s is the **storage time**, measured from the start point on the trailing edge of the input pulse to the start point on the trailing edge of the output pulse.
- t_f is the **fall time**, measured between the start and end points on the trailing edge of the output pulse.

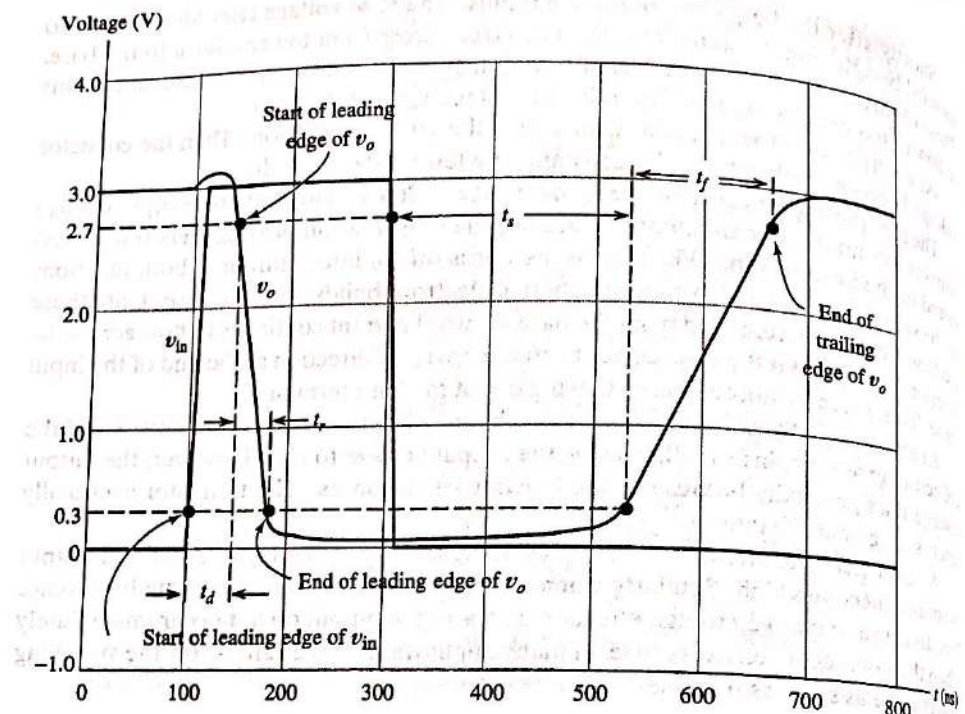


Figure 4.50 Waveforms illustrating turn-on and turn-off times.

If you examine a manufacturer's data sheet for the 2N2222 or the very similar 2N2222A, you will find that typical values are given for t_d , t_r , t_s , and t_f for stated test conditions. The actual test circuits are usually shown on the data sheet.

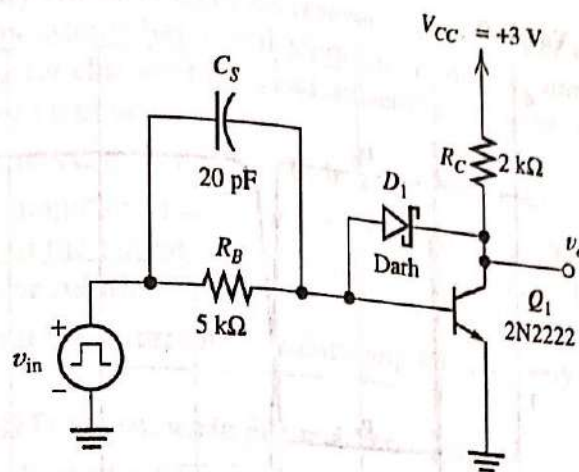
Device Design

Several aspects of device construction influence a circuit's switching speed. For example, the device capacitances can be reduced by reducing junction areas. Doping levels and junction grading also affect junction capacitances. A thinner base region leads to quicker diffusion of minority carriers out of the base region. Selected impurities can be used to reduce the lifetime of minority carriers. Device designers can make many important contributions to fast switching circuits.

Speedup Techniques

Two additional techniques for speeding up the transitions of the RTL inverter are shown in Figure 4.51. First, a **speedup capacitor** has been added in parallel with the base resistor R_B . Second, a **Schottky clamp diode** has been added between the base and the collector terminal. Schottky diodes conduct at lower forward biases than the usual pn junctions do. Also, Schottky diodes do not exhibit charge-storage effects.

Figure 4.51
The speed-up capacitor C_S and Schottky clamp diode D_1 dramatically reduce the switching times of the RTL inverter.



First, we used Schematics to draw the circuit, initially employing the breakout part Dbreak for the diode. Then we click on the diode to select it and use the **edit/model/edit instance model** command to bring up the window illustrated in Figure 4.52, where we change the model name to Darh and enter diode model parameters corresponding to a typical Schottky diode.

Next, we simulate the circuit, and Probe starts and displays the waveforms shown in Figure 4.53. Notice that the switching times for this circuit are much smaller than for the simple RTL inverter of Figure 4.46. One reason for this is that the speed-up capacitor couples the leading edge of the input pulse to the base. The voltage across a capacitor cannot change instantaneously in a real-world circuit. Hence, the rapid increase of the input pulse causes a rapid increase in v_{BE} . Thus, the transistor is forced to turn on quickly. On the other hand, without the speedup capacitor, the junction capacitances must be charged through R_B , and v_{BE} rises more gradually.

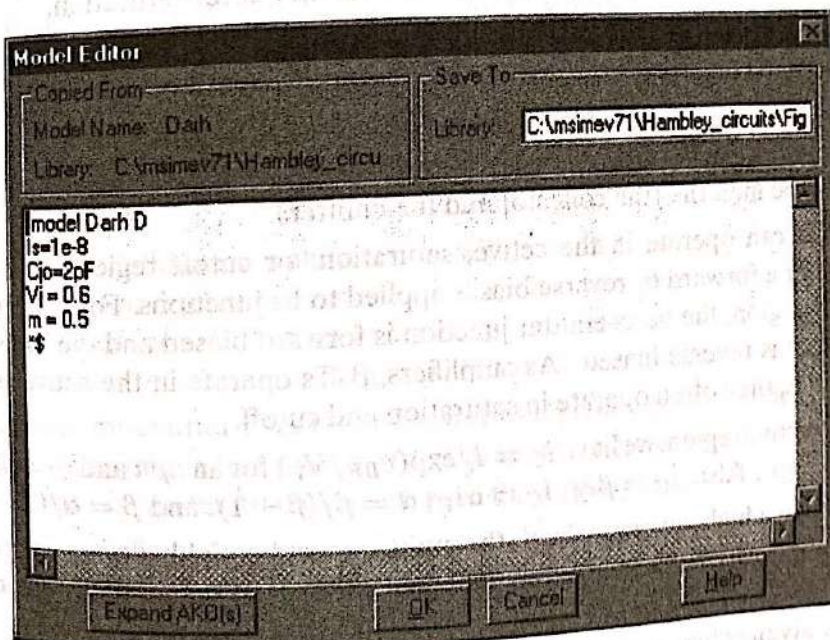


Figure 4.52 Model-editor window.

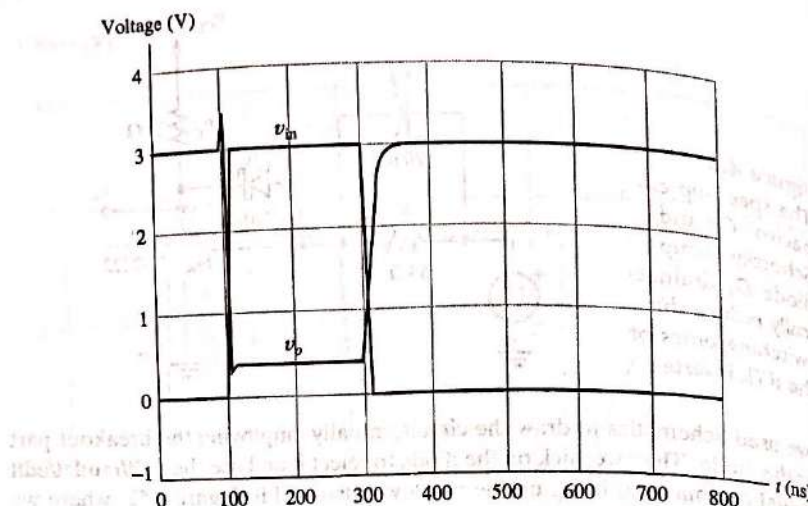


Figure 4.53 Waveforms of the Schottky-clamped RTL inverter.

Junction capacitances and an excess accumulation of minority charges in the base region slow the switching of BJT circuits. For faster switching, circuits should be designed so that the BJTs do not enter saturation.

Another reason the circuit is faster is that the Schottky diode prevents the BJT from entering the saturation region. When the collector voltage reaches approximately 0.4 V, the diode conducts and reduces the base current that is available to the transistor. Thus, the output voltage is not allowed to fall below about 0.3 V, and the transistor remains in the active region, which greatly reduces the concentration of electrons in the base region. Consequently, the storage interval is virtually eliminated.

An important point for the circuit designer is that, if fast switching is important, BJT logic circuits should be designed so that the BJTs do not enter saturation.

SUMMARY

- An *n*pn BJT consists of a layer of *p*-type material (the base) between two layers of *n*-type material (the collector and the emitter).
- A BJT can operate in the active, saturation, or cutoff regions, depending on whether a forward or reverse bias is applied to its junctions. For operation in the active region, the base-emitter junction is forward biased and the base-collector junction is reverse biased. As amplifiers, BJTs operate in the active region. As switches, they often operate in saturation and cutoff.
- In the active region, we have $i_C = I_s \exp(v_{BE}/V_T)$ for an *n*pn and $i_C = I_s \exp(-v_{BE}/V_T)$ for a *p*np. Also, $i_C = \beta i_B$, $i_C = \alpha i_E$, $\alpha = \beta/(\beta + 1)$, and $\beta = \alpha/(1 - \alpha)$.
- To attain a high current gain β , the emitter must be highly doped compared with the base, the base must be thin, and recombination in the base region must be minimized.
- For a given collector current, the base-to-emitter voltage decreases in magnitude by 2 mV/K.

- Some important secondary effects in BJTs are reverse leakage current, which can be important at high temperatures, base-width modulation, which accounts for the upward slope of the collector characteristics, and collector breakdown, which can be caused by avalanche or by punch-through.
- Simple BJT amplifier circuits can be analyzed by load-line techniques.
- Distortion occurs in BJT amplifiers due to nonlinearity of the input characteristic and nonuniform spacing of the output characteristics. Clipping occurs if the BJT swing reaches saturation or cutoff.
- Except for voltage polarities and current directions, *pnp* BJTs are very similar to *npn* BJTs.
- Large-signal models of BJTs are shown in Figure 4.19 on page 232.
- In the large-signal dc analysis of a BJT circuit, we assume that the circuit is operating in the saturation, active, or cutoff region. Then we analyze the circuit by using the appropriate model for the BJT. Next, we check to make sure that the device constraints for the assumed region are satisfied. If they are not, we assume a different operating region and repeat.
- The four-resistor bias circuit shown in Figure 4.28a on page 242 is commonly used in discrete design. A rule of thumb in designing this circuit is to make the currents through R_1 and R_2 10 to 20 times the maximum expected base current and to make the voltages across R_C and R_E equal to one-third of V_{CC} .
- Current sources and direct coupling are commonly used in biasing IC amplifiers.
- The small-signal equivalent circuit for a BJT consists of a resistance r_π and a current source βi_b (or $g_m v_{be}$). Given the Q -point collector current I_{CQ} and β , we can compute the small-signal parameters $r_\pi = \beta V_T / I_{CQ}$ and $g_m = I_{CQ} / V_T$.
- A BJT amplifier circuit can be analyzed by drawing the small-signal equivalent circuit and applying circuit laws. Important amplifier characteristics are voltage gain, current gain, input impedance, and output impedance.
- The common-emitter amplifier is inverting. Its voltage and current gains are both potentially larger than unity (100 is typical). Input and output impedance magnitudes are moderate compared with those of other BJT and FET amplifier configurations.
- The emitter follower is noninverting, with a voltage gain slightly less than unity. The current and power gains are potentially larger than unity. In general, the output impedance of the emitter follower is much lower and the input impedance is higher than the corresponding impedances of other single-stage BJT amplifiers.
- The common-emitter amplifier is noninverting and can have a high voltage gain. The current gain is less than unity. The input impedance is low and the output impedance is moderate compared with the corresponding impedances of other BJT amplifiers.
- Logic inverters and NOR gates can be constructed with BJTs and resistors.
- Junction capacitances and accumulation of excess minority charge in the base region slow the switching of BJT circuits. For faster switching, circuits should be designed so that the BJTs do not enter saturation.

PROBLEMS

Section 4.1: Basic Operation of the *n*pn Bipolar Junction Transistor

- 4.1. Draw the circuit symbol for an *n*pn BJT. Label the terminals and the currents. Choose reference directions that agree with the true direction of the current for operation in the active region.
- 4.2. To forward bias a *pn* junction, which side of the junction should be connected to the positive voltage? In the active region, which type of bias (forward or reverse) is applied to the emitter–base junction? To the collector–base junction?
- 4.3. Sketch the input characteristic curve for a typical small-signal silicon *n*pn BJT at room temperature. Sketch the output characteristic curves if $\beta = 250$.
- 4.4. A certain *n*pn silicon transistor has $v_{BE} = 0.7$ V for $i_B = 0.1$ mA at a temperature of 30°C . Sketch the input characteristic to scale at 30°C . What is the approximate value of v_{BE} for $i_B = 0.1$ mA at 180°C ? (Use the rule of thumb that v_{BE} is reduced in magnitude by 2 mV per degree increase in temperature.) Sketch the input characteristic to scale at 180°C .
- 4.5. A certain *n*pn silicon transistor has $\beta = 100$ and $i_B = 0.1$ mA. Sketch i_C against v_{CE} for v_{CE} ranging from 0 to 5 V. Repeat for $\beta = 300$. Ignore second-order effects.
- 4.6. Sketch the output characteristics of a BJT, illustrating the Early voltage and collector breakdown.
- 4.7. An *n*pn transistor has $\beta \cong 200$ and $i_B = 0.1$ mA. The collector-to-emitter breakdown voltage is 20 V, and the Early voltage is $V_A = 100$ V. Sketch i_C against v_{CE} to scale for the voltage range from 0 to 25 V.
- 4.8. An *n*pn transistor is operating with the base–emitter junction forward biased and the base–collector junction reverse biased. If $i_C = 9$ mA for $i_B = 0.3$ mA, find i_E , α , and β .
- 4.9. A transistor has $\beta = 50$. What is the value of α ?
- 4.10. Consider an *n*pn transistor at room temperature that has $I_{ES} = 10^{-13}$ A, $\beta = 100$, $v_{CE} = 10$ V, and $i_E = 10$ mA. Find v_{BE} , v_{BC} , i_B , i_C , and α . (Assume that $V_T = 26$ mV at room temperature.)
- 4.11. Consider the circuit shown in Figure P4.11. The transistors Q_1 and Q_2 are identical, both having $I_{ES} = 10$ fA $= 10^{-14}$ A and $\beta = 100$. Find V_{BE} and I_{C2} . Assume a temperature of 300 K for both transistors. (Hint: Both transistors are operating in the active region. Because the transistors are identical and have identical values of V_{BE} , their collector currents are equal.)

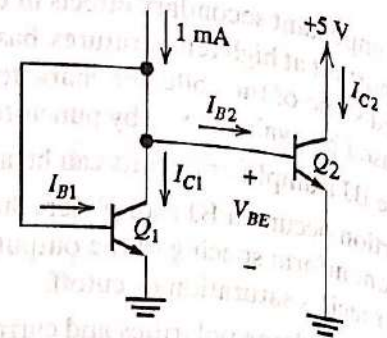


Figure P4.11

- 4.12. Repeat Problem 4.11 if Q_1 has $I_{ES1} = 10$ fA $= 10^{-14}$ A, and $\beta_1 = 100$, whereas Q_2 has $I_{ES2} = 100$ fA $= 10^{-13}$ A, and $\beta_2 = 100$.
- 4.13. Two transistors Q_1 and Q_2 connected in parallel are equivalent to a single transistor as indicated in Figure P4.13. If the individual transistors have $I_{ES1} = I_{ES2} = 10^{-13}$ A and $\beta_1 = \beta_2 = 100$, find I_{ES} and β for the equivalent transistor. Assume the same temperature for all transistors.

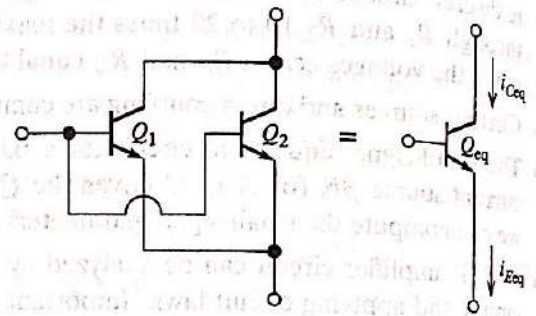


Figure P4.13

- 4.14. Find the values of β for the transistors of Figure P4.14.

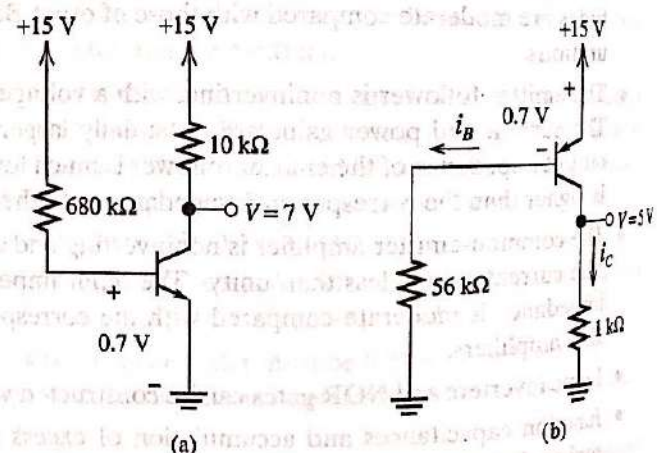


Figure P4.14

4.15. An *nnp* transistor has $V_{BE} = 0.7$ V for $I_E = 10$ mA. Find V_{BE} if $I_E = 1$ mA. Repeat for $I_E = 1$ μ A. Assume a temperature of 300 K.

4.16. **Beta meter.** Design a " β -meter" for measurement of the β of small-signal *nnp* silicon transistors at room temperature. Assume that $v_{BE} = 0.7$ for the transistors to be measured. The following parts are available:

1. A 1-mA-full-scale meter having a resistance of 150 Ω .
2. Standard 5%-tolerance resistors. (See Appendix A.)
3. Potentiometers of 100 Ω , 1 k Ω , 10 k Ω , 100 k Ω , and 1 M Ω .
4. A 4.7-V Zener diode.
5. Switches and mechanical components, as required.
6. A 9-V "transistor" battery.

The meter is to have switch-selectable full-scale values of $\beta_{FS} = 10, 100$, and 1000. Adjustments are to be provided that allow calibration of the meter, which is to provide accurate readings for battery voltages ranging from 7 to 9 V. Under reasonable operating conditions (including short-circuited test terminals), the battery drain should not exceed 5 mA.

- Suggestions:**
1. Use a Zener diode regulator to obtain a constant source voltage for delivering base current to the transistor.
 2. Use a switch and resistor network to apply a suitable base current to the transistor under test for each range of β to be measured.
 3. Use the meter to measure the collector current with full scale corresponding to $\beta = 10, 100$, or 1000.

4.17. Use SPICE to obtain output characteristics for an *nnp* BJT having $I_s = 10^{-16}$ A, $\beta = 200$, and $V_A = 25$ V. Allow v_{CE} to range from 0 to 10 V, and let $i_B = 0, 10, 20, 30, 40$, and 50 μ A.

4.18. Use SPICE to obtain input characteristics for an *nnp* BJT having $I_s = 10^{-16}$ A, $\beta = 200$, and $V_A = 25$ V. Set $v_{CE} = 10$ V, and allow v_{BE} to range from 0 to 0.7 V.

Section 4.2: Load-Line Analysis of a Common-Emitter Amplifier

4.19. What can cause distortion in BJT amplifiers?

4.20. Consider the circuit of Figure 4.10. Assume that $V_{CC} = 20$ V, $V_{BB} = 0.8$ V, $R_B = 40$ k Ω , and $R_C = 2$ k Ω . The input signal is a 0.2-V-peak, 1-kHz sinusoid given by $v_{in}(t) = 0.2 \sin(2000\pi t)$. The common-emitter characteristics for the transistor are shown in Figure P4.20. Find the maximum, minimum, and Q -point values for v_{CE} . What is the approximate voltage gain for this circuit?

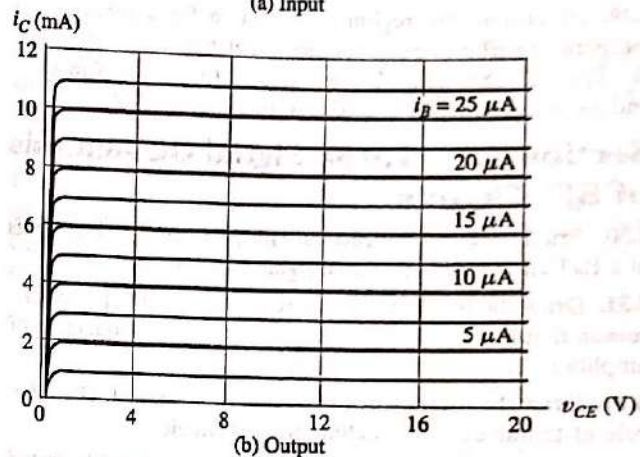
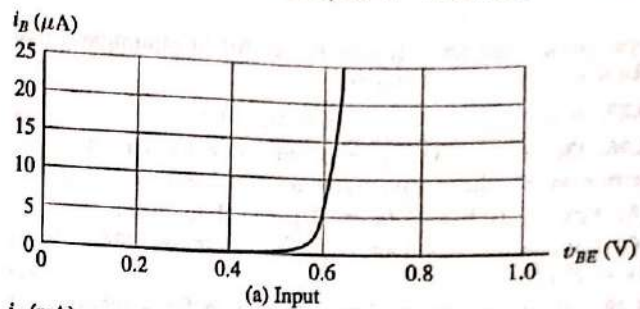


Figure P4.20

4.21. Repeat Problem 4.20 for $R_C = 10$ k Ω . What can you say about the waveform for $v_{CE}(t)$?

4.22. Repeat Problem 4.20 for $V_{BB} = 0.3$ V. Why is the gain so small in magnitude?

Section 4.3: The *pnp* Bipolar Junction Transistor

4.23. Draw the circuit symbol for a *pnp* BJT. Label the terminals and the currents. Choose reference directions that agree with the true directions of the current for operation in the active region.

4.24. A certain *pnp* silicon transistor has $\beta = 100$ and $i_B = 0.1$ mA. Sketch i_C against v_{CE} for v_{CE} ranging from 0 to -5 V. Repeat for $\beta = 300$. Ignore second-order effects.

4.25. At a temperature of 30°C, a particular *pnp* transistor has $V_{BE} = -0.7$ V for $I_E = 2$ mA. Estimate V_{BE} for $I_E = 0.1$ mA at a temperature of 180°C.

Section 4.4: Large-Signal DC Circuit Models

4.26. Draw the large-signal dc circuit model for a silicon *nnp* transistor operating in the active region at room temperature. Include the constraints of any currents or voltages that guarantee

operation in the active region. Repeat for the saturation region. Repeat for the cutoff region.

4.27. Repeat Problem 4.26, for a *pnp* transistor.

4.28. Determine the region of operation for a room-temperature silicon *nnp* transistor that has $\beta = 100$ if (a) $V_{CE} = 10\text{ V}$ and $I_B = 20\text{ }\mu\text{A}$; (b) $I_C = I_B = 0$; (c) $V_{CE} = 3\text{ V}$ and $V_{BE} = 0.4\text{ V}$; (d) $I_C = 1\text{ mA}$ and $I_B = 50\text{ }\mu\text{A}$.

4.29. Determine the region of operation for a room-temperature silicon *pnp* transistor that has $\beta = 100$ if (a) $V_{CE} = -5\text{ V}$ and $V_{BE} = -0.3\text{ V}$; (b) $I_C = 10\text{ mA}$ and $I_B = 1\text{ mA}$; (c) $I_B = 0.05\text{ mA}$ and $V_{CE} = -5\text{ V}$.

Section 4.5: Large-Signal DC Analysis of BJT Circuits

4.30. Briefly discuss the procedure for performing a dc analysis of a BJT circuit using the large-signal circuit models.

4.31. Draw the fixed-base bias circuit. What is the principal reason that this circuit is unsuitable for the mass production of amplifier circuits?

4.32. Draw the four-resistor bias circuit for the BJT. Give the rule-of-thumb design guidelines for this circuit.

4.33. Use the large-signal models for the transistors illustrated in Figure 4.19 to find I_C and V_{CE} for the circuits of Figure P4.33. Assume that $\beta = 100$. Repeat for $\beta = 300$ and compare the results for both values.

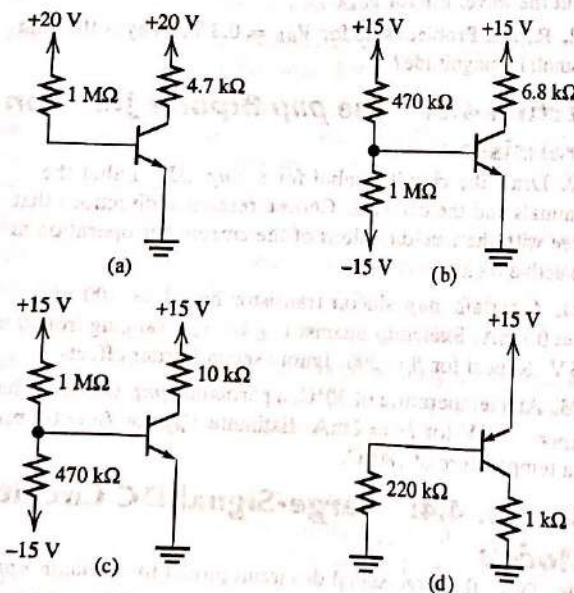


Figure P4.33

4.34. Find I and V in the circuits shown in Figure P4.34. For all transistors, assume that $\beta = 100$ and $|V_{BE}| = 0.7\text{ V}$ in both the active and saturation regions. Repeat for $\beta = 300$.

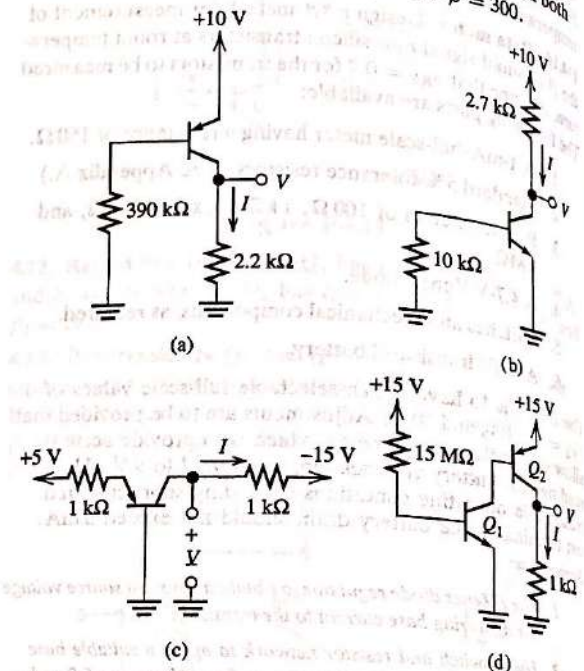


Figure P4.34

4.35. Consider the circuit displayed in Figure P4.35. A Q -point value for I_C between a minimum of 4 mA and a maximum of 5 mA is required. Assume constant resistor values, and suppose that β ranges from 100 to 300 . It is desired that R_B have the largest possible value while meeting the other constraints. Find the values of R_B and R_E . The resistors in this problem are not required to be nominal values.

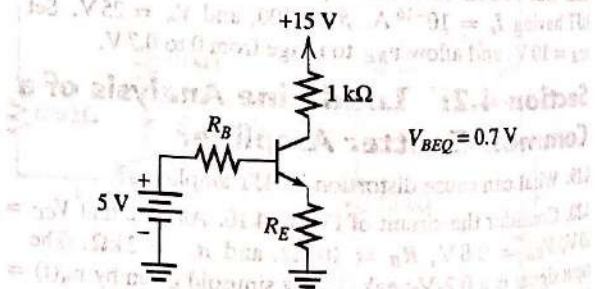


Figure P4.35

4.36. Consider the four-resistor bias network of Figure 4.28a with $V_{CC} = 15\text{ V}$, $R_1 = 100\text{ k}\Omega$, $R_2 = 47\text{ k}\Omega$, $R_C = 4.7\text{ k}\Omega$,

and $R_E = 4.7 \text{ k}\Omega$. Suppose that β ranges from 50 to 200, $V_{BE} = 0.7 \text{ V}$, and the resistors have a tolerance of $\pm 5\%$. Find the maximum and minimum values of I_C .
 4.37. Consider the circuit shown in Figure P4.37. Find R_1 and R_C if a bias point of $V_{CE} = 5 \text{ V}$ and $I_C = 2 \text{ mA}$ is required. What are the closest 5%-tolerance nominal values for R_1 and R_C ?

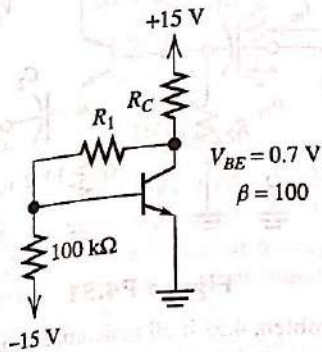


Figure P4.37

4.38. Find I_C and V_{CE} in the circuit of Figure P4.38.

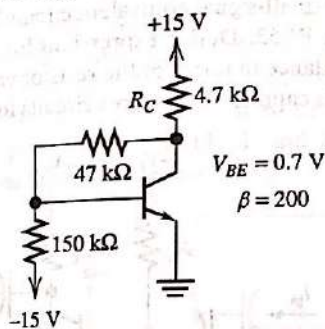


Figure P4.38

D4.39. **Four-resistor bias circuit design.** Suppose that $V_{CC} = 20 \text{ V}$, $R_C = 1 \text{ k}\Omega$, and a Q -point of $I_{CQ} \cong 5 \text{ mA}$ is desired. The transistor has β ranging from 50 to 150. Design a four-resistor bias circuit. Use standard 5%-tolerance resistor values. *Many correct answers exist for this problem. Design so that approximately one-third of the supply voltage is dropped across R_C , one-third across the transistor (V_{CE}), and one-third across R_E .*

Section 4.6: Small-Signal Equivalent Circuits

- 4.40. Draw two small-signal equivalent circuits for the BJT.
 4.41. Give the formulas for determining r_π and g_m , assuming that β and the Q -point are known.
 4.42. A certain npn silicon transistor at room temperature has $\beta = 100$. Find the corresponding values of g_m and r_π if

$I_{CQ} = 1 \text{ mA}$, 0.1 mA , and $1 \mu\text{A}$. Assume that the device is operating in the active region.

Section 4.7: The Common-Emitter Amplifier

4.43. Why are coupling capacitors often used to connect the signal source and the load to discrete amplifier circuits? Should coupling capacitors be used if it is necessary to amplify dc signals? Explain.

4.44. Draw the circuit diagram of a common-emitter amplifier circuit that uses the four-resistor biasing network. Include a signal source and a load resistance.

4.45. Consider the common-emitter amplifier of Figure P4.45. Draw the dc circuit and find I_{CQ} . Find the value of r_π . Then calculate values for A_v , A_{v0} , Z_{in} , A_i , G , and Z_o . Assume that the circuit is operating in the midband region for which the coupling and bypass capacitors are short circuits.

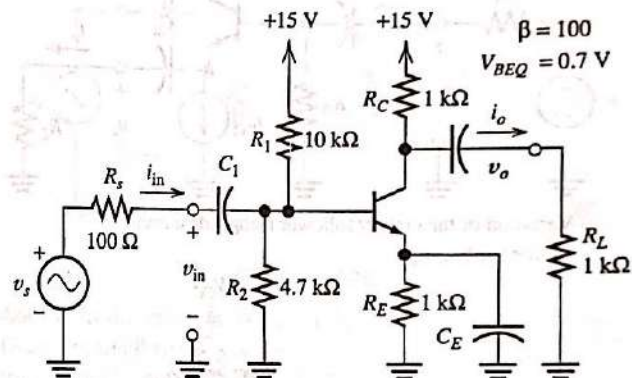


Figure P4.45

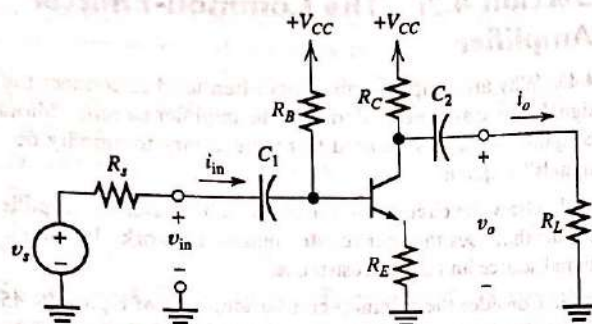
4.46. Repeat Problem 4.45 if all resistance values, including R_s and R_L , are increased in value by a factor of 100. If you have also worked Problem 4.45, prepare a table comparing the results for the low-impedance amplifier with those for the high-impedance amplifier. (*Comment: When we consider the high-frequency response of these circuits, we will find that the gain of the high-impedance circuit falls off at lower frequencies than the gain of the low-impedance circuit does. Thus, if we want constant gain to extend to very high frequencies, we should use the low-impedance circuit.*)

Section 4.8: The Emitter Follower

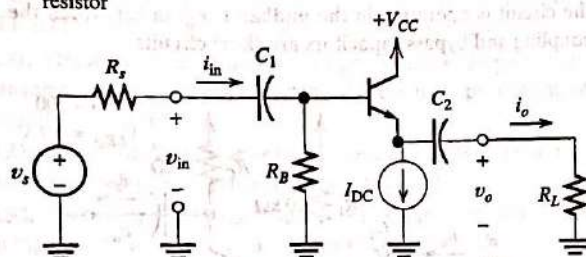
4.47. Draw the circuit diagram of a discrete emitter follower.

4.48. For a small-signal midband analysis of an amplifier, with what do we replace the coupling capacitors? Dc voltage sources? Dc current sources? Very large inductors?

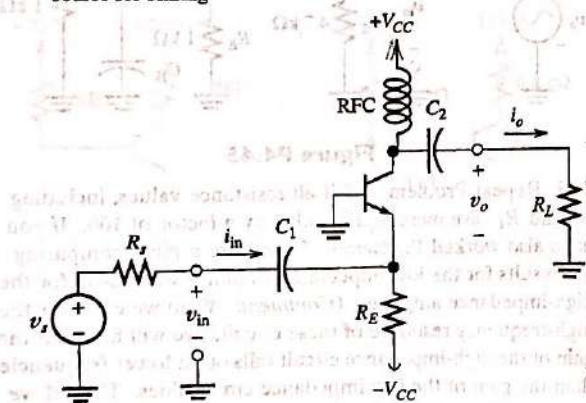
4.49. Draw the small-signal equivalent circuits for the circuits illustrated in Figure P4.49.



(a) Common-emitter amplifier with unbypassed emitter resistor



(b) Variation of the emitter follower using a dc current source for biasing



(c) Variation of the common-base amplifier [assume that the radio-frequency choke (RFC) is an open circuit for the ac signals]

Figure P4.49 Amplifier circuits.

4.50. Briefly describe the small-signal analysis procedure for finding the output resistance of an amplifier.

4.51. Consider the emitter-follower amplifier of Figure P4.51. Draw the dc circuit and find I_{CQ} . Find the value of r_{π} . Then calculate midband values for A_v , A_{v_o} , Z_{in} , A_i , G , and Z_o .

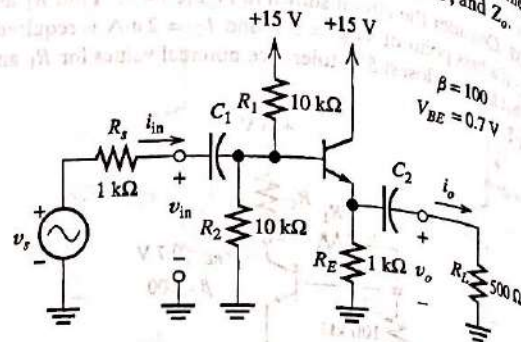


Figure P4.51

4.52. Repeat Problem 4.51 if all resistance values, including R_s and R_L , are increased in value by a factor of 100. Prepare a table comparing the results for the low-impedance amplifier with those for the high-impedance amplifier.

4.53. Draw the small-signal equivalent circuit for the amplifier shown in Figure P4.53. Derive expressions for the voltage gain and input impedance in terms of the resistor values, r_{π} , and β . Assume that the capacitors are short circuits for the signals.

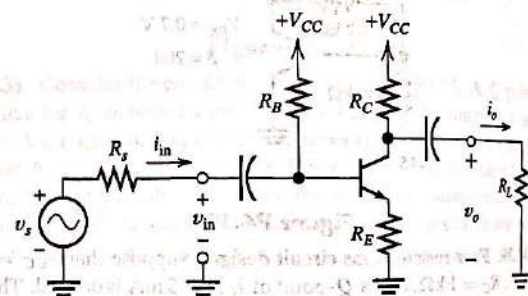


Figure P4.53

4.54. Find the values of I_{CQ} , r_{π} , A_v , and Z_{in} for the circuit of Problem 4.53 if $V_{CC} = 15$ V, $\beta = 100$, $V_{BEQ} = 0.7$, $R_B = 270$ k Ω , $R_C = 1$ k Ω , $R_E = 100$ Ω , and $R_L = 1$ k Ω . Repeat for $R_E = 0$ and prepare a table comparing the results.

4.55. Find an expression for the output impedance of the amplifier displayed in Figure P4.53.

4.56. Draw the small-signal equivalent circuit of the circuit shown in Figure P4.56, and derive expressions for the input impedance and voltage gain. Assume that the capacitors are short circuits for the signals.

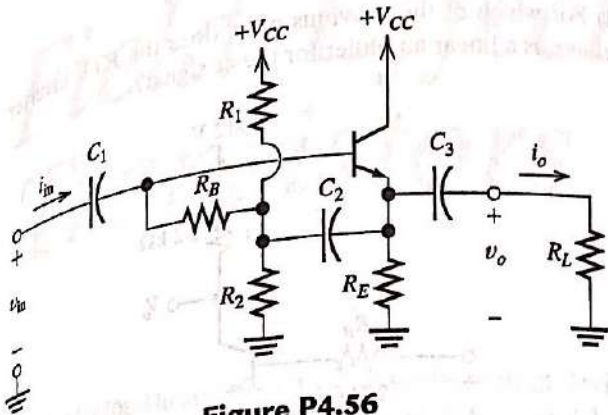


Figure P4.56

4.57. Consider the circuit of Figure P4.56 with $V_{CC} = 15\text{ V}$, $R_1 = 10\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_B = 100\text{ k}\Omega$, $R_E = 10\text{ k}\Omega$, and $R_L = 4.7\text{ k}\Omega$. Assume a transistor having $\beta = 200$ and $V_{BEQ} = 0.7\text{ V}$. Evaluate the expressions found in Problem 4.56 for input impedance and voltage gain.

4.58. Consider the common-emitter amplifier circuits displayed in Figure P4.58. The ac sources shown in series with the dc supply represent power-supply hum. Draw the small-signal equivalent circuits. Be sure to include the hum source in your model. Notice that if $v_{hum} = 0$, the two equivalent circuits are identical. Find an expression for the voltage gain v_o/v_{in} if $v_{hum} = 0$. Then set $v_{in} = 0$ and solve for $A_{hum} = v_o/v_{hum}$ if $v_{hum} = 0$. Evaluate the gain values for $V_{CC} = 15\text{ V}$, $V_{BEQ} = 0.7\text{ V}$, $\beta = 100$, $R_B = 1\text{ M}\Omega$, and $R_C = 4.7\text{ k}\Omega$. Which of these circuits is preferable? Why?

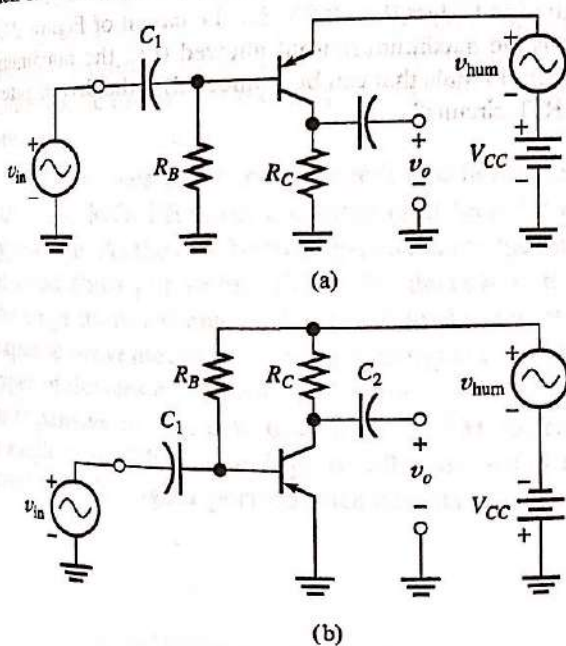


Figure P4.58

4.59. Consider the common-emitter amplifier illustrated in Figure P4.59. The ac source in series with the dc supply represents power-supply hum. (a) Assume that a large bypass capacitor is connected between points A and E. Draw the small-signal equivalent circuit, including the hum source. Solve for $A_{hum} = v_o/v_{hum}$, assuming that $v_i = 0$.

(b) Now consider connecting the emitter bypass capacitor from point E to ground, and again find A_{hum} . Notice that if $v_{hum} = 0$, the two equivalent circuits are identical, so they perform equally as far as the source signal v_i is concerned. Which option is best for the connection of the bypass capacitor? Why?

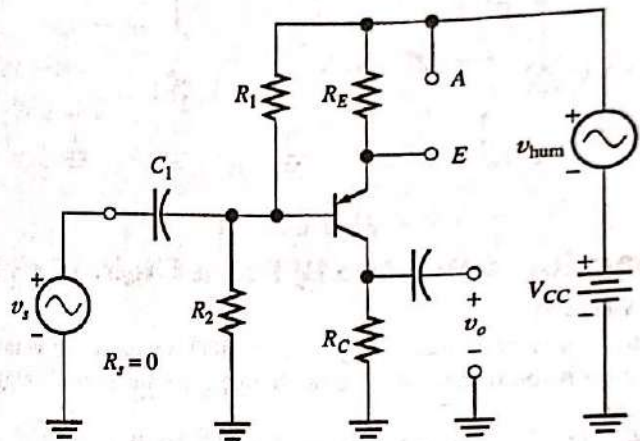


Figure P4.59

4.60. Find the value of V_{CEQ} for the circuit of Figure P4.60. Draw the small-signal equivalent circuit and find an expression for the small-signal output impedance Z_o in terms of β , r_{π} , R_1 , and R_2 . Evaluate Z_o for the values shown in the figure.

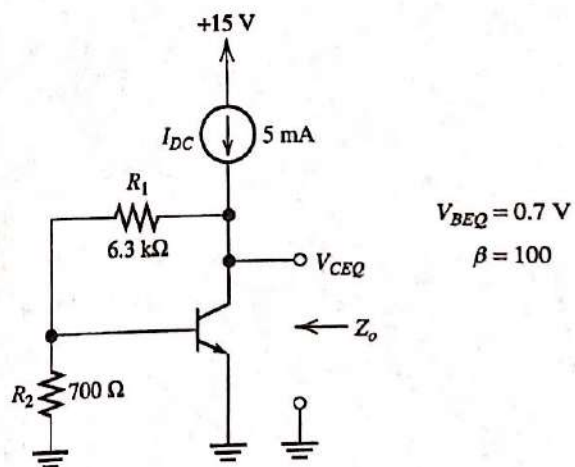


Figure P4.60

4.61. Consider the voltage-reference circuits illustrated in Figure P4.61. The dynamic small-signal resistance of each Zener diode is $r_d = 100 \Omega$. Find the dc output voltage of each circuit. Draw the small-signal equivalent circuit, and derive an expression for the output impedance of each circuit. Evaluate the expressions for the resistances and transistor parameters shown.

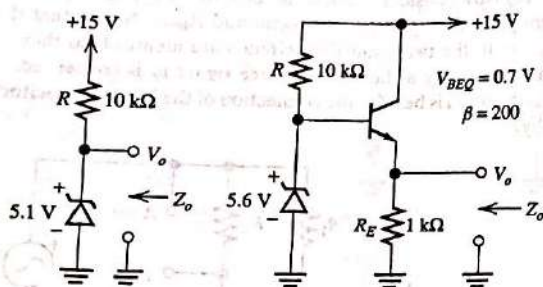


Figure P4.61

Section 4.9: The BJT as a Digital Logic Switch

- 4.62. Draw the circuit diagram of an RTL inverter. In what region is the transistor intended to operate if the input is high? Low?
- 4.63. Draw the circuit diagram of an RTL NOR gate.
- 4.64. Consider the transfer characteristic of the RTL inverter shown in Figure 4.43. Sketch the transfer characteristic to scale for the values shown in Figure P4.64. Sketch the output voltage $v_o(t)$ to scale versus time if (a) $v_{in}(t) = 2.7 \sin(2000\pi t)$; (b) $v_{in}(t) = 2.7 + \sin(2000\pi t)$; (c) $v_{in}(t) = 2.7 + 5 \sin(2000\pi t)$.

(d) For which of the previous parts does the RTL inverter behave as a linear amplifier for the ac signal?

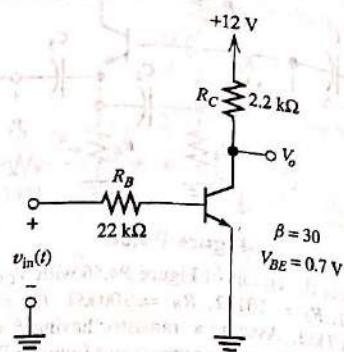


Figure P4.64

- 4.65. Consider the RTL inverter of Figure P4.64. Assuming that we require the minimum output voltage with the transistor in the cutoff region to be $V_{OH} = 6V$, what is the maximum number of driven gates (i.e., the fan-out) that can be connected? Assume that the driven gates have input circuits identical to those of the RTL inverter.
- 4.66. If $V_{in} = 6V$ for the circuit of Figure P4.64, find the minimum value of β to ensure that the transistor is in saturation.
- 4.67. If V_{OL} (i.e., the output voltage in the low logic state) is required to be less than $0.5V$ for the circuit of Figure P4.64, what is the maximum fan-out allowed (i.e., the maximum number of inputs that can be connected) if the driven gates are also RTL circuits?

Field-Effect Transistors

Field-effect transistors (FETs) are important devices that, like BJTs, are used as amplifiers and logic switches. We will discuss several types of FETs. The most important type is the enhancement-mode **metal-oxide-semiconductor field-effect transistor (MOSFET)**, which is the primary device that underlies the rapid advances that have occurred in digital electronics over the past several decades. Two other types of FETs are the **depletion-mode MOSFET** and the **junction field-effect transistor (JFET)**.

Compared with BJTs, MOSFETs can occupy less chip area and can be fabricated with fewer processing steps. Complex digital circuits such as memories and microprocessors are often implemented solely with MOSFETs. On the other hand, BJTs are capable of producing large output currents that are needed for fast switching of capacitive loads, such as circuit board traces that interconnect digital chips. Each type of device has some applications in which it performs better than the others.

More processing steps are needed to fabricate both BJTs and MOSFETs on the same chip than for either type alone. As the number of steps increases, the number of good chips per wafer (the yield) decreases, making the chips more expensive. Until relatively recently, this expense prevented designers from using many different types of devices on a given chip. However, now it is not as expensive to fabricate both BJTs and MOSFETs on a single chip. The technology is called **BiCMOS** and is used to make higher performance circuits.

5

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5.1 NMOS TRANSISTORS

Overview

The physical structure of an n -channel enhancement-mode MOSFET (also known as an NMOS transistor) is shown in Figure 5.1. The device terminals are the **drain** (D), **gate** (G), **source** (S), and **body** (B). (Another commonly used term for **body** is **substrate**.) In normal operation, negligible current flows through the body terminal. In our discussion of the NMOS, we often assume that the body is connected to the source, so that we have a three-terminal device. The gate is insulated from the substrate by a thin layer of silicon dioxide, and negligible current flows through the gate terminal. When a sufficiently large (positive) voltage is applied to the gate relative to the source, electrons are attracted to the region under the gate, and a channel of n -type material is induced between the drain and the source. Then, if voltage is applied between the drain and the source, current flows into the drain, through the channel, and out of the source. Drain current is controlled by the voltage applied to the gate.

The channel length L and width W are illustrated in Figure 5.1. The length is in the range from 0.2 to $10\text{ }\mu\text{m}$, and the width ranges from 0.5 to $500\text{ }\mu\text{m}$. (Recall that $1\text{ }\mu\text{m} = 10^{-6}\text{ m}$.) The silicon dioxide layer is 0.05 to $0.1\text{ }\mu\text{m}$ thick. In the early days of MOS technology, the gate was made of aluminum. However, in most modern devices, the gate is a layer of a special type of silicon called **polysilicon**.

Device characteristics depend on L , W , and process parameters such as the doping level and the thickness of the oxide used. Usually, the process parameters are predetermined, but the circuit designer can adjust L and W to obtain the device best suited for a given application.

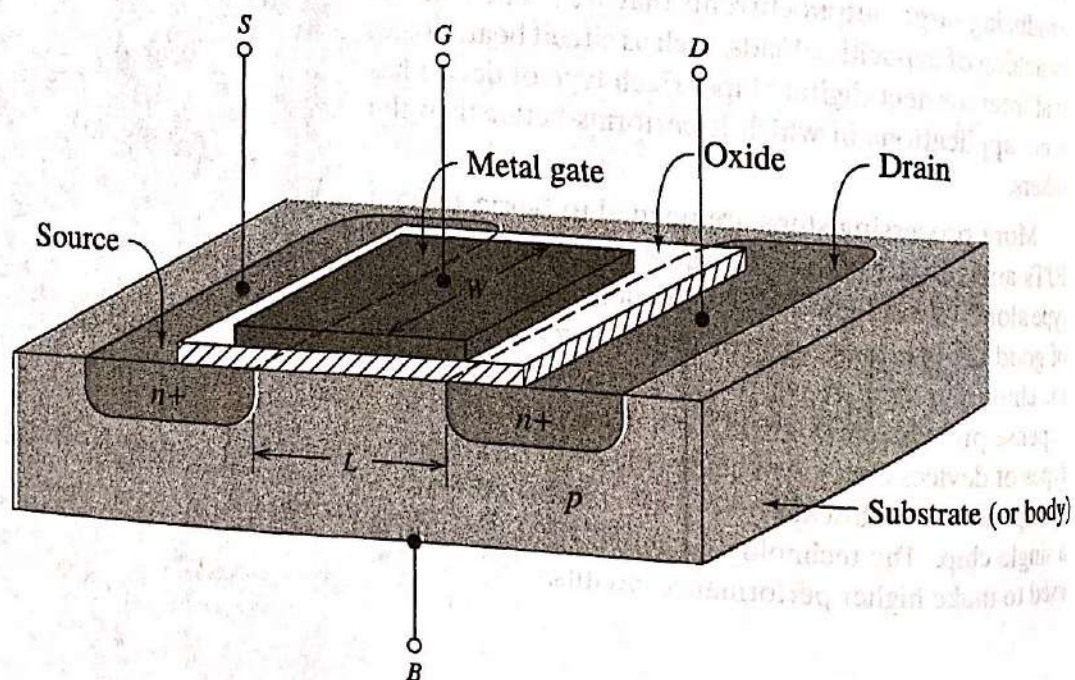
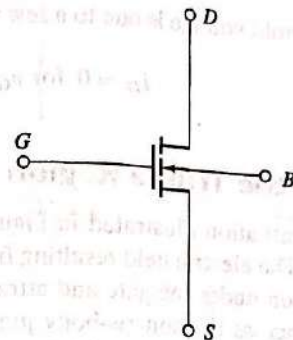


Figure 5.1 n -Channel enhancement MOSFET showing channel length L and channel width W .

Drain current is controlled by the voltage applied to the gate.

...the circuit designer can adjust L and W to obtain the device best suited for a given application.

Figure 5.2
Circuit symbol for
an enhancement-
mode n -channel
MOSFET.



The circuit symbol for the n -channel enhancement MOSFET is illustrated in Figure 5.2. We discuss the basic operation of this device next.

Operation in the Cutoff Region

Consider the situation shown in Figure 5.3. Suppose that a positive voltage is applied to the drain relative to the source and that we start with $v_{GS} = 0$. Notice that pn junctions appear at the drain-body and at the source-body interfaces. Virtually no current flows into the drain terminal, because the drain-body junction is reverse biased by the v_{DS} source. This is called the **cutoff region** of operation. As v_{GS} is increased, the device remains in cutoff until v_{GS} reaches a particular value called the **threshold voltage** V_{to} .

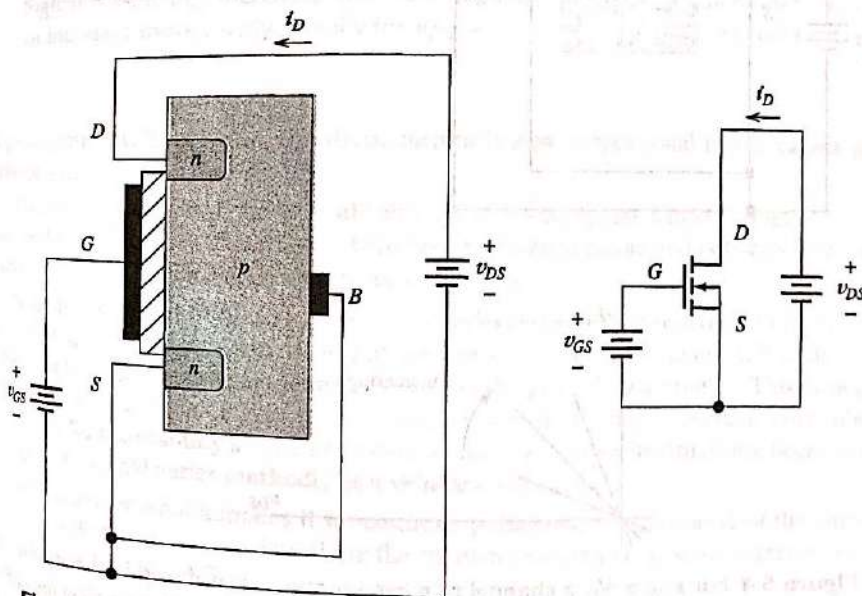


Figure 5.3 For $v_{GS} < V_{to}$ the pn junction between drain and body is reverse biased and $i_D = 0$.

Typically, the threshold voltage is one to a few volts. Thus, in cutoff, we have

$$i_D = 0 \text{ for } v_{GS} \leq V_{to} \quad (5.1)$$

Key equation for enhancement NMOS in cutoff.

The triode region is also called the linear region.

Operation in the Triode Region

Now consider the situation illustrated in Figure 5.4, in which v_{GS} is greater than the threshold voltage. The electric field resulting from the applied gate voltage has repelled holes from the region under the gate and attracted electrons that can easily flow in the forward direction across the source-body junction. This simultaneous repulsion and attraction produces an n -type channel between the drain and the source. Then, when v_{DS} is increased, current flows into the drain, through the channel, and out of the source. For small values of v_{DS} , the drain current is proportional to v_{DS} . Furthermore, for

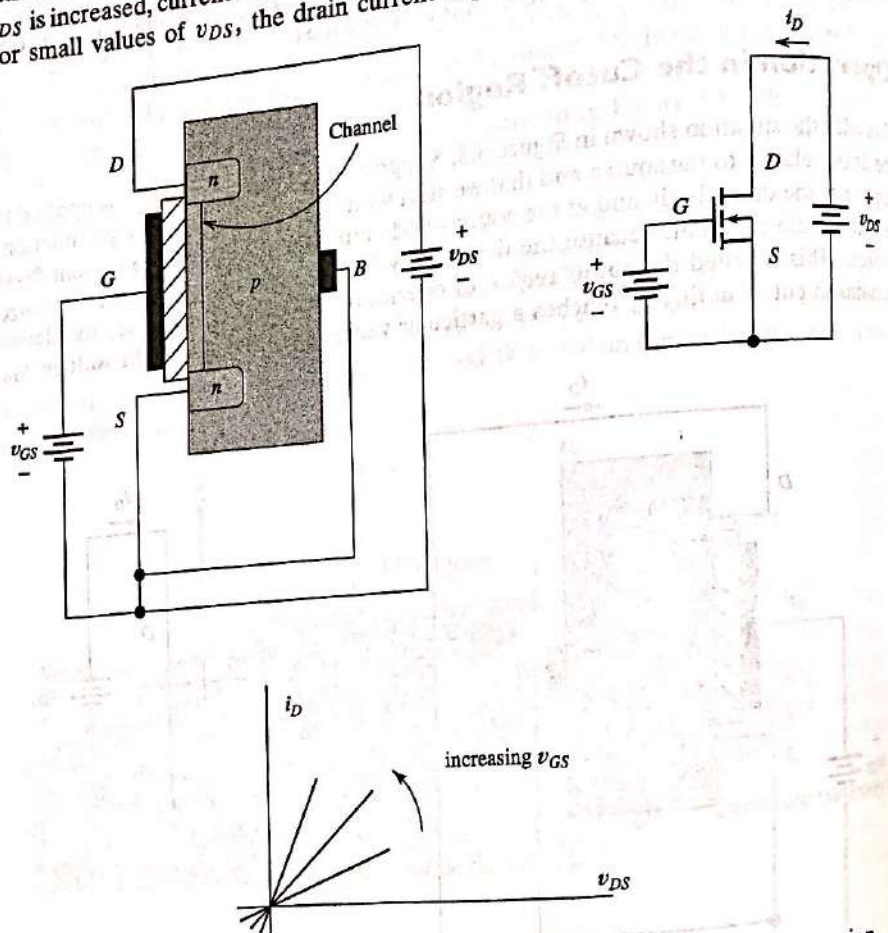


Figure 5.4 For $v_{GS} > V_{to}$ a channel of n -type material is induced in the region under the gate. As v_{GS} increases, the channel becomes thicker. For small values of v_{DS} , i_D is proportional to v_{DS} . The device behaves as a resistor whose value depends on v_{GS} .

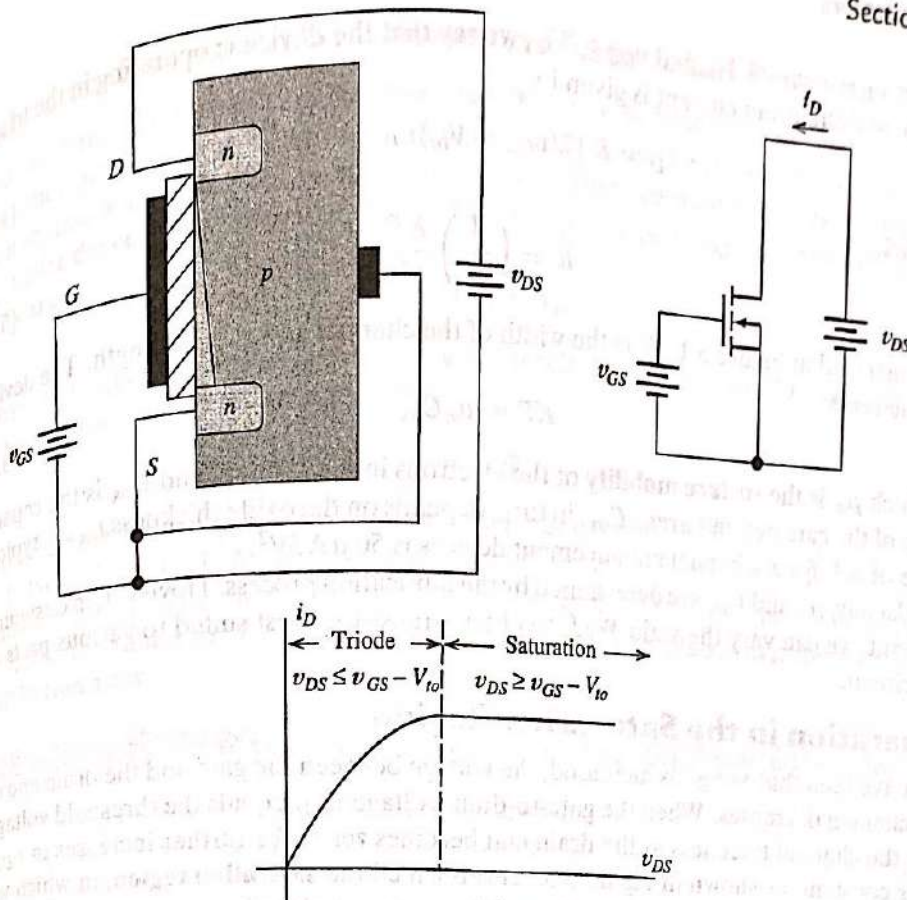


Figure 5.5 As v_{DS} increases, the channel pinches down at the drain end and i_D increases more slowly. Finally for $v_{DS} > v_{GS} - V_{to}$, i_D becomes constant.

a given (small) value of v_{DS} , the drain current is also proportional to the excess gate voltage, $v_{GS} - V_{to}$.

Plots of i_D versus v_{DS} for several values of gate voltage are shown in Figure 5.4. In the triode region, the NMOS device behaves as a resistor connected between drain and source, but the resistance decreases as v_{GS} increases.

Sometimes, circuit designers use FETs as **voltage-controlled resistors**. For example, we can design amplifiers in which the gain depends on a certain resistance value. By using a FET for the resistor, we can electrically control the gain of the amplifier. This principle is employed for automatic gain control (AGC) in radio receivers. AGC is particularly important for maintaining a nearly constant sound level in mobile situations, because the strength of a signal varies markedly as a vehicle moves about.

Now consider what happens if we continue to increase v_{DS} . Because of the current flow, the voltages between points along the channel and the source become greater as we move toward the drain. Thus, the voltage between gate and channel becomes smaller as we move toward the drain, resulting in a tapering of the channel thickness as illustrated in Figure 5.5. Because of the tapering of the channel, its resistance becomes larger with increasing v_{DS} , resulting in a lower rate of increase of i_D .

In the triode region, the NMOS device behaves as a resistor connected between drain and source, but the resistance decreases as v_{GS} increases.

For $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$, we say that the device is operating in the triode region, and the drain current is given by

$$i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] \quad (5.2)$$

Key equation for enhancement NMOS in the triode region.

in which

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} \quad (5.3)$$

As illustrated in Figure 5.1, W is the width of the channel and L is its length. The device parameter is

$$KP = \mu_n C_{ox} \quad (5.4)$$

A typical value of KP for n -channel enhancement devices is $50 \mu\text{A}/\text{V}^2$.

in which μ_n is the surface mobility of the electrons in the channel and C_{ox} is the capacitance of the gate per unit area. C_{ox} , in turn, depends on the oxide thickness t_{ox} . A typical value of KP for n -channel enhancement devices is $50 \mu\text{A}/\text{V}^2$.

Usually, μ_n and C_{ox} are determined by the fabrication process. However, in designing a circuit, we can vary the ratio W/L to obtain transistors best suited to various parts of the circuit.

Operation in the Saturation Region

We have seen that as v_{DS} is increased, the voltage between the gate and the drain end of the channel decreases. When the gate-to-drain voltage v_{GD} equals the threshold voltage V_{to} , the channel thickness at the drain end becomes zero. For further increases in v_{DS} , i_D is constant, as shown in Figure 5.5. This is called the **saturation region**, in which we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ and the current is given by

$$i_D = K(v_{GS} - V_{to})^2 \quad (5.5)$$

Key equation for enhancement NMOS in the saturation region.

Figure 5.6 shows the drain characteristics of an NMOS transistor.

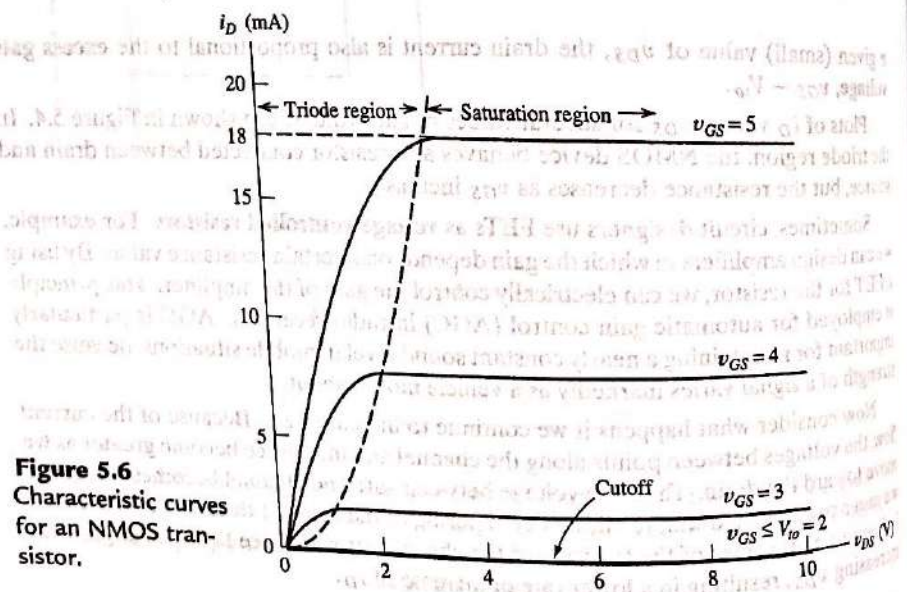


Figure 5.6 Characteristic curves for an NMOS transistor.

Boundary Between the Triode and Saturation Regions

Next, we derive the equation for the boundary between the triode region and the saturation region in the i_D - v_{DS} plane. This boundary exists when the channel thickness at the drain reaches zero, which occurs when $v_{GD} = V_{to}$. Thus, we want to find i_D in terms of v_{DS} under the condition that $v_{GD} = V_{to}$. Since $v_{GD} = v_{GS} - v_{DS}$, the condition at the boundary is

$$v_{GS} - v_{DS} = V_{to} \quad (5.6)$$

Solving this equation for v_{GS} , substituting the result into Equation (5.5), and reducing, we have the desired boundary equation:

$$i_D = K v_{DS}^2 \quad (5.7)$$

Key equation for boundary between triode and saturation regions.

Notice that the boundary between the triode region and the saturation region is a parabola.

Solving Equation (5.6) for v_{GS} and substituting into Equation (5.2) also produces Equation (5.7). [Equations (5.2) and (5.5) give the same values for i_D on the boundary.]

Given the values for KP , L , W , and V_{to} , we can plot the static characteristics of an NMOS transistor.

Example 5.1 Plotting the Characteristics of an NMOS Transistor

A certain enhancement-mode NMOS transistor has $W = 160 \mu\text{m}$, $L = 2 \mu\text{m}$, $KP = 50 \mu\text{A}/\text{V}^2$, and $V_{to} = 2 \text{ V}$. Plot the drain characteristic curves to scale for $v_{GS} = 0, 1, 2, 3, 4$, and 5 V .

SOLUTION First, we use Equation (5.3) to compute the device constant:

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} = 2 \text{ mA}/\text{V}^2$$

Equation (5.7) gives the boundary between the triode region and the saturation region. Thus, we have

$$i_D = K v_{DS}^2 = 2 v_{DS}^2$$

where i_D is in mA and v_{DS} is in volts. The plot of this equation is the dashed line shown in Figure 5.6.

Next, we use Equation (5.5) to compute the drain current in the saturation region for each of the v_{GS} values of interest. We obtain

$$i_D = K(v_{GS} - V_{to})^2 = 2(v_{GS} - 2)^2$$

where, again, the current is in mA. Substituting values, we have

$$i_D = 18 \text{ mA for } v_{GS} = 5 \text{ V}$$

$$i_D = 8 \text{ mA for } v_{GS} = 4 \text{ V}$$

$$i_D = 2 \text{ mA for } v_{GS} = 3 \text{ V}$$

and

$$i_D = 0 \text{ mA for } v_{GS} = 2 \text{ V}$$

For $v_{GS} = 0$ and 1 V, the device is in cutoff and $i_D = 0$. The preceding values are plotted in the saturation region as shown in Figure 5.6.

Finally, Equation (5.2) is used to plot the characteristics in the triode region. For each value of v_{GS} , this equation plots as a parabola that passes through the origin ($i_D = 0$ and $v_{DS} = 0$). The apex of each parabola is on the boundary between the triode region and the saturation region.

Channel-Length Modulation

So far, we have indicated that the drain current i_D is independent of v_{DS} in the saturation region. This is approximately true for devices having longer channel lengths (say, $L = 10 \mu\text{m}$ and up). If we look closely at the operation of the device, we find that the channel length becomes shorter as v_{DS} increases. This is due to the fact that the depletion region surrounding the drain becomes thicker with increasing reverse bias. With long channels, the change in length is relatively insignificant. However, in the case of shorter channel lengths, the effect can be important.

The effect of channel-length modulation can be accounted for in the equations for the drain current by including the factor $(1 + \lambda v_{DS})$, in which λ is called the **channel-length modulation parameter**. For typical devices, it has a value of approximately

$$\lambda \cong \frac{0.1}{L} \text{ V}^{-1} \quad (5.8)$$

with L in μm .

Next, we give the NMOS transistor equations, taking channel-length modulation into account. In cutoff ($v_{GS} \leq V_{to}$)

$$i_D = 0 \quad (5.9)$$

In the triode region ($v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$)

$$i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] (1 + \lambda v_{DS}) \quad (5.10)$$

In the saturation region ($v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$)

$$i_D = K (v_{GS} - V_{to})^2 (1 + \lambda v_{DS}) \quad (5.11)$$

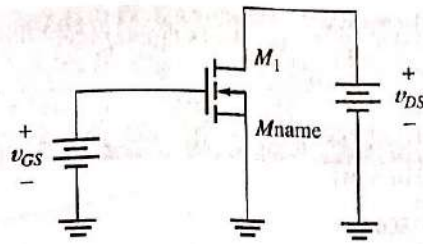
We can use SPICE to obtain plots of the characteristic curves for an NMOS transistor having given parameters.

Example 5.2 Using SPICE to Plot Drain Characteristics

Use SPICE to obtain a plot of the drain characteristics of a transistor having $W = 160 \mu\text{m}$, $L = 2 \mu\text{m}$, $KP = 50 \mu\text{A/V}^2$, $\lambda = 0.05$, and $V_{to} = 2 \text{ V}$. Plot the drain characteristic curves to scale for $v_{GS} = 0, 1, 2, 3, 4$, and 5 V .

NMOS transistor equations taking channel-length modulation into account.

Figure 5.7
This circuit
can be used
to plot drain
characteris-
tics.



SOLUTION First, we start Schematics and draw the circuit illustrated in Figure 5.7. Initially, we used the breakout part **MbreakN3** for the NMOS transistor. To specify the model parameters, we first click on the NMOS symbol (it turns red), and then we use the **edit/model/edit instance model** command to bring up the window shown in Figure 5.8 and enter the model name (we used Mname) and the parameters shown, after which we click on OK. Then we double click on the NMOS symbol to bring up the window displayed in Figure 5.9, in which we enter the length and width values and click again on OK.

Next, we return to the main Schematics window and use the **analysis/setup/dc sweep** command to bring up the **DC Sweep** window shown in Figure 5.10a. We choose v_{DS} as the main sweep variable and set up for a sweep from 0 to 10 V, in 0.1 V increments. Then we click on the **Nested Sweep** button to bring up the **DC Nested Sweep** window illustrated in Figure 5.10b, where we choose v_{GS} as the variable and set up for a start value of 0, an end value of 5 V, and an increment of 1 V. Be sure to click on Enable Nested Sweep; a check will appear in the adjacent box.

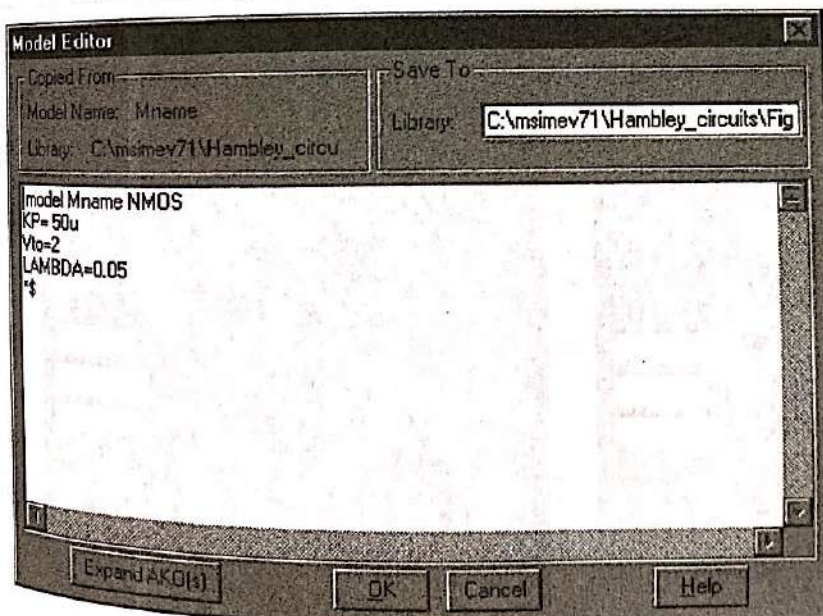
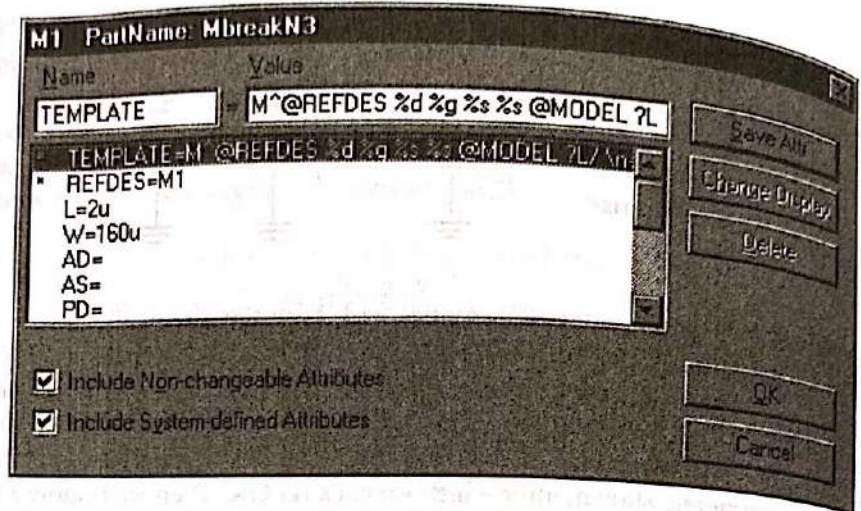


Figure 5.8 Model-editor window.

Figure 5.9 Attribute window for M_1 .

Then we use the **analysis/simulate** command to start the simulation, after which Probe starts and displays the characteristics shown in Figure 5.11. (We have attached a current marker to the drain of the NMOS to allow Probe to automatically plot the drain current after the simulation is finished.) The upward slope of the characteristics is due to the nonzero value of λ . Compare these characteristics to those of Figure 5.6, which are plots for the same parameters, except that $\lambda = 0$.

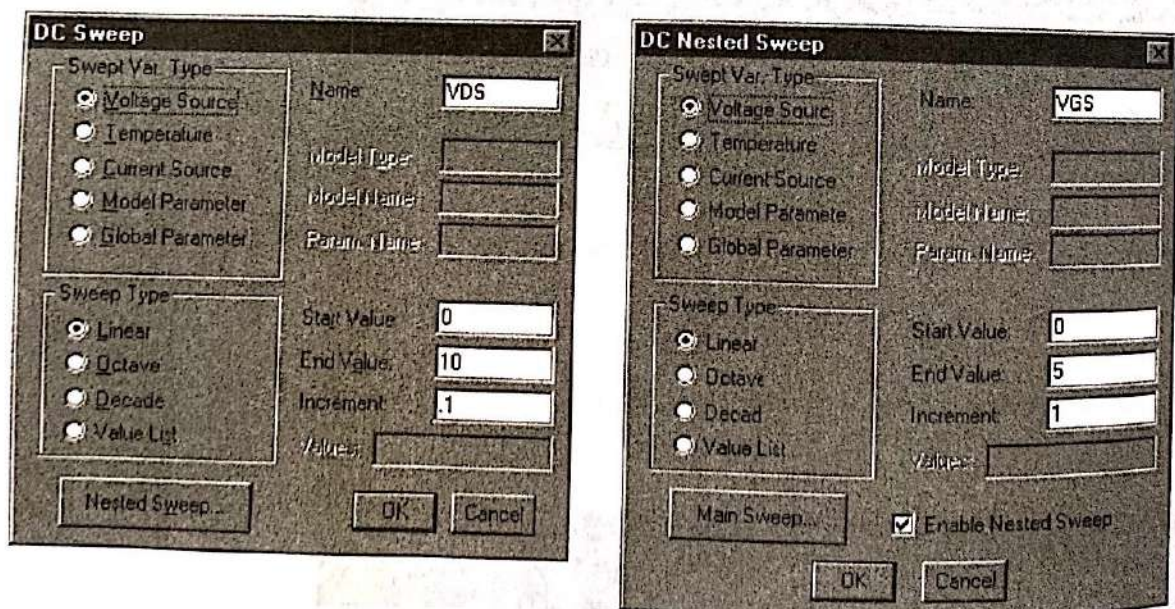


Figure 5.10 Dc-sweep setup windows.

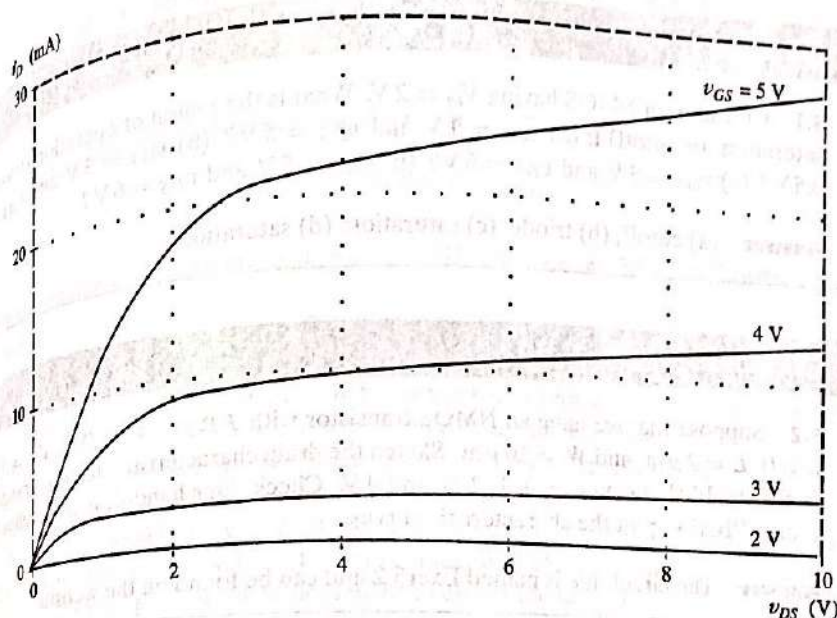


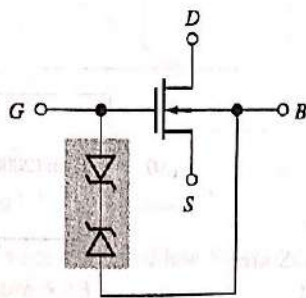
Figure 5.11 Drain characteristics for Example 5.2.

Gate Protection

Because of their construction, MOSFETs have extremely high input impedances between gate and channel—in excess of $1000\text{ M}\Omega$. In handling these devices, it is easy to develop static electric voltages greater than the breakdown voltage of the gate insulation. The breakdown of the insulating layer is destructive, usually resulting in a short circuit between gate and channel.

To alleviate this problem, the gate terminals can be protected by back-to-back Zener diodes as illustrated in Figure 5.12. If the device is exposed to a static electric charge, the Zener diodes break down, providing a nondestructive discharge path. The diodes are fabricated on the same chip as the FET. Often in ICs, gate protection takes the form of diodes connected from the input terminals to the power supply and ground terminals. (In normal operation, these diodes are reverse biased.) Protection diodes are not needed for devices internal to ICs that do not have direct external connections.

Figure 5.12
Diodes protect
the oxide layer
from destruction
by static electric
charge.



Section summary: In an NMOS transistor, when a sufficiently large (positive) voltage is applied to the gate relative to the source, electrons are attracted to the region under the gate, and a channel of n -type material is induced between the drain and the source. Then, if voltage is applied between the drain and the source, current flows into the drain, through the channel, and out of the source. Drain current is controlled by the voltage applied to the gate.

EXERCISE

5.1 Consider an NMOS having $V_{to} = 2$ V. What is the region of operation (triode, saturation, or cutoff) if (a) $v_{GS} = 1$ V and $v_{DS} = 5$ V? (b) $v_{GS} = 3$ V and $v_{DS} = 0.5$ V? (c) $v_{GS} = 3$ V and $v_{DS} = 6$ V? (d) $v_{GS} = 5$ V and $v_{DS} = 6$ V?

Answer (a) cutoff; (b) triode; (c) saturation; (d) saturation.

EXERCISE

5.2 Suppose that we have an NMOS transistor with $KP = 50 \mu\text{A}/\text{V}^2$, $V_{to} = 1$ V, $\lambda = 0$, $L = 2 \mu\text{m}$, and $W = 10 \mu\text{m}$. Sketch the drain characteristics for v_{DS} , ranging from 0 to 10 V and $v_{GS} = 0, 1, 2, 3$, and 4 V. Check your hand-drawn sketches by using SPICE to plot the characteristic curves.

Answer The circuit file is named Exer5.2 and can be found on the website.

5.2 LOAD-LINE ANALYSIS OF A SIMPLE NMOS AMPLIFIER

... the input voltage $v_{in}(t)$ causes v_{GS} to vary with time, which in turn causes i_D to vary. The changing voltage drop across R_D causes an amplified version of the signal to appear at the drain terminal.

In this section, we analyze the NMOS amplifier circuit shown in Figure 5.13 by using the graphical load-line approach. The dc sources bias the MOSFET at a suitable operating point so that amplification of the input signal $v_{in}(t)$ can take place. We will see that the input voltage $v_{in}(t)$ causes v_{GS} to vary with time, which in turn causes i_D to vary. The changing voltage drop across R_D causes an amplified version of the signal to appear at the drain terminal.

Applying Kirchhoff's voltage law to the input loop, we obtain the following expression:

$$v_{GS}(t) = v_{in}(t) + V_{GG} \quad (5.12)$$

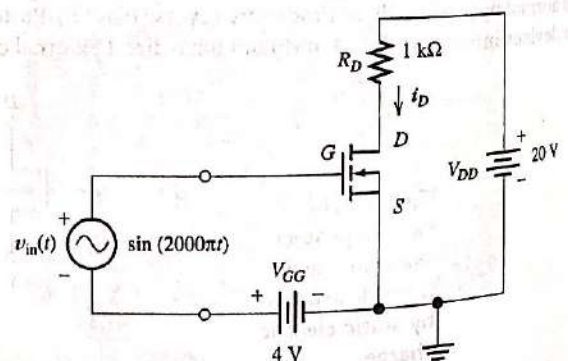


Figure 5.13
Simple NMOS amplifier circuit.

As an example, we assume that the input signal is a 1-V peak, 1-kHz sinusoid and that V_{GG} is 4 V. Then we have

$$v_{GS}(t) = \sin(2000\pi t) + 4 \quad (5.13)$$

Writing a voltage equation around the drain circuit, we obtain

$$V_{DD} = R_D i_D(t) + v_{DS}(t) \quad (5.14) \quad \text{Load-line equation.}$$

For our example, we assume that $R_D = 1 \text{ k}\Omega$ and $V_{DD} = 20 \text{ V}$, so Equation (5.14) becomes

$$20 = i_D(t) + v_{DS}(t) \quad (5.15)$$

where we have assumed that $i_D(t)$ is in milliamperes. A plot of this equation on the drain characteristics of the transistor is a straight line called the **load line**.

To establish the load line, we first locate two points on it. Assuming that $i_D = 0$ in Equation (5.15), we find that $v_{DS} = 20 \text{ V}$. These values plot as the lower right-hand end of the load line shown in Figure 5.14. For a second point, we assume that $v_{DS} = 0$, which yields $i_D = 20 \text{ mA}$ when substituted into Equation (5.15). This pair of values ($v_{DS} = 0$ and $i_D = 20 \text{ mA}$) plots as the upper left-hand end of the load line.

The operating point of an amplifier for a zero input signal is called the **quiescent operating point**, or **Q-point**. For $v_{in}(t) = 0$, Equation (5.12) yields $v_{GS} = V_{GG} = 4 \text{ V}$. Therefore, the intersection of the curve for $v_{GS} = 4 \text{ V}$ with the load line is the Q-point. The quiescent values are $I_{DQ} = 9 \text{ mA}$ and $V_{DSQ} = 11 \text{ V}$.

The maximum and minimum values of the gate-to-source voltage are $V_{GS\text{max}} = 5 \text{ V}$ and $V_{GS\text{min}} = 3 \text{ V}$. [See Equation (5.13).] In Figure 5.14, the intersections of the corresponding curves with the load line are labeled as points A and B, respectively. At

To establish the load line, we first locate two points on it.

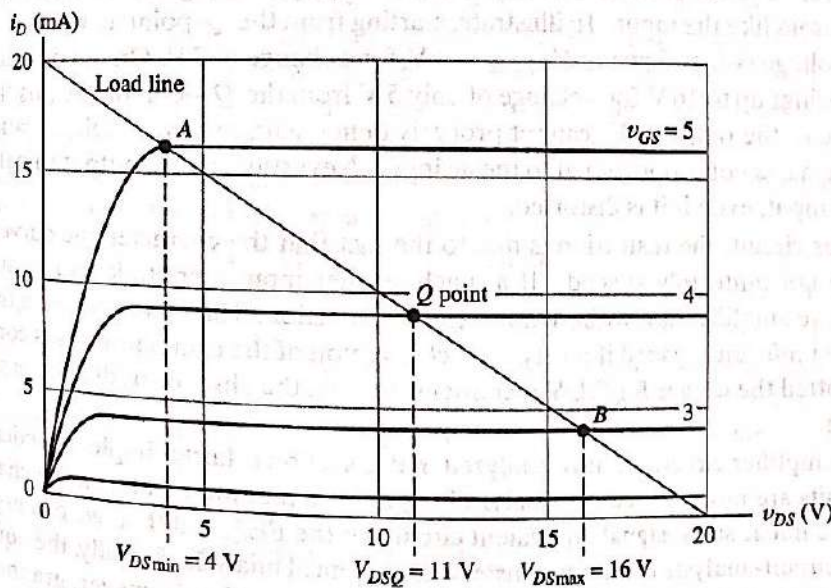


Figure 5.14 Drain characteristics and load line for the circuit of Figure 5.13.

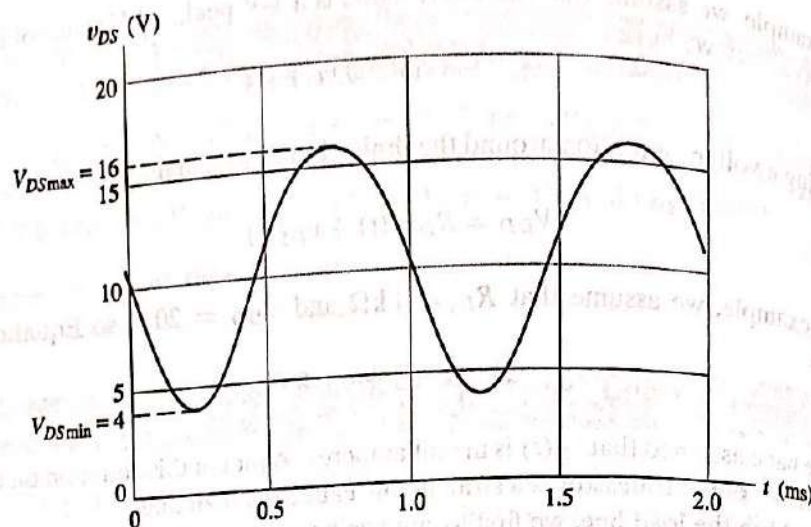


Figure 5.15 v_{DS} versus time for the circuit of Figure 5.13.

point A, we find that $V_{DS\min} = 4\text{ V}$ and $I_{D\max} = 16\text{ mA}$. At point B, we find that $V_{DS\max} = 16\text{ V}$ and $I_{D\min} = 4\text{ mA}$.

A plot of $v_{DS}(t)$ versus time is shown in Figure 5.15. Notice that the peak-to-peak swing is 12 V, whereas the peak-to-peak swing of the input signal is 2 V. Furthermore, compared to the input signal, the ac voltage at the drain is inverted. (In other words, the positive peak of the input occurs at the same time as the minimum value of v_{DS} .) Therefore, the circuit is an inverting amplifier. Apparently, the circuit has a voltage gain $A_v = -12\text{ V}/2\text{ V} = -6$, where the minus sign is due to the inversion.

Notice, however, that the output waveform displayed in Figure 5.15 is not a symmetrical sinusoid like the input. To illustrate, starting from the Q-point at $V_{DSQ} = 11\text{ V}$, the output voltage swings down to $V_{DS\min} = 4\text{ V}$, for a change of 7 V. On the other hand, the output swings up to 16 V for a change of only 5 V from the Q-point on the positive-going half cycle of the output. We cannot properly define gain for the circuit, because the ac output signal is not proportional to the ac input. Nevertheless, the output signal is larger than the input, even if it is distorted.

... distortion is due to the fact that the characteristic curves for the FET are not uniformly spaced. If a much smaller input amplitude were applied, we would have amplification without appreciable distortion.

In this circuit, the distortion is due to the fact that the characteristic curves for the FET are not uniformly spaced. If a much smaller input amplitude were applied, we would have amplification without appreciable distortion. This is true because the curves are more uniformly spaced if a very restricted region of the characteristics is considered. If we plotted the curves for 0.1-V increments in v_{GS} , the absence of distortion would be apparent.

The amplifier circuit we have analyzed in this section is fairly simple. Practical amplifier circuits are more difficult to analyze by graphical methods. Later in the chapter, we develop a linear small-signal equivalent circuit for the FET, and then we can use mathematical circuit-analysis techniques instead of graphical analysis. Usually, the equivalent-circuit approach is more useful for practical amplifier circuits. However, graphical analysis of simple circuits provides an excellent way to understand the basic concepts of amplifiers.

A DesignLab schematic of this circuit is found on the website in the file named Fig5_13. Use DesignLab to look at the various waveforms and become familiar with the operation of the circuit. You can learn much about electronics by using SPICE to play with circuits.

You can learn much about electronics by using SPICE to lay with circuits.

EXERCISE

5.3 Find V_{DSQ} , $V_{DS\min}$, and $V_{DS\max}$ for the circuit of Figure 5.13 if the circuit values are changed to $V_{DD} = 15\text{ V}$, $V_{GG} = 3\text{ V}$, $R_D = 1\text{ k}\Omega$, and $v_{in}(t) = \sin(2000\pi t)$. The characteristics for the MOSFET are shown in Figure 5.14. Check your answers by using a SPICE simulation. The parameters of the NMOS transistor are $KP = 50\text{ }\mu\text{A/V}^2$, $V_{to} = 1\text{ V}$, $\lambda = 0$, $L = 10\text{ }\mu\text{m}$, and $W = 400\text{ }\mu\text{m}$.

Answer $V_{DSQ} \cong 11\text{ V}$, $V_{DS\min} \cong 6\text{ V}$, $V_{DS\max} \cong 14\text{ V}$. The circuit is stored in the file named Exer5_3, which can be found on the website.

5.3 BIAS CIRCUITS

The analysis of amplifier circuits is often undertaken in two steps. First, we analyze the dc circuit to determine the Q -point. In this analysis, the nonlinear device equations or the characteristic curves are used. Then, after the bias analysis is completed, we use a linear small-signal equivalent circuit to find the input resistance, voltage gain, and so on.

In integrated multistage amplifiers, the bias points of the various devices are interdependent. On the other hand, in discrete circuits, capacitors can be used to couple the stages, and the bias point for each stage can be established independently of the other stages. In this section, we consider the analysis and design of dc bias circuits suitable for RC-coupled discrete FET amplifiers, mainly to give you a better understanding of MOSFETs, biasing, and related concepts. The bias circuits discussed in the section are also applicable to JFETs. Later in the book, we will consider the more difficult problems associated with bias design for integrated circuits.

The two-battery bias circuit used in the amplifier of Figure 5.13 is not practical. Usually, only one dc voltage is readily available instead of two. However, a more significant problem is that FET parameters vary considerably from device to device. In general, we want to establish a Q -point near the middle of the load line, so that the output signal can swing in both directions without clipping. When the FET parameters vary from unit to unit, the two-battery circuit can wind up with some circuits biased near one end or the other.

The Fixed- Plus Self-Bias Circuit

The fixed- plus self-bias circuit illustrated in Figure 5.16a is a good discrete circuit for establishing Q -points that are relatively independent of device parameters.

Amplifier analysis has two steps: 1. Determine the Q -point. 2. Use a small-signal equivalent circuit to find impedances and gains.

In integrated multistage amplifiers, the bias points of the various devices are interdependent. On the other hand, in discrete circuits, capacitors can be used to couple the stages, and the bias point for each stage can be established independently of the other stages.

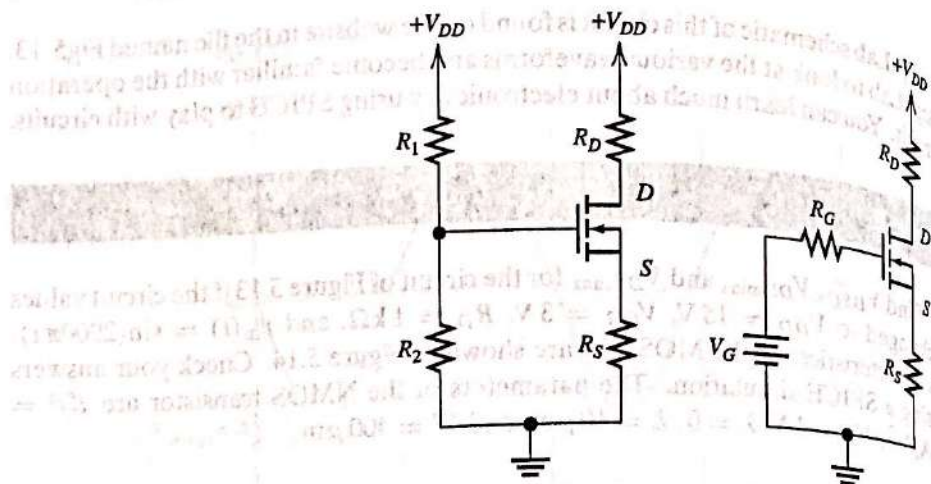


Figure 5.16
Fixed-bias plus self-bias
circuit.

(a) Original circuit

(b) Gate bias circuit
replaced by its
Thévenin equivalent

For purposes of analysis, we replace the gate circuit with its Thévenin equivalent, as shown in Figure 5.16b. The Thévenin voltage is

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} \quad (5.16)$$

and the Thévenin resistance R_G is the parallel combination of R_1 and R_2 . Writing a voltage equation around the gate loop of Figure 5.16b, we obtain

$$V_G = v_{GS} + R_S i_D \quad (5.17)$$

(We have assumed that the voltage drop across R_G is zero, because the gate current of an NMOS transistor is extremely small.)

Usually, we want to bias the transistor in its saturation region, so we have

$$i_D = K(v_{GS} - V_{to})^2 \quad (5.18)$$

(To simplify bias-point analysis, we assume that $\lambda = 0$.)

The simultaneous solution of Equations (5.17) and (5.18) yields the operating point (provided that it falls in the saturation region). Plots of these two equations are illustrated in Figure 5.17. Equation (5.17) plots as a straight line called the **bias line**. Notice that two roots will be found, because Equation (5.18) plots as the dashed curve for $v_{GS} < V_{to}$. Thus, the smaller root found for v_{GS} is extraneous and should be discarded. The larger root found for v_{GS} and the smaller root for i_D is the true operating point.

Finally, we can find v_{DS} by writing a voltage equation around the drain loop of Figure 5.16:

$$v_{DS} = V_{DD} - (R_D + R_S)i_D \quad (5.19)$$

The simultaneous solution of Equations (5.17) and (5.18) yields the operating point (provided that it falls in the saturation region). The larger root found for v_{GS} and the smaller root for i_D is the true operating point.

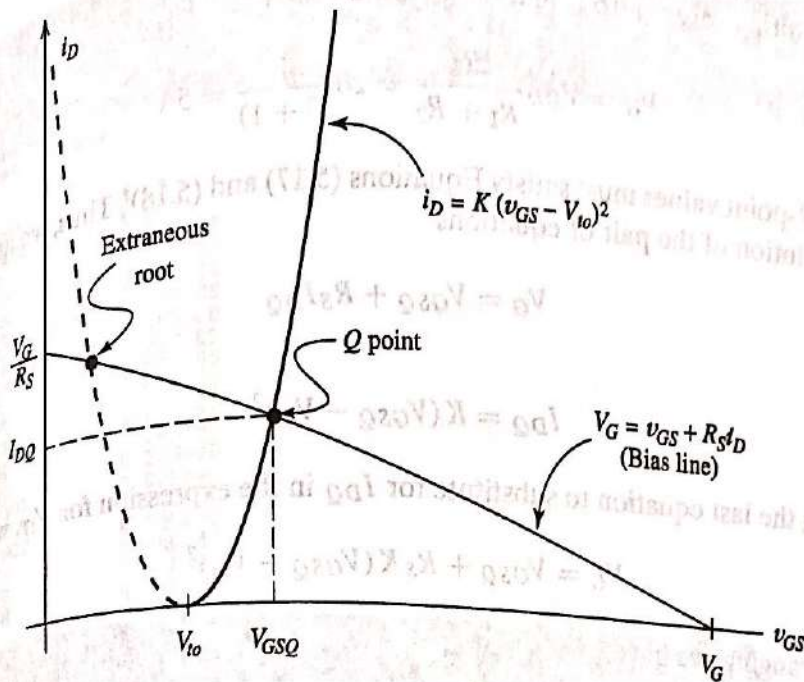


Figure 5.17 Graphical solution of Equations (5.17) and (5.18).

Example 5.3 Determination of Q-Point for the Fixed- Plus Self-Bias Circuit

Analyze the fixed- plus self-bias circuit shown in Figure 5.18. The transistor has $K_P = 50 \mu\text{A}/\text{V}^2$, $V_{to} = 2 \text{ V}$, $\lambda = 0$, $L = 10 \mu\text{m}$, and $W = 400 \mu\text{m}$. Check your results by using SPICE.

SOLUTION First, we use Equation (5.3) to compute the device constant:

$$K = \left(\frac{W}{L}\right) \frac{K_P}{2} = 1 \text{ mA}/\text{V}^2$$

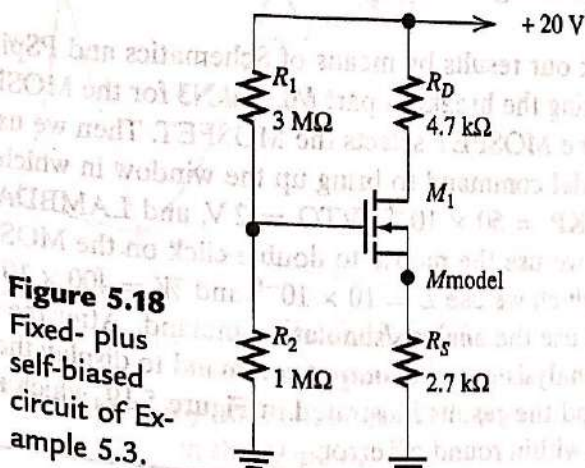


Figure 5.18
Fixed- plus
self-biased
circuit of Ex-
ample 5.3.

Substituting values into Equation (5.16), we have

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 20 \frac{1}{(3 + 1)} = 5 \text{ V}$$

The Q -point values must satisfy Equations (5.17) and (5.18). Thus, we need to find the solution of the pair of equations

$$V_G = V_{GSQ} + R_S I_{DQ}$$

and

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

Using the last equation to substitute for I_{DQ} in the expression for V_G , we obtain

$$V_G = V_{GSQ} + R_S K(V_{GSQ} - V_{to})^2$$

Rearranging, we have

$$V_{GSQ}^2 + \left(\frac{1}{R_S K} - 2V_{to} \right) V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_S K} = 0$$

After the values are substituted, we get

$$V_{GSQ}^2 - 3.630 V_{GSQ} + 2.148 = 0$$

Solving, we find that $V_{GSQ} = 2.886$ and $V_{GSQ} = 0.744$. The second root is extraneous and should be discarded. Then we have

$$I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.784 \text{ mA}$$

Solving for the drain-to-source voltage yields

$$V_{DSQ} = V_{DD} - (R_D + R_S)I_{DQ} = 14.2 \text{ V}$$

which is high enough to ensure that operation is in saturation, as assumed in the solution.

To check our results by means of Schematics and PSpice, first we draw the circuit, utilizing the breakout part **MbreakN3** for the MOSFET. Using the mouse to click on the MOSFET selects the MOSFET. Then we use the **edit/model/edit instance model** command to bring up the window in which we enter the device parameters $K_P = 50 \times 10^{-6}$, $V_{TO} = 2 \text{ V}$, and $LAMBDA = 0$. Returning to Schematics, we use the mouse to double click on the MOSFET to bring up the window in which we use $L = 10 \times 10^{-6}$ and $W = 400 \times 10^{-6}$.

Then we use the **analysis/simulate** command. After the simulation is finished, we use the **analysis/examine output** command to display the output file. Scrolling down, we find the results illustrated in Figure 5.19, which agree with our hand calculations within round off error.

The simulation is stored in Fig5.18.

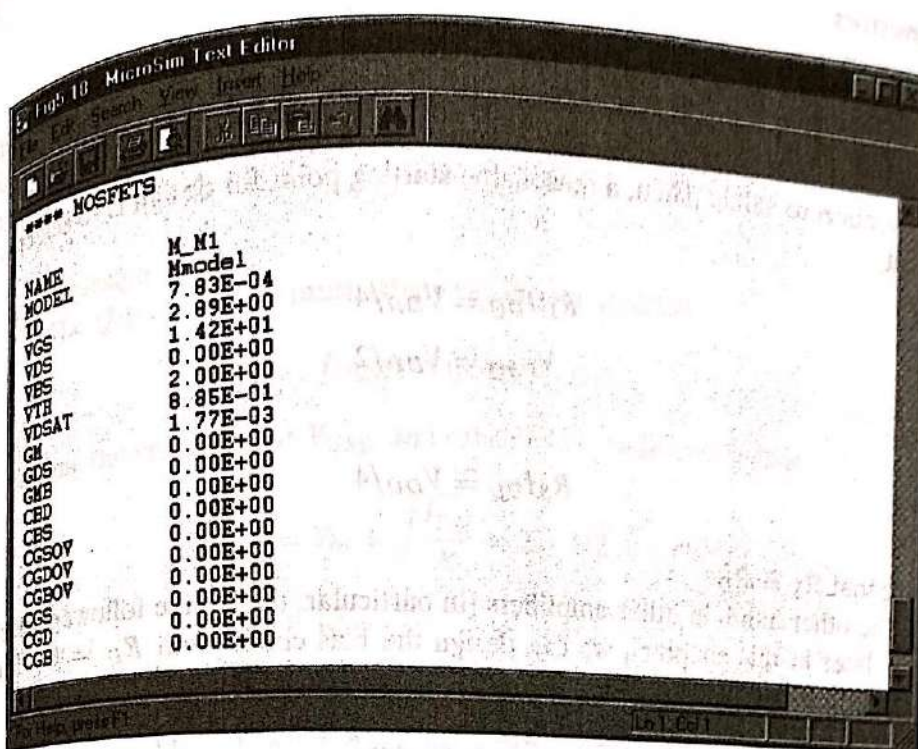


Figure 5.19 Part of the output file for the SPICE simulation of the circuit of Figure 5.18.

Design of the Fixed- Plus Self-Bias Circuit

Figure 5.20 shows graphical solutions of Equations (5.17) and (5.18) for several transistors with different values of V_{to} and K . Notice that a higher value of V_G (i.e., V_{G2}) results in less variation in I_{DQ} between the high-current device and the low-current device, because the bias line becomes closer to horizontal. However, we cannot choose V_G too high, because this raises the voltage drop across R_S , and sufficient voltage must be allocated for V_{DSQ} and the drop across R_D .

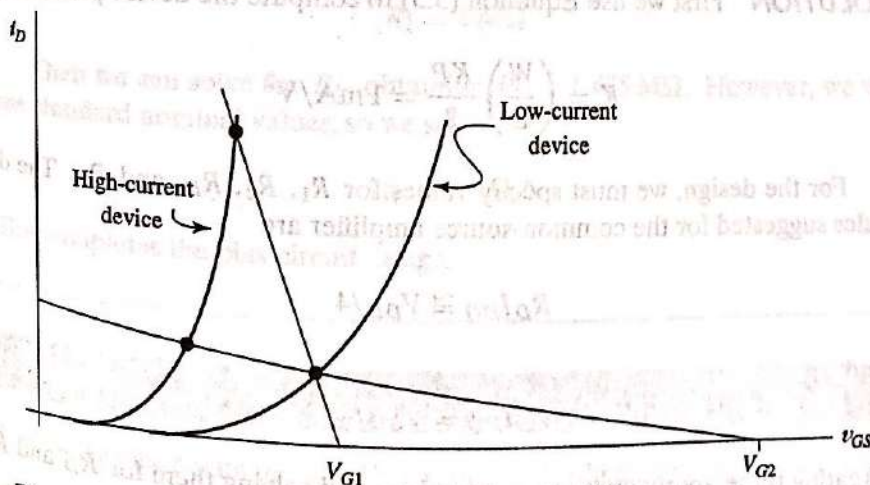


Figure 5.20 The more nearly horizontal bias line results in less change in the Q -point.

The selection of the Q -point and the design of the bias circuit depend on the intended ac operation of the circuit. Later, we will see that in some amplifiers (for example, the common-source configuration) the output signal appears at the drain, and R_D must assume a nonzero value. Then, a reasonable starting point for design is to select values such that

Design rules for the NMOS bias circuit if R_D must assume a nonzero value.

$$R_D I_{DQ} \cong V_{DD}/4$$

$$V_{DSQ} \cong V_{DD}/2$$

and

$$R_S I_{DQ} \cong V_{DD}/4$$

implying that $R_S \cong R_D$.

On the other hand, in other amplifiers (in particular, the source follower, which we consider later in this chapter), we can design the bias circuit with $R_D = 0$. Then, a reasonable starting point for design is to select values such that

Design rules for the NMOS bias circuit if $R_D = 0$.

$$V_{DSQ} \cong V_{DD}/2$$

and

$$R_S I_{DQ} \cong V_{DD}/2$$

Example 5.4 NMOS Bias-Circuit Design

Design a fixed- plus self-bias circuit for a common-source NMOS amplifier. Nominally, the transistor has $KP = 50 \mu\text{A}/\text{V}^2$, $W = 80 \mu\text{m}$, $L = 2 \mu\text{m}$, $\lambda = 0$, and $V_{to} = 2 \text{ V}$. The circuit is to have $V_{DD} = 20 \text{ V}$ and $I_{DQ} \cong 2 \text{ mA}$.

SOLUTION First we use Equation (5.3) to compute the device parameter:

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} = 1 \text{ mA}/\text{V}^2$$

For the design, we must specify values for R_1 , R_2 , R_D , and R_S . The design rules suggested for the common-source amplifier are

$$R_D I_{DQ} \cong V_{DD}/4$$

and

$$R_S I_{DQ} \cong V_{DD}/4$$

Treating these approximations as equations and solving them for R_D and R_S , we find that

$$R_D = R_S = \frac{V_{DD}}{4I_{DQ}} = \frac{20 \text{ V}}{4 \times 2 \text{ mA}} = 2.5 \text{ k}\Omega$$

In a discrete design, we need to select standard nominal values for the resistors. Usually, 5%-tolerance resistors are suitable for bias circuits. Thus, we choose

$$R_D = R_S = 2.4 \text{ k}\Omega$$

in this design.

The Q -point values must satisfy the device equation

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

Solving the equation for V_{GSQ} and substituting values, we obtain

$$V_{GSQ} = V_{to} + \sqrt{\frac{I_{DQ}}{K}} = 2 + \sqrt{2} = 3.414 \text{ V}$$

($V_{GSQ} = V_{to} - \sqrt{I_{DQ}/K}$ is an extraneous root.) Equation (5.17) must be satisfied by the Q -point values, so we have

$$V_G = V_{GSQ} + R_S I_{DQ} = 3.414 + 2.4(2) = 8.214 \text{ V}$$

Substituting values into Equation (5.16), we get

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2}$$

so that

$$8.214 = 20 \frac{R_2}{R_1 + R_2}$$

We now choose either R_1 or R_2 . Usually, we want to use large values for these resistors to keep the current taken from the power supply small. Arbitrarily, we choose

$$R_2 = 1 \text{ M}\Omega$$

Then we can solve for R_1 , obtaining $R_1 = 1.435 \text{ M}\Omega$. However, we want to use standard nominal values, so we select

$$R_1 = 1.5 \text{ M}\Omega$$

This completes the bias-circuit design. $\square$

EXERCISE

5.4 Analyze the circuit designed in Example 5.4. Check your results by using SPICE.

Answer $I_{DQ} = 1.92 \text{ mA}$, $V_{GSQ} = 3.39 \text{ V}$, $V_{DSQ} = 10.8 \text{ V}$. The circuit schematic is stored in the file named Exer5.4.

EXERCISE

5.5 Design a fixed- plus self-bias circuit for an NMOS source follower. Nominally, the transistor has $KP = 50 \mu\text{A}/\text{V}^2$, $W = 100 \mu\text{m}$, $L = 2 \mu\text{m}$, $\lambda = 0$, and $V_{to} = 1\text{V}$. The circuit is to have $V_{DD} = 15\text{V}$ and $I_{DQ} \cong 2\text{mA}$. Use SPICE to check that your design provides a Q -point close to the desired value.

Answer We should choose $R_D = 0$ for a source follower. Many values will work for the other resistors. A reasonable set of values is $R_S = 3.9\text{k}\Omega$, $R_1 = 1\text{M}\Omega$, and $R_2 = 2\text{M}\Omega$. These values yield $I_{DQ} = 1.96\text{mA}$ and $V_{DSQ} = 7.26\text{V}$.

5.4 SMALL-SIGNAL EQUIVALENT CIRCUITS

In the preceding section, we considered discrete dc bias circuits for FET amplifiers. Now we consider the relationships between signal currents and voltages resulting in small changes from the Q -point. As usual, we denote total quantities by lowercase letters with uppercase subscripts, such as $i_D(t)$ and $v_{GS}(t)$. The dc Q -point values are denoted by uppercase letters with an additional Q subscript, such as I_{DQ} and V_{GSQ} . The signals are denoted by lowercase letters with lowercase subscripts, such as $i_d(t)$ and $v_{gs}(t)$. The total current or voltage is the sum of the Q -point value and the signal. Thus, we can write

$$i_D(t) = I_{DQ} + i_d(t) \quad (5.20)$$

and

$$v_{GS}(t) = V_{GSQ} + v_{gs}(t) \quad (5.21)$$

Figure 5.21 illustrates the terms in Equation (5.20).

In the following discussion, we assume that the FETs are biased in the saturation region, which is usually the case for amplifier circuits. Equation (5.5), repeated here for convenience, gives the total drain current in terms of the total gate-to-source voltage:

$$i_D = K(v_{GS} - V_{to})^2$$

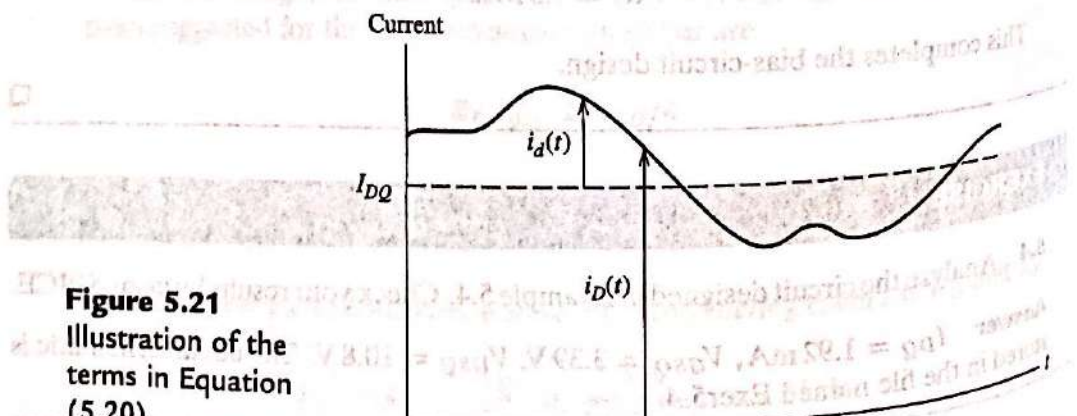


Figure 5.21
Illustration of the
terms in Equation
(5.20).

Using Equations (5.20) and (5.21) to substitute into Equation (5.5), we obtain

$$I_{DQ} + i_d(t) = K [V_{GSQ} + v_{gs}(t) - V_{to}]^2 \quad (5.22)$$

The right-hand side of Equation (5.22) can be expanded to get

$$I_{DQ} + i_d(t) = K(V_{GSQ} - V_{to})^2 + 2K(V_{GSQ} - V_{to})v_{gs}(t) + Kv_{gs}^2(t) \quad (5.23)$$

However, the Q -point values are also related by Equation (5.5), so that we have

$$I_{DQ} = K(V_{GSQ} - V_{to})^2 \quad (5.24)$$

Therefore, the first term on each side of Equation (5.23) can be canceled. Furthermore, we are interested in small-signal conditions for which the last term on the right-hand side of Equation (5.23) is negligible and can be dropped [i.e., we assume that $|v_{gs}(t)|$ is much smaller than $|V_{GSQ} - V_{to}|$]. With these changes, Equation (5.23) becomes

$$i_d(t) = 2K(V_{GSQ} - V_{to})v_{gs}(t) \quad (5.25)$$

If we define the **transconductance** of the FET as

$$g_m = 2K(V_{GSQ} - V_{to}) \quad (5.26)$$

Equation (5.25) can be written as

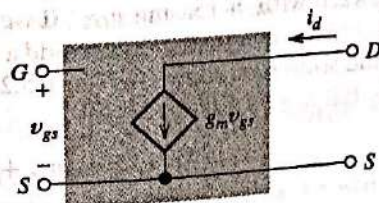
$$i_d(t) = g_mv_{gs}(t) \quad (5.27)$$

The gate current for the FET is negligible, so that we have

$$i_g(t) = 0 \quad (5.28)$$

Equations (5.27) and (5.28) can be represented by the **small-signal equivalent circuit** illustrated in Figure 5.22. Thus, for small signals, the FET is modeled by a voltage-controlled current source connected between the drain and source terminals. The model has an open circuit between gate and source.

Figure 5.22
Small-signal equivalent circuit for FETs.



Thus, for small signals, the FET is modeled by a voltage-controlled current source connected between the drain and source terminals. The model has an open circuit between gate and source.

Dependence of Transconductance on Q -Point and Device Parameters

We will see that the transconductance g_m is an important parameter in the design of amplifier circuits. In general, better performance is obtained with higher values of g_m . Thus, designers need to know how Q -point and device parameters influence transconductance. Solving Equation (5.24) for the quantity $(V_{GSQ} - V_{to})$ and substituting the results into Equation (5.26), we obtain

$$g_m = 2\sqrt{K I_{DQ}} \quad (5.29)$$

Key equation.

We can increase g_m by choosing a higher value of I_{DQ} .

An important point to notice is that g_m is proportional to the square root of the Q -point drain current. Accordingly, we can increase g_m by choosing a higher value of I_{DQ} . If we use Equation (5.3) to substitute for K in Equation (5.29), we obtain

$$g_m = \sqrt{2KP} \sqrt{W/L} \sqrt{I_{DQ}} \quad (5.30)$$

Then, by using Equation (5.4) to substitute for KP , we have

$$g_m = \sqrt{2\mu_n C_{ox}} \sqrt{W/L} \sqrt{I_{DQ}} \quad (5.31)$$

... we can obtain higher values of g_m for a given value of I_{DQ} by increasing the width-to-length ratio of the MOSFET.

High transconductance is obtained at the cost of chip area.

Thus, we can obtain higher values of g_m for a given value of I_{DQ} by increasing the width-to-length ratio of the MOSFET. Because process limitations place a minimum value on L , high g_m implies large values for W . High transconductance is obtained at the cost of chip area.

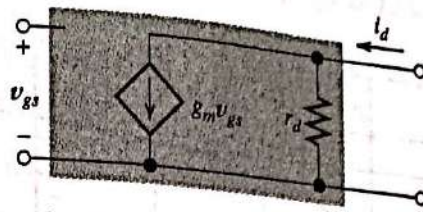
More Complex Equivalent Circuits

Sometimes, additions to the equivalent circuit are needed to accurately model FETs. For example, we will need to include small capacitances between the device terminals when we consider the high-frequency response of FET amplifiers. The device equations and the equivalent circuit that we have derived from them describe only the static behavior of the device. For an accurate model with rapidly changing currents and voltages, capacitances are required.

Furthermore, the first-order equations we have used to obtain the equivalent circuit for the FET did not account for the small effect of v_{DS} on the drain current, because we assumed that $\lambda = 0$. In other words, we assumed that the drain characteristics are horizontal in the saturation region, but this is not exactly true—the drain characteristics slope slightly upward with increasing v_{DS} . If we wish to account for the effect of v_{DS} in the small-signal equivalent circuit, we must add a resistance r_d , called the **drain resistance**, between drain and source, as shown in Figure 5.23. In this case, Equation (5.27) becomes

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d} \quad (5.32)$$

Figure 5.23
FET small-signal equivalent circuit that accounts for the dependence of i_D on v_{DS} .



Transconductance and Drain Resistance as Partial Derivatives

An alternative definition of g_m can be found by examining Equation (5.32). Notice that if $v_{ds} = 0$, g_m is the ratio of i_d to v_{gs} . Mathematically, we obtain

$$g_m = \left. \frac{i_d}{v_{gs}} \right|_{v_{ds}=0} \quad (5.33)$$

However, i_d , v_{gs} , and v_{ds} represent small changes from the Q -point. Therefore, the condition $v_{ds} = 0$ is equivalent to requiring v_{DS} to remain constant at the Q -point value, namely, V_{DSQ} . Thus, we can write

$$g_m \cong \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_{v_{DS}=V_{DSQ}} \quad (5.34)$$

where Δi_D is an increment of drain current, centered at the Q -point. Similarly, Δv_{GS} is an increment of gate-to-source voltage, centered at the Q -point.

Equation (5.34) is an approximation to a partial derivative. Therefore, g_m is the partial derivative of i_D with respect to v_{GS} , evaluated at the Q -point:

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{Q\text{-point}} \quad (5.35)$$

Similarly, the reciprocal of the drain resistance is

$$\frac{1}{r_d} \cong \left. \frac{\Delta i_D}{\Delta v_{DS}} \right|_{v_{GS}=V_{GSQ}} \quad (5.36)$$

Hence, we can write

$$\frac{1}{r_d} = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{Q\text{-point}} \quad (5.37)$$

Given the drain characteristics, we can determine approximate values of the partial derivatives for a specific Q -point. Then we can model the FET by its small-signal equivalent in the analysis of an amplifier circuit and use the values found for g_m and r_d to compute amplifier gains and impedances. In the next several sections, we present examples of this process. First, we show how to determine the values of g_m and r_d , starting from the characteristic curves.

Example 5.5 Determination of g_m and r_d from the Characteristic Curves

Determine the values of g_m and r_d for the MOSFET having the characteristics illustrated in Figure 5.24 at a Q -point defined by $V_{GSQ} = 3.5$ and $V_{DSQ} = 10$ V.

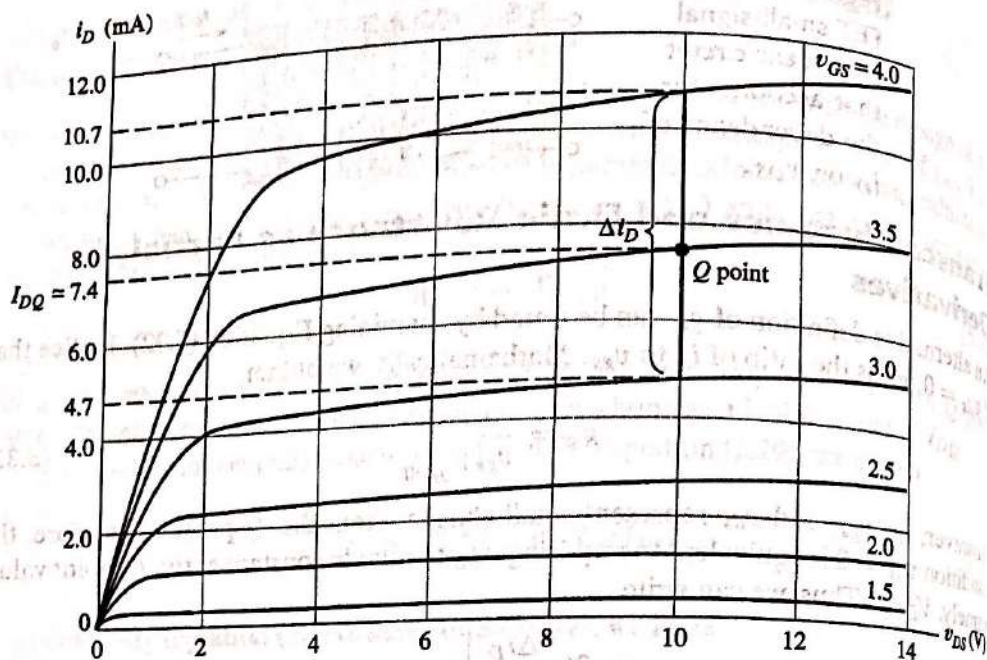


Figure 5.24 Determination of g_m and r_d . See Example 5.5.

SOLUTION First, we locate the Q -point as shown in the figure. Then we use Equation (5.34) to find g_m :

$$g_m = \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_{v_{DS}=V_{DSQ}=10 \text{ V}}$$

We must make changes around the Q -point, while holding v_{DS} constant at 10 V. Thus, the incremental changes are made along a vertical line through the Q -point. To obtain a representative value for g_m , we consider an increment centered on the Q -point (rather than making the changes in one direction from the Q -point). Taking the changes starting from the curve below the Q -point and ending at the curve above the Q -point, we have $\Delta i_D \cong 10.7 - 4.7 = 6 \text{ mA}$ and $\Delta v_{GS} = 1 \text{ V}$. This increment is labeled in the figure. Thus, we have

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} = \frac{6 \text{ mA}}{1 \text{ V}} = 6 \text{ mS}$$

The drain resistance is found by applying Equation (5.36):

$$\frac{1}{r_d} = \left. \frac{\Delta i_D}{\Delta v_{DS}} \right|_{v_{GS}=V_{GSQ}}$$

Because the incremental changes are to be made while holding v_{GS} constant, the changes are made along the characteristic curve through the Q -point. Therefore, $1/r_d$ is the slope of the curve through the Q -point. For $v_{GS} = V_{GSQ} = 3.5 \text{ V}$, we

obtain $i_D \cong 6.7 \text{ mA}$ at $v_{DS} = 4 \text{ V}$ and $i_D \cong 8.0 \text{ mA}$ at $v_{DS} = 14 \text{ V}$. Accordingly, we obtain

$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}} \cong \frac{(8.0 - 6.7) \text{ mA}}{(14 - 4) \text{ V}} = 0.13 \times 10^{-3} \text{ S}$$

Taking the reciprocal, we find that $r_d = 7.7 \text{ k}\Omega$. □

EXERCISE

5.6 Find the values of g_m and r_d for the characteristics of Figure 5.24 at a Q -point of $V_{GSQ} = 2.5 \text{ V}$ and $V_{DSQ} = 6 \text{ V}$.

Answer $g_m \cong 3.3 \text{ mS}$ and $r_d \cong 20 \text{ k}\Omega$.

EXERCISE

5.7 Show that Equation (5.26) results from applying Equation (5.35) to Equation (5.5).

5.5 THE COMMON-SOURCE AMPLIFIER

The circuit diagram of a **common-source amplifier** is shown in Figure 5.25. The ac signal to be amplified is $v(t)$. The coupling capacitors C_1 and C_2 , as well as the bypass capacitor C_s , are intended to have very small impedances for the ac signal. In this section, we carry

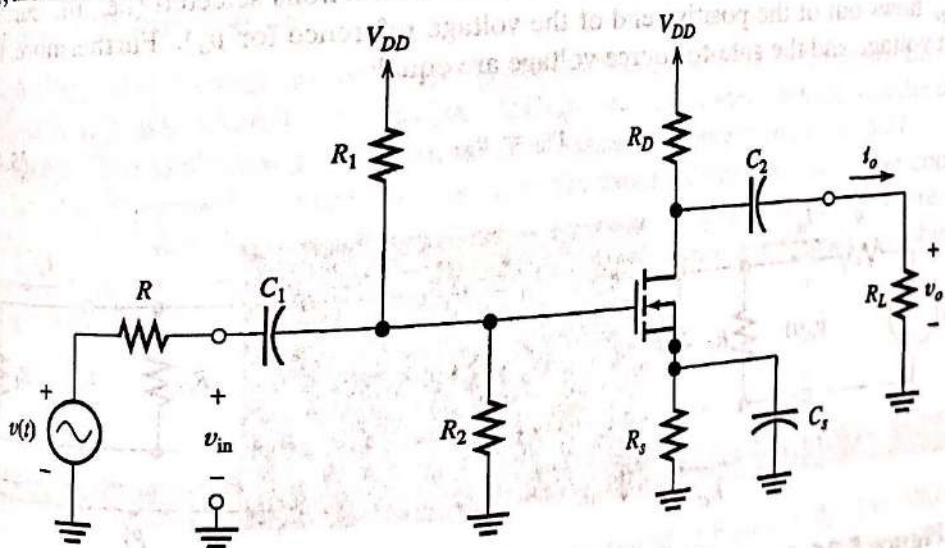


Figure 5.25 Common-source amplifier.

out a midband analysis in which we assume that these capacitors are short circuits for the signal. Later, when we consider the frequency response of amplifiers, we include the capacitors. The resistors R_1 , R_2 , R_S , and R_D form the bias network, and their values are selected to obtain a suitable Q -point. The amplified output signal is applied to the load R_L .

The Small-Signal Equivalent Circuit

The small-signal equivalent circuit for the amplifier is illustrated in Figure 5.26. The input coupling capacitor C_1 has been replaced by a short circuit. The MOSFET has been replaced by its small-signal equivalent. Because the bypass capacitor C_S is assumed to be a short circuit, the source terminal of the FET is connected directly to ground—which is why the circuit is called a *common-source amplifier*.

The dc supply voltage source acts as a short circuit for the ac signal.

The dc supply voltage source acts as a short circuit for the ac signal. (Even if ac current flows through the dc source, the ac voltage across it is zero. Thus, for ac signals, the dc voltage source is a short.) Consequently, both R_1 and R_2 are connected from gate to ground in the equivalent circuit. Similarly, R_D is connected from drain to ground.

Voltage Gain

Next, we derive an expression for the voltage gain of the common-source amplifier. Referring to the small-signal equivalent circuit, we notice that the resistances r_d , R_D , and R_L are in parallel. We denote the equivalent resistance by

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} \quad (5.38)$$

The output voltage is the product of the current from the controlled source and the equivalent resistance:

$$v_o = -(g_m v_{gs}) R'_L \quad (5.39)$$

The minus sign is needed because of the reference directions selected (i.e., the current $g_m v_{gs}$ flows out of the positive end of the voltage reference for v_o). Furthermore, the input voltage and the gate-to-source voltage are equal:

$$v_{in} = v_{gs} \quad (5.40)$$

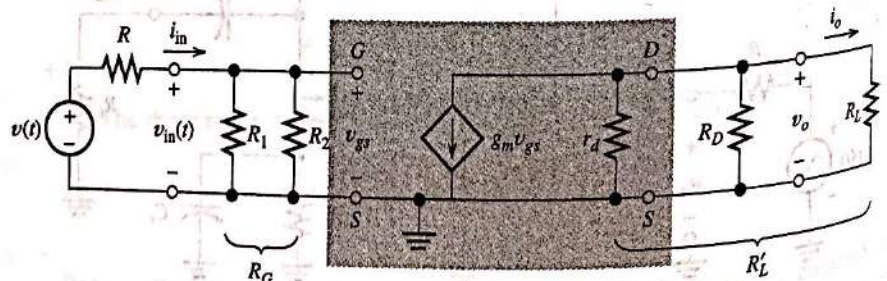


Figure 5.26 Small-signal equivalent circuit for the common-source amplifier.

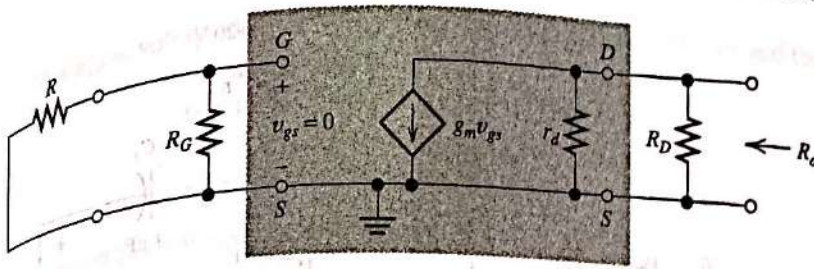


Figure 5.27 Circuit used to find R_o .

Now, if we divide the respective sides of Equation (5.39) by those of Equation (5.40), we obtain the voltage gain:

$$A_v = \frac{v_o}{v_{in}} = -g_m R'_L \quad (5.41)$$

The minus sign in the expression for the voltage gain shows that the common-source amplifier is inverting. Notice that the voltage gain is proportional to g_m .

Input Resistance

The input resistance of the common-source amplifier is given by

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2 \quad (5.42)$$

The resistances R_1 and R_2 form part of the bias network, but their values are not critical. (See Section 5.3 for a discussion of the bias circuit.) Practical values range up to perhaps 10 M Ω in circuits with discrete components. Thus, we have a great deal of freedom in designing the input resistance of a common-source amplifier. This is not true for BJT amplifier circuits.

Output Resistance

To find the output resistance of an amplifier, we disconnect the load, replace the signal source by its internal resistance, and then find the resistance seen looking into the output terminals. The equivalent circuit with these changes is displayed in Figure 5.27.

Because there is no source connected to the input side of the circuit, we conclude that $v_{gs} = 0$. Therefore, the controlled current source $g_m v_{gs}$ produces zero current and appears as an open circuit. Consequently, the output resistance is the parallel combination of R_D and r_d :

$$R_o = \frac{1}{1/R_D + 1/r_d} \quad (5.43)$$

In the small-signal midband analysis of FET amplifiers, the coupling capacitors, bypass capacitors, and dc voltage sources are replaced by short circuits. The FET is replaced with its small-signal equivalent circuit. Then we write circuit equations and derive useful expressions for gains, input impedance, and output impedance.

... we have a great deal of freedom in designing the input resistance of a common-source amplifier. This is not true for BJT amplifier circuits.

To find the output resistance of an amplifier, we disconnect the load, replace the signal source by its internal resistance, and then find the resistance seen looking into the output terminals.

Example 5.6 Gain and Impedance of a Common-Source Amplifier

Consider the common-source amplifier illustrated in Figure 5.28. The NMOS transistor has $K_P = 50 \mu\text{A}/\text{V}^2$, $V_{to} = 2 \text{ V}$, $\lambda = 0$, $L = 10 \mu\text{m}$, and $W = 400 \mu\text{m}$.

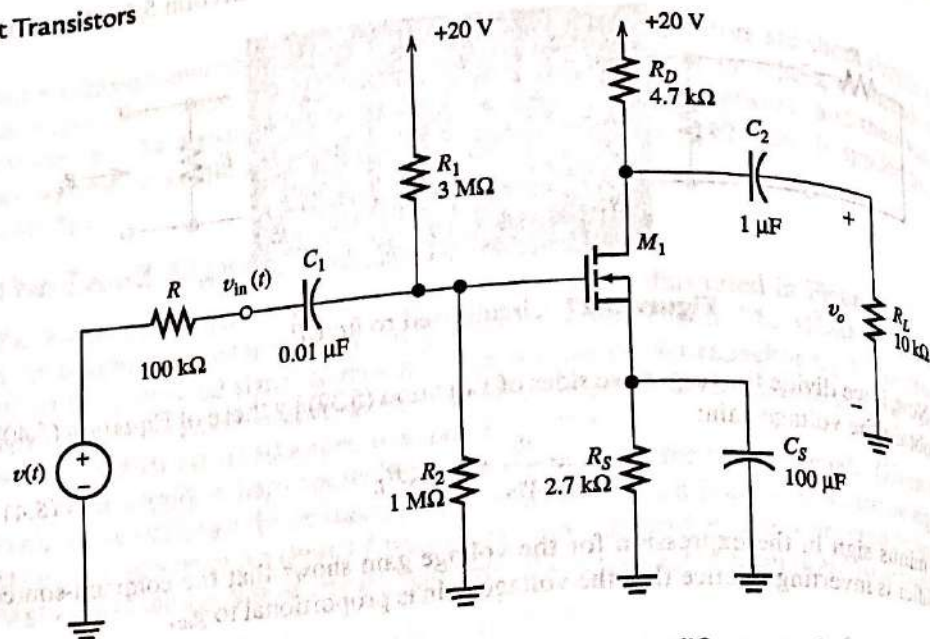


Figure 5.28 Common-source amplifier.

Find the midband voltage gain, input resistance, and output resistance of the amplifier. Then, if the input source is given by

$$v(t) = 100 \sin(2000\pi t) \text{ mV}$$

compute the output voltage. Assume that the frequency of the source (which is 1000 Hz) is in the midband region.

SOLUTION First, we need to find the Q -point so that we can determine the value of g_m for the MOSFET. The bias circuit consists of R_1 , R_2 , R_D , R_S , and the MOSFET. This circuit was analyzed in Example 5.3, where we determined that $I_{DQ} = 0.784 \text{ mA}$.

Next, we use Equation (5.30) to find the transconductance of the device:

$$g_m = \sqrt{2KP} \sqrt{W/L} \sqrt{I_{DQ}} = 1.77 \text{ mS}$$

Because we have $\lambda = 0$, the drain characteristics are horizontal in the saturation region, and $r_d = \infty$.

Now we use Equations (5.38), (5.41), (5.42), and (5.43) to find

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = 3197 \Omega$$

$$A_v = \frac{v_o}{v_{in}} = -g_m R'_L = -5.66$$

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2 = 750 \text{ k}\Omega$$

and

$$R_o = \frac{1}{1/R_D + 1/r_d} = 4.7 \text{ k}\Omega$$

The signal voltage divides between the internal source resistance and the input resistance of the amplifier. Thus, we have

$$v_{in} = v(t) \frac{R_{in}}{R + R_{in}} = 88.23 \sin(2000\pi t) \text{ mV}$$

Then the output voltage can be found as

$$v_o(t) = A_v v_{in}(t) = -500 \sin(2000\pi t) \text{ mV}$$

Notice the phase inversion of $v_o(t)$ compared with $v_{in}(t)$.

□

Example 5.7 SPICE Analysis of a Common-Source Amplifier

Perform a transient analysis with PSpice to verify the result found for the output voltage in Example 5.6. Also, use an ac sweep to obtain a plot of the voltage-gain magnitude versus frequency to verify that 1000 Hz is in the midband region.

SOLUTION First we use Schematics to draw the circuit as shown in Figure 5.28. Next, we double click on the input source to bring up the window illustrated in Figure 5.29. For the ac analysis, we specify a source amplitude of AC = 100 mV. For the transient analysis, we enter the parameters VOFF = 0, VAMPL = 100 mV, and FREQ = 1000.

We set up the MOSFET parameters exactly as we did in Example 5.3. Then we use the **analysis/setup/ac sweep** command to bring up the window displayed in Figure 5.30a, in which we enter the parameters shown. Next, we use the **analysis/setup/transient** command to bring up the window shown in Figure 5.30b, in which we entered the parameters for the transient analysis.

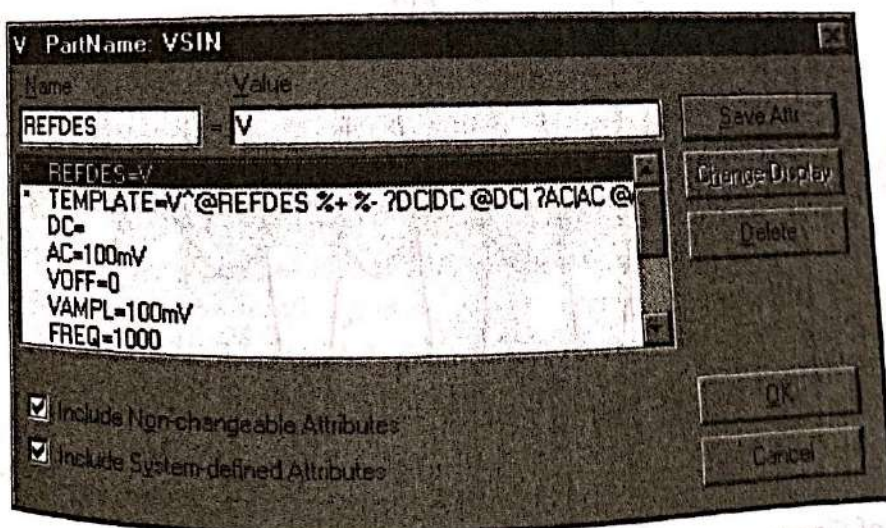


Figure 5.29 Setup window for the signal source.

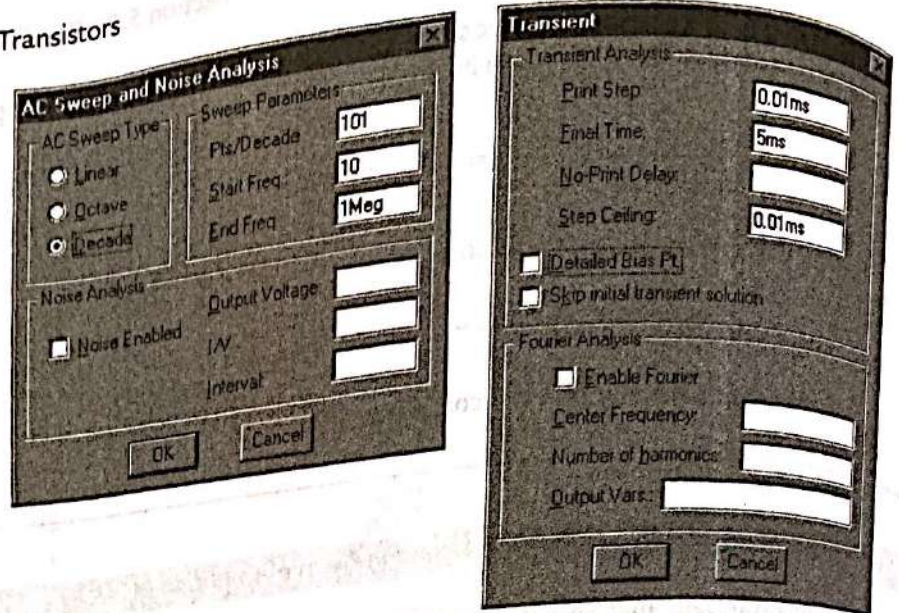


Figure 5.30 Analysis setup windows.

Now we use the **analysis/simulate** command to start the simulation, after which Probe starts. First, we look at the results of the transient analysis, which are shown in Figure 5.31. As expected, the output voltage is a 500-mV peak sine wave that is inverted compared with the input signal.

Next, we use the **plot/ac** command in Probe to look at the ac sweep results. The gain magnitude $|V_{out}/V_{in}|$ is illustrated in Figure 5.32. We see that the gain magnitude is nearly constant upward from about 100 Hz. Thus, 1000 Hz is indeed in the midband range. Below 100 Hz, the gain magnitude declines because of

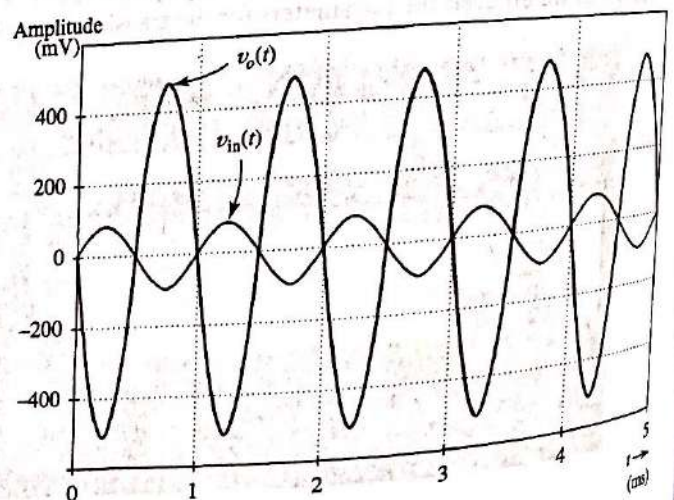


Figure 5.31 $v_o(t)$ and $v_{in}(t)$ versus time for the common-source amplifier of Figure 5.28.

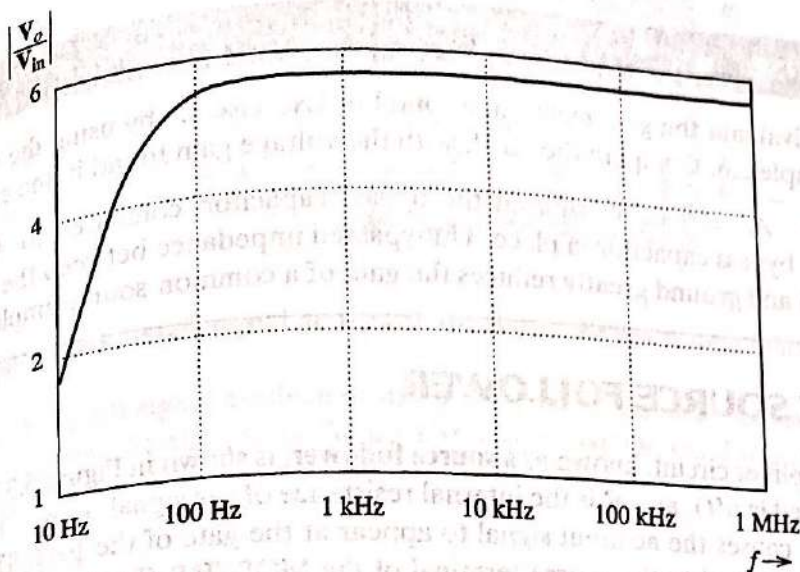


Figure 5.32 Gain magnitude versus frequency for the common-source amplifier of Figure 5.28.

the coupling and bypass capacitors. (We will consider the frequency response of amplifiers and how to choose the capacitor values later.)

EXERCISE

5.8 Find the voltage gain of the amplifier of Example 5.6 if R_L is replaced by an open circuit.

Answer $A_{vo} = -8.32$.

EXERCISE

5.9 Consider the circuit of Figure 5.25 with the bypass capacitor C_S replaced by an open circuit. Draw the small-signal equivalent circuit. Then, assuming, for simplicity, that r_d is an open circuit, derive an expression for the voltage gain in terms of g_m and the resistances.

Answer

$$A_v = \frac{-g_m R'_L}{1 + g_m R_S}$$

EXERCISE

5.10 Evaluate the gain expression found in Exercise 5.9 by using the values given in Example 5.6. Compare the result with the voltage gain found in the example.

Answer $A_v = -0.849$ without the bypass capacitor, compared to $A_v = -5.66$ with the bypass capacitor in place. Unbypassed impedance between the FET source terminal and ground greatly reduces the gain of a common-source amplifier.

Unbypassed impedance between the FET source terminal and ground greatly reduces the gain of a common-source amplifier.

5.6 THE SOURCE FOLLOWER

Another amplifier circuit, known as a **source follower**, is shown in Figure 5.33. The signal to be amplified is $v(t)$, and R is the internal resistance of the signal source. The coupling capacitor C_1 causes the ac input signal to appear at the gate of the FET. The capacitor C_2 connects the load to the source terminal of the MOSFET. (In the midband analysis of the amplifier, we assume that the coupling capacitors behave as short circuits.) The resistors R_S , R_1 , and R_2 form the bias circuit.

The Small-Signal Equivalent Circuit

The small-signal equivalent circuit is shown in Figure 5.34. The coupling capacitors have been replaced by short circuits, and the FET has been replaced by its small-signal equivalent. Notice that the drain terminal is connected directly to ground, because the dc supply becomes a short in the small-signal equivalent. Here, the FET equivalent circuit is drawn in a different configuration (i.e., with the drain at the bottom) from that illustrated earlier, but it is the same electrically.

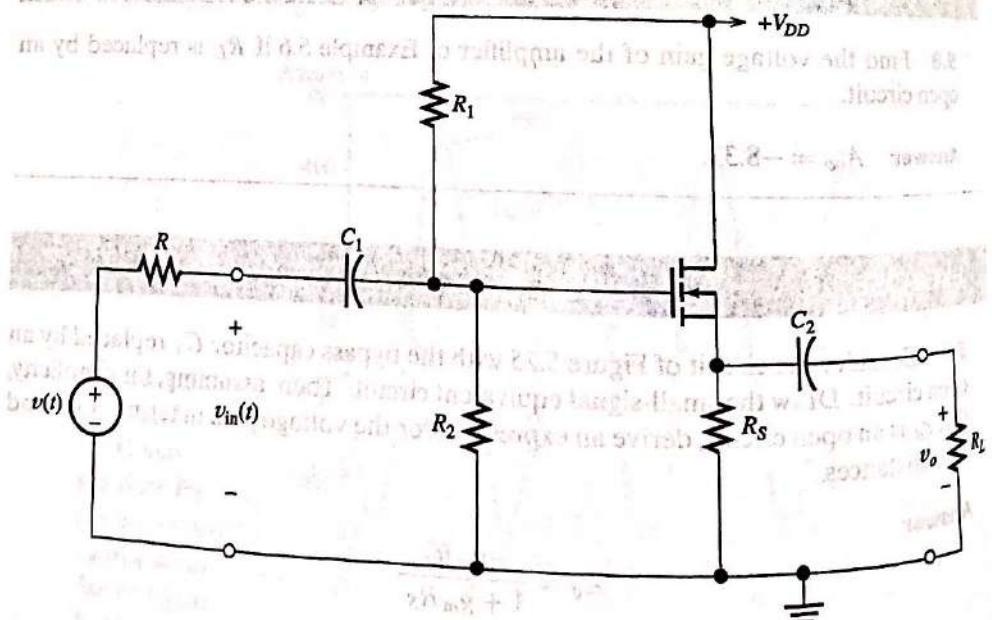


Figure 5.33 Source follower.

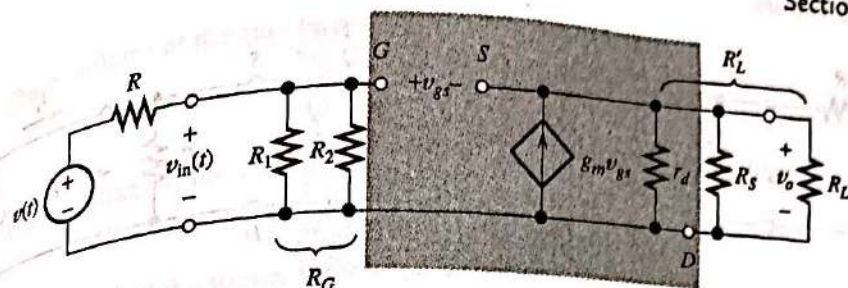


Figure 5.34 Small-signal ac equivalent circuit for the source follower.

Drawing the small-signal equivalent of an amplifier circuit is an important skill for electronics engineers. Starting from Figure 5.33, test yourself to see if you can obtain the small-signal circuit.

Voltage Gain

We now derive an expression for the voltage gain of the source follower. Notice that r_d , R_S , and R_L are in parallel. We denote the parallel combination by

$$R'_L = \frac{1}{1/r_d + 1/R_S + 1/R_L} \quad (5.44)$$

The output voltage is given by

$$v_o = g_m v_{gs} R'_L \quad (5.45)$$

Furthermore, we can write the following voltage equation:

$$v_{in} = v_{gs} + v_o \quad (5.46)$$

Using Equation (5.45) to substitute for v_o in Equation (5.46), we have

$$v_{in} = v_{gs} + g_m v_{gs} R'_L \quad (5.47)$$

Dividing the respective sides of Equations (5.45) and (5.47), we obtain the following expression for the voltage gain:

$$A_v = \frac{v_o}{v_{in}} = \frac{g_m R'_L}{1 + g_m R'_L} \quad (5.48)$$

Notice that the voltage gain given in Equation (5.48) is positive and less than unity. Thus, the source follower is a noninverting amplifier with voltage gain slightly less than unity.

Input Resistance

The input resistance is the resistance seen looking into the input terminals of the equivalent circuit. Hence, we have

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G \quad (5.49)$$

Drawing the small-signal equivalent of an amplifier circuit is an important skill for electronics engineers.

... the source follower is a noninverting amplifier with voltage gain slightly less than unity.

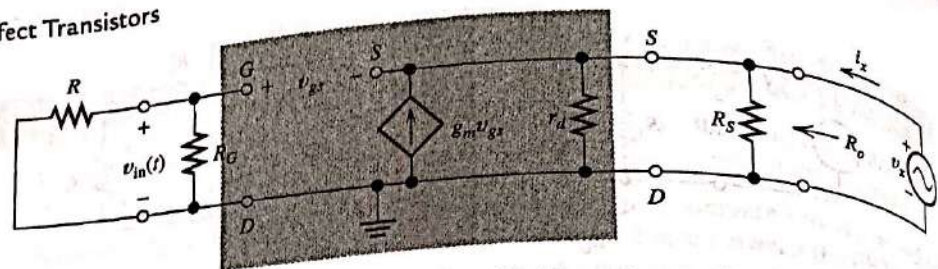


Figure 5.35 Equivalent circuit used to find the output resistance of the source follower.

Output Resistance

To find the output resistance, we remove the load resistance, replace the signal source with its internal resistance, and look back into the output terminals. It is helpful to attach a test source v_x to the output terminals as illustrated in Figure 5.35. Then the output resistance is

$$R_o = \frac{v_x}{i_x} \quad (5.50)$$

where i_x is the current supplied by the test source as shown in the figure. The output resistance is given by

$$R_o = \frac{1}{g_m + 1/R_S + 1/r_d} \quad (5.51)$$

... another reason for using a source follower is to obtain low output resistance.

This resistance can be quite low, and another reason for using a source follower is to obtain low output resistance.

Example 5.8 Gain and Impedance Calculations for a Source Follower

Consider the source follower illustrated in Figure 5.33, given that $R_L = 1\text{ k}\Omega$ and $R_1 = R_2 = 2\text{ M}\Omega$. The NMOS transistor has $KP = 50\text{ }\mu\text{A/V}^2$, $\lambda = 0$, $L = 2\text{ }\mu\text{m}$, $W = 160\text{ }\mu\text{m}$, and $V_{to} = 1\text{ V}$. Find the value required for R_S to achieve $I_{DQ} = 10\text{ mA}$. Then compute the voltage gain, input resistance, and output resistance.

SOLUTION From Equations (5.3) and (5.5), we have

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} = 2\text{ mA/V}^2$$

and

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

Solving the latter equation for V_{GSQ} and substituting values, we obtain

$$V_{GSQ} = \sqrt{I_{DQ}/K} + V_{to} = 3.236\text{ V}$$

The dc voltage at the gate terminal is given by

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2} = 7.5 \text{ V}$$

The dc voltage at the source terminal of the NMOS is

$$V_S = V_G - V_{GSQ} = 4.264 \text{ V}$$

Finally, we find the source resistance:

$$R_S = \frac{V_S}{I_{DQ}} = 426.4 \Omega$$

(Of course, in a discrete circuit, we would choose a standard nominal value for R_S . However, we will continue this example using the exact value computed for R_S .) Next, we use Equation (5.30) to find the transconductance of the device:

$$g_m = \sqrt{2KP} \sqrt{W/L} \sqrt{I_{DQ}} = 8.944 \text{ mS}$$

Because we have $\lambda = 0$, the drain characteristics are horizontal in the saturation region, and $r_d = \infty$.

Next, we substitute values into Equation (5.44):

$$R'_L = \frac{1}{1/r_d + 1/R_S + 1/R_L} = 298.9 \Omega$$

Then the voltage gain is given by Equation (5.48):

$$A_v = \frac{v_o}{v_{in}} = \frac{g_m R'_L}{1 + g_m R'_L} = 0.7272$$

The input resistance is

$$R_{in} = R_1 || R_2 = 1 \text{ M}\Omega$$

The output resistance is given by Equation (5.51):

$$R_o = \frac{1}{g_m + 1/R_S + 1/r_d} = 88.58 \Omega$$

This is a fairly low output resistance compared with that of other single-FET amplifier configurations.

The current gain can be found by the use of Equation (1.4):

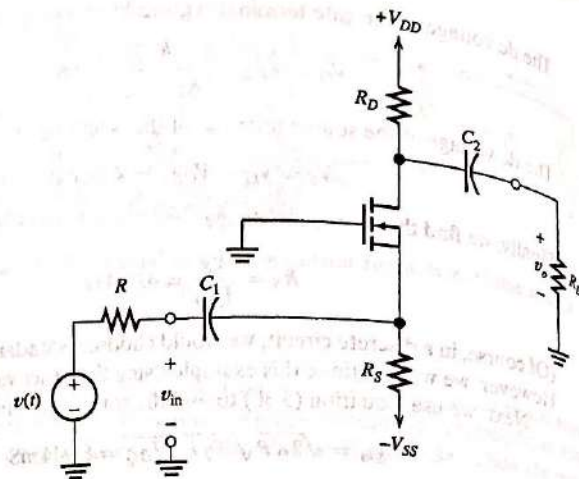
$$A_i = A_v \frac{R_{in}}{R_L} = 727.2$$

The power gain is given by

$$G = A_v A_i = 528.8$$

Even though the voltage gain is less than unity, the output power is much greater than the input power because of the high input resistance. $\square$

Figure 5.36
Common-gate amplifier.



The source follower has voltage gain slightly less than unity, high input impedance, and low output impedance. The current gain and power gain can be larger than unity.

In the preceding section and in this one, we have considered two of the most important single-stage FET amplifiers: the common-source amplifier and the source follower. Later in the book, we discuss other amplifier configurations that use FETs, multistage amplifiers, and amplifiers that use both FETs and BJTs.

EXERCISE

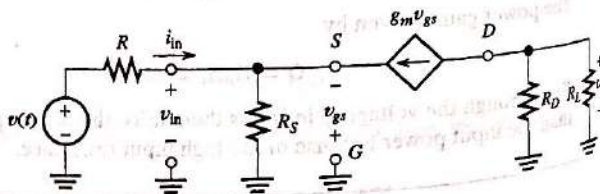
5.11 Derive Equation (5.51).

EXERCISE

5.12 Derive expressions for the voltage gain, input resistance, and output resistance of the common-gate amplifier illustrated in Figure 5.36.

Answer The small-signal equivalent circuit is shown in Figure 5.37. $A_v = g_m R'_L$ in which $R'_L = R_D || R_L$; $R_{in} = 1/(g_m + 1/R_S)$; $R_o = R_D$.

Figure 5.37
See Exercise 5.12.



5.7 JFET p-CHAN

So far, we have considered MOSFET applications.

The n-Ch

The physical structure of the n-channel MOSFET is shown in Figure 5.38. The drain and source are electrically connected to the substrate.

The physical structure of the p-channel MOSFET is shown in Figure 5.39. The drain and source are electrically connected to the substrate.

Recall from the previous chapter that the gate and channel are separated by a thin layer of oxide. This is called the gate oxide layer, and it is the cross-section of the channel, and that the cross-section of the channel is shown in Figure 5.40.

Figure 5.38
n-Ch

5.7 JFETS, DEPLETION-MODE MOSFETS, AND p -CHANNEL DEVICES

So far, we have looked at only one type of FET, namely, the n -channel enhancement-mode MOSFET. In this section, we introduce several other types of FETs and their applications.

The n -Channel Junction FET

The physical structure of an n -channel junction field-effect transistor (JFET) is illustrated in Figure 5.38a and the circuit symbol is displayed in Figure 5.38b. The device consists of a channel of n -type semiconductor, with ohmic (nonrectifying) contacts at each end, called the **drain** and the **source**. Alongside the channel are regions of p -type semiconductor electrically connected to each other and to the gate terminal.

The pn junction between the gate and the channel is a rectifying contact similar to the pn -junction diodes discussed in Chapter 3. In almost all applications, the junction between the gate and the channel is reverse biased, so virtually no current flows in the gate terminal. (Recall that, to achieve reverse bias in a pn -junction, the p -side is negative with respect to the n -side.) Hence, the gate is negative with respect to the channel in the normal operation of an n -channel JFET. (In contrast, for operation in the saturation or triode regions, the gate of an enhancement-mode NMOS is positive with respect to the channel.)

Recall from our discussion of pn -junction physics that applying reverse bias between gate and channel causes a layer of the channel next to the gate to become nonconductive. This is called the **depletion layer**. The greater the reverse bias, the thicker the depletion layer becomes. Eventually, the nonconductive layer extends all the way across the channel, and we say that **pinch-off** has occurred. This is illustrated in Figure 5.39. Notice that the cross-sectional area of the conductive path from drain to source depends on the

While MOSFETs are predominantly employed in ICs, JFETs are the FET of choice in discrete circuits.

... the gate is negative with respect to the channel in the normal operation of an n -channel JFET.

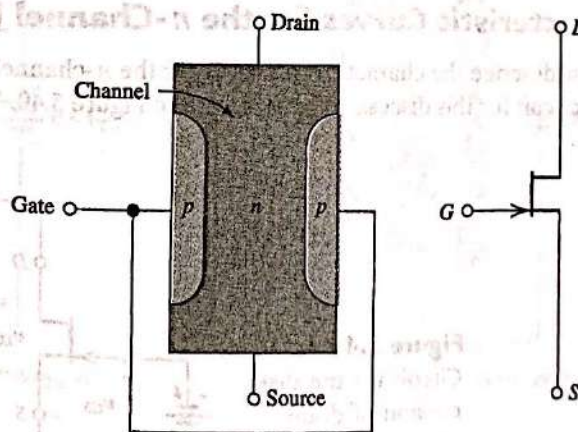


Figure 5.38
 n -Channel JFET.

(a) Simplified physical structure

(b) Circuit symbol

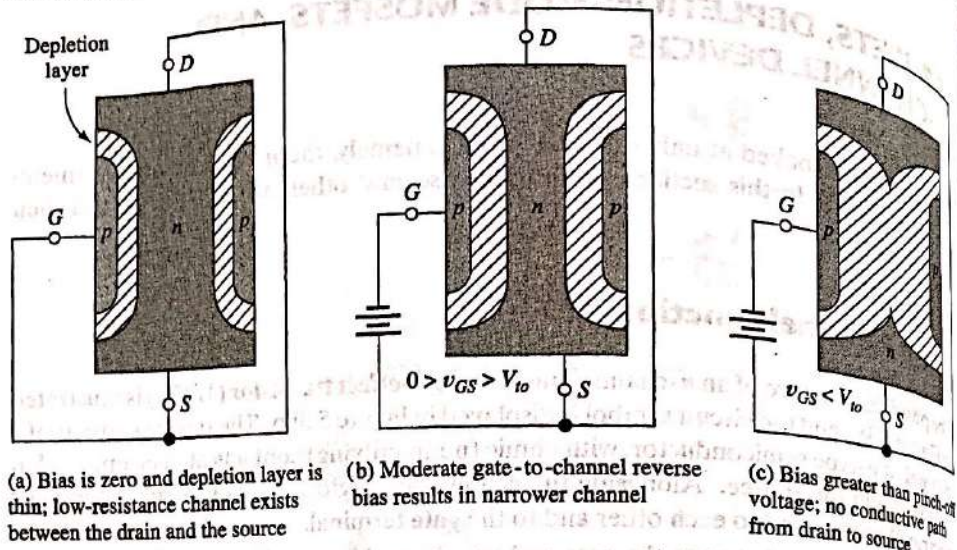


Figure 5.39 The nonconductive depletion region becomes thicker with increased reverse bias. (Note: The two gate regions of each FET are connected to each other.)

... the resistance between the drain and the source depends on the gate-to-channel bias.

amount of reverse bias between gate and channel. Therefore, the resistance between the drain and the source depends on the gate-to-channel bias.

The **pinch-off voltage** V_{to} of a given device is the value of gate-to-channel bias required for the depletion region to extend completely across the channel. Typically, it is a few volts in magnitude and is negative for n -channel devices. (For consistency with SPICE, we use the symbol V_{to} for both the pinch-off voltage of a JFET and the threshold voltage of a MOSFET.)

In the normal operation of an n -channel device, the drain is positive with respect to the source. Current flows into the drain, through the channel, and out of the source. Because the resistance of the channel depends on the gate-to-source voltage, the drain current is controlled by that voltage.

Characteristic Curves for the n -Channel JFET

We now describe the characteristic curves for the n -channel JFET in detail. A diagram of the circuit for this discussion is illustrated in Figure 5.40. To start, suppose that v_{GS} is

Figure 5.40
Circuit for the discussion of drain characteristics of the n -channel JFET.

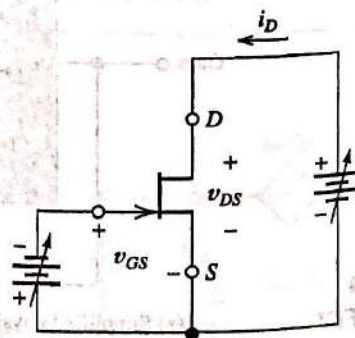
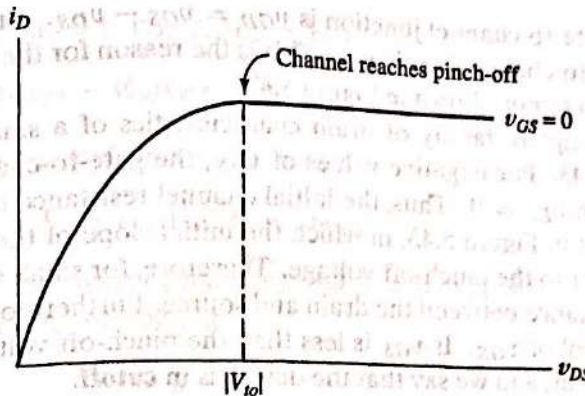


Figure 5.41
Drain current
versus drain-to-
source voltage for
zero gate-to-source
voltage.



zero. Then, as v_{DS} is increased, i_D increases, as shown in Figure 5.41. The channel is a bar of conductive material with ohmic contacts at the ends—exactly the type of construction used for ordinary resistors. Therefore, it is not surprising that i_D is proportional to v_{DS} for small values of v_{DS} .

For larger values of v_{DS} , the drain current increases more and more slowly. This is because the end of the channel closest to the drain is reverse biased by the v_{DS} source. As v_{DS} increases, the depletion layer becomes wider, causing the resistance of the channel to increase, as illustrated in Figure 5.42. After the pinch-off voltage is reached, the drain current becomes nearly constant for additional increases in v_{DS} .

The flow of current results in a voltage drop along the channel (particularly at the drain end, where the channel is very narrow). Thus, the voltage between the channel and the gate varies along the length of the channel. At the drain end of the channel, the bias

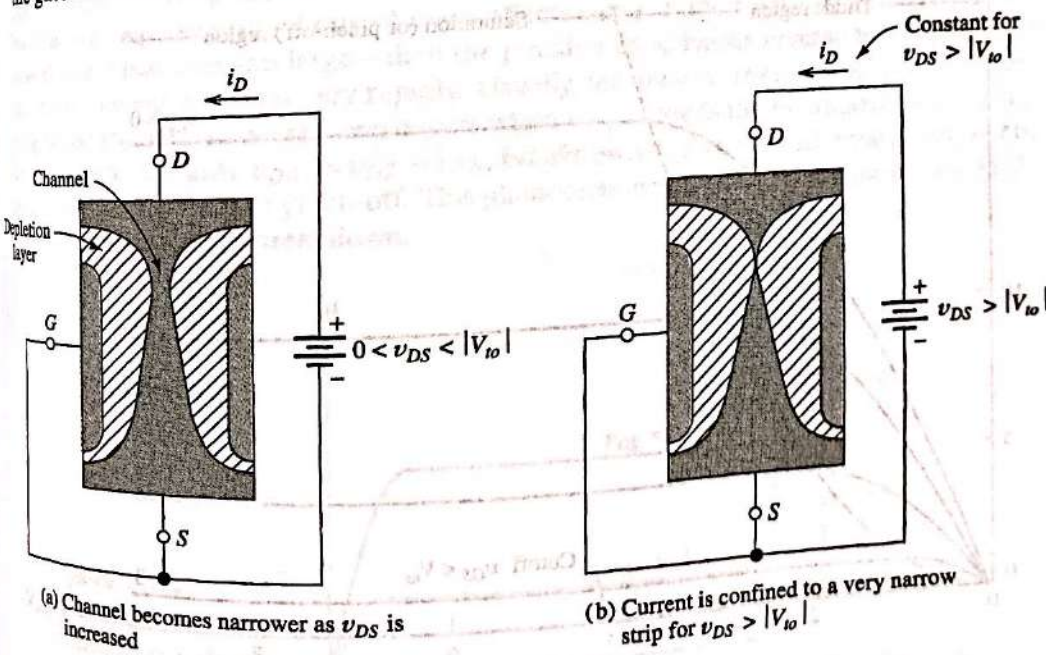


Figure 5.42 n -Channel FET for $v_{GS} = 0$.

of the gate-to-channel junction is $v_{GD} = v_{GS} - v_{DS}$. At the source end of the channel, the gate-to-channel bias is v_{GS} . This is the reason for the tapering of the thickness of the depletion region shown in Figure 5.42.

A complete family of drain characteristics of a small-signal JFET is displayed in Figure 5.43. For negative values of v_{GS} , the gate-to-channel junction is reverse biased even with $v_{DS} = 0$. Thus, the initial channel resistance is higher. This higher resistance is evident in Figure 5.43, in which the initial slope of the curves is smaller for values of v_{GS} closer to the pinch-off voltage. Therefore, for small values of v_{DS} , the FET behaves as a resistance between the drain and source. Furthermore, the resistance value is under the control of v_{GS} . If v_{GS} is less than the pinch-off voltage, the resistance becomes an open circuit, and we say that the device is in **cutoff**.

As in the case with $v_{GS} = 0$, the drain current for other values of v_{GS} eventually becomes constant as v_{DS} is raised, due to pinch-off at the drain end of the channel. The region where the drain current is constant is called the **saturation region** or the **pinch-off region**. The region for which i_D depends on v_{DS} is called the **linear region** or the **triode region**. These regions are labeled in Figure 5.43.

The equations for the drain current of an n -channel JFET are exactly the same as those given earlier for NMOS transistors. As with NMOS transistors, for many JFETs, the characteristic curves slope upward in the saturation region, and we include the term $(1 + \lambda v_{DS})$ in the equations to account for the slope. The equations are as follows:

In cutoff ($v_{GS} \leq V_{to}$),

$$i_D = 0 \quad (5.52)$$

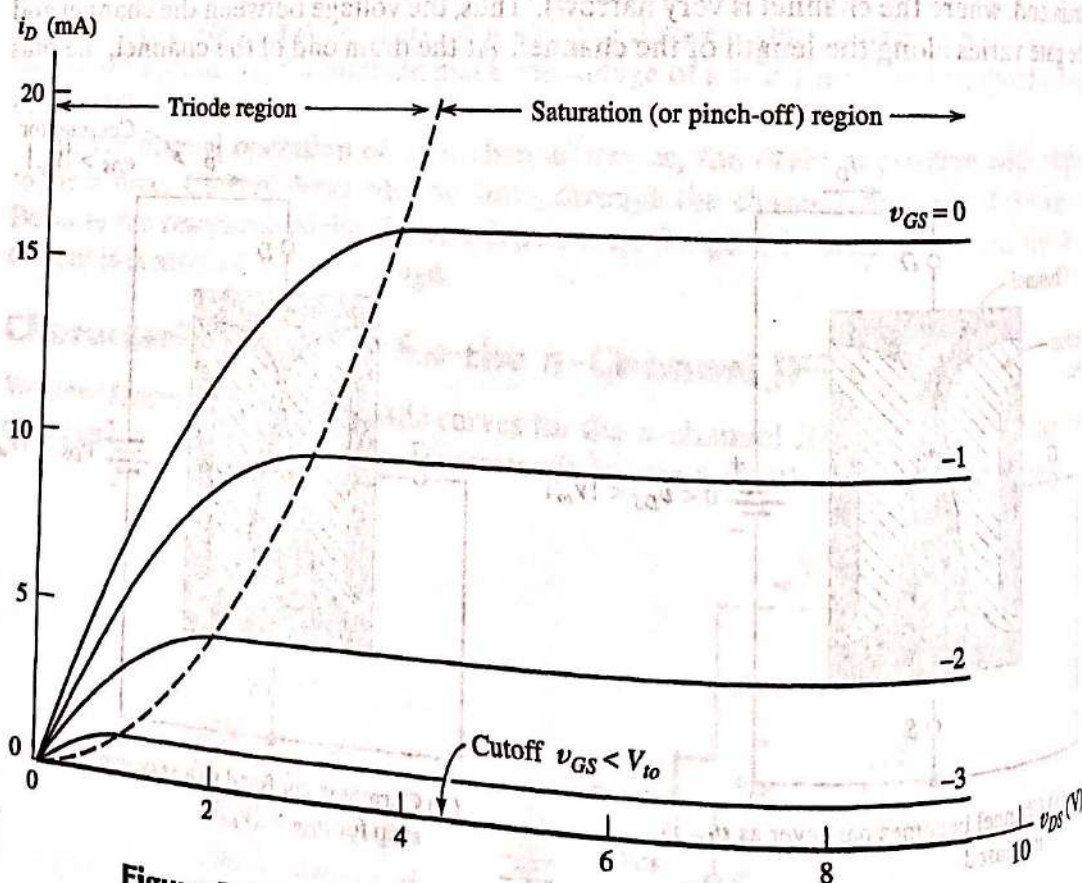


Figure 5.43 Typical drain characteristics of an n -channel JFET.

In the triode region ($v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$),

$$i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] (1 + \lambda v_{DS}) \quad (5.53)$$

In the saturation region ($v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$),

$$i_D = K (v_{GS} - V_{to})^2 (1 + \lambda v_{DS}) \quad (5.54)$$

As in the case of the NMOS transistor (assuming that $\lambda = 0$), the equation for the boundary between the linear and saturation regions is

$$i_D = K v_{DS}^2 \quad (5.55)$$

In the JFET SPICE model, the name for K is BETA.

Zero-Bias Saturation Current

The drain current in the saturation region for $v_{GS} = 0$ is denoted as I_{DSS} and is usually specified on manufacturers' data sheets. Substituting $v_{GS} = 0$ into Equation (5.54) and assuming that $\lambda = 0$, we find that

$$I_{DSS} = K V_{to}^2 \quad (5.56)$$

Solving for K , we have

$$K = \frac{I_{DSS}}{V_{to}^2} \quad (5.57)$$

Breakdown

As we mentioned earlier, several effects are not modeled by the device equations we have given. An example of one of these effects occurs if the reverse bias between gate and channel becomes too large—then the junction experiences reverse breakdown and the drain current increases very rapidly. Usually, the greatest reverse bias is at the drain end of the channel, so breakdown occurs when v_{DG} exceeds the breakdown voltage V_B in magnitude. Because $v_{DG} = v_{DS} - v_{GS}$, breakdown occurs at smaller values of v_{DS} as v_{GS} takes values closer to pinch-off. This phenomenon is illustrated in Figure 5.44. FETs are seldom operated in breakdown.

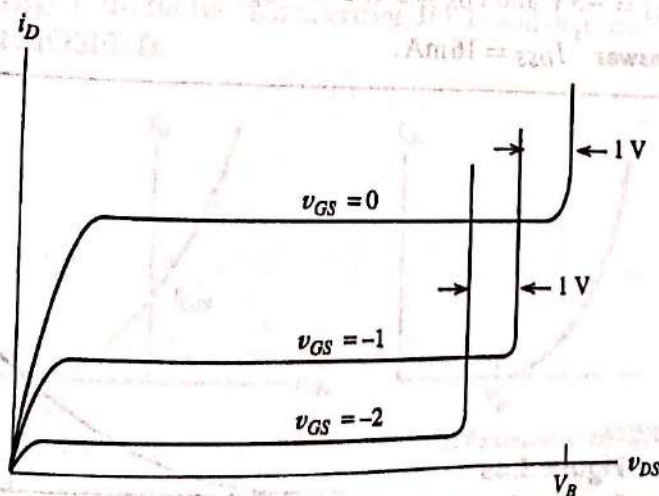


Figure 5.44
If v_{DG} exceeds the breakdown voltage V_B , drain current increases rapidly.

EXERCISE

5.13 A certain n -channel JFET has $\lambda = 0$, $I_{DSS} = 18 \text{ mA}$, and $V_{to} = -3 \text{ V}$. Determine the value of K , and sketch the drain characteristic curves to scale for $v_{GS} = 0, -1, -2$, and -3 V and for v_{DS} ranging from 0 to 10 V. Check your sketches by using a SPICE simulation. (Hint: See Example 5.2, but replace the NMOS transistor with a JFET. The SPICE name for the device parameter K is BETA.)

Answer $K = 2 \text{ mA/V}^2$; the simulation is stored in file Exer5_13.

EXERCISE

5.14 Plot i_D against v_{GS} for the JFET of Exercise 5.13, assuming that the circuit is operating in the saturation region.

Answer See Figure 5.45.

EXERCISE

5.15 Consider an n -channel JFET with $V_{to} = -4 \text{ V}$. What is the region of operation (linear, saturation, or cutoff) if (a) $v_{GS} = -5 \text{ V}$ and $v_{DS} = 5 \text{ V}$? (b) $v_{GS} = -2 \text{ V}$ and $v_{DS} = 1 \text{ V}$? (c) $v_{GS} = -1 \text{ V}$ and $v_{DS} = 5 \text{ V}$? (d) $v_{GS} = 0 \text{ V}$ and $v_{DS} = 2 \text{ V}$?

Answer (a) cutoff; (b) linear; (c) saturation; (d) linear.

EXERCISE

5.16 A certain n -channel JFET has $V_{to} = -4 \text{ V}$. Furthermore, $i_D = 1 \text{ mA}$ for $v_{GS} = -3 \text{ V}$ and $v_{DS} = 5 \text{ V}$. Find I_{DSS} for this device.

Answer $I_{DSS} = 16 \text{ mA}$.

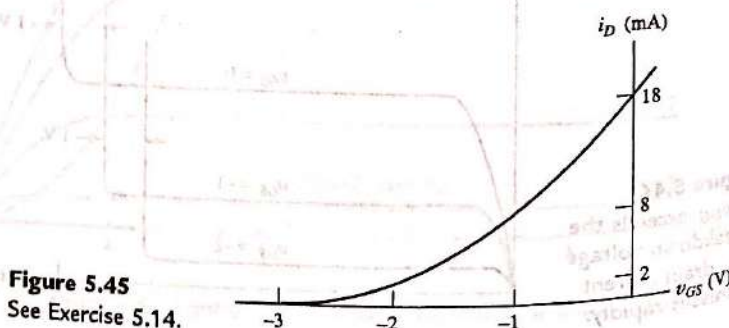
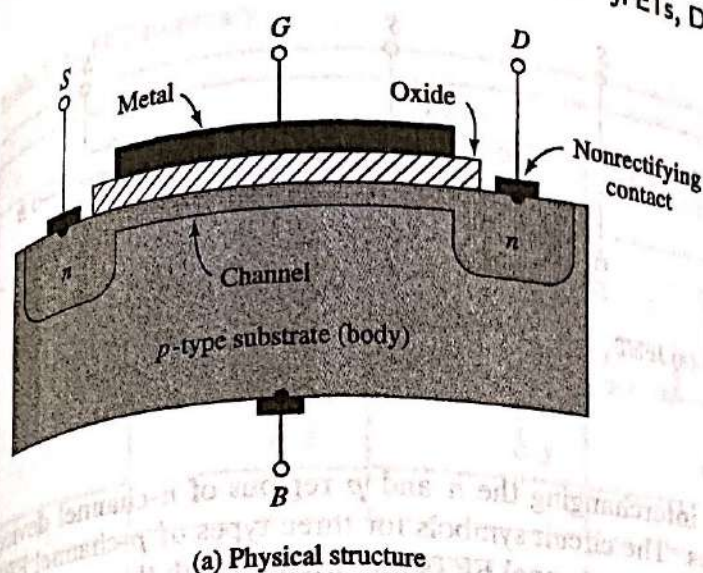
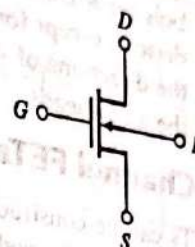


Figure 5.45
See Exercise 5.14.



(a) Physical structure



(b) Circuit symbol

Figure 5.46 *n*-Channel depletion MOSFET.

Depletion MOSFETs

The depletion MOSFET has characteristics nearly identical to those of the JFET, but its construction, which is shown in Figure 5.46a, is somewhat different. A thin channel of *n*-type semiconductor connects the source and drain. On top of the channel is a layer of insulating material such as silicon dioxide. On top of the insulator is a layer of metal (aluminum or polycrystalline silicon) that forms the gate. The *p*-region is called the substrate, or the body.

The main operational difference between the *n*-channel JFET and the *n*-channel depletion MOSFET is the fact that the MOSFET can be operated with positive values of v_{GS} . (This is usually not done with the JFET, because it would result in forward bias of the gate-to-channel junction.) The output characteristics of the devices are nearly identical, and the equations we have given earlier for the *n*-channel JFET also apply to the *n*-channel depletion MOSFET.

Figure 5.47 shows the drain current versus v_{GS} for the three types of *n*-channel FETs. Notice that the parameter I_{DSS} is useful for characterizing JFETs and depletion MOSFETs, but not enhancement MOSFETs.

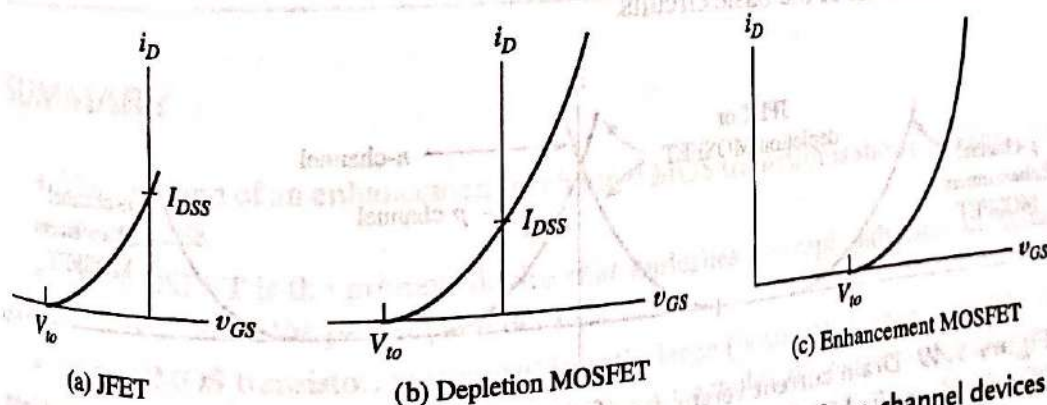
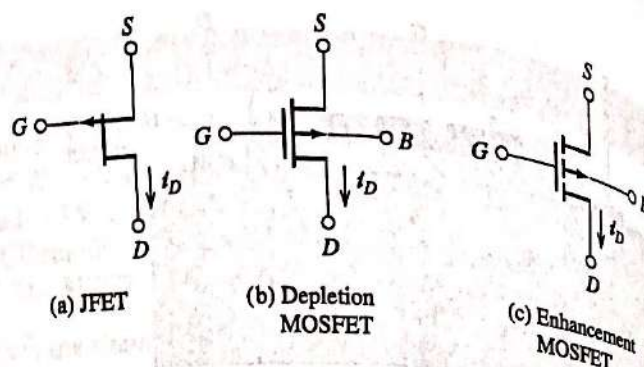

Figure 5.47 Drain current versus v_{GS} in the saturation region for *n*-channel devices.

Figure 5.48
p-Channel FET
 circuit symbols. These are the same as the circuit symbols for *n*-channel devices, except for the directions of the arrowheads.



p-Channel FETs

The *p*-channel FETs are oriented with the source at the top, so that current normally flows from top to bottom.

FETs can be constructed by interchanging the *n* and *p* regions of *n*-channel devices, resulting in *p*-channel devices. The circuit symbols for three types of *p*-channel FETs are illustrated in Figure 5.48. The *p*-channel FETs are oriented with the source at the top, so that current normally flows from top to bottom. The symbols are the same as for the *n*-channel devices, except for the directions of the arrowheads. Notice that the symbol for the enhancement MOSFET has a dashed line connecting the drain and the source, suggesting that a channel is not present with zero bias. On the other hand, the symbol for the depletion device has a solid line connecting the drain and the source.

The characteristics of *p*-channel FETs are the same as for *n*-channel devices, except that voltage polarities and current directions are inverted. If we reference the drain current out of the drain of *p*-channel devices, the characteristic curves of a *p*-channel device are exactly like those of an *n*-channel device, except that the algebraic signs of the voltages must be inverted. Figure 5.49 shows the drain currents versus v_{GS} in saturation for the various types of FET. Table 5.1 summarizes the characteristics of all of the FETs that we have discussed.

Small-Signal Equivalent Circuits

The small-signal equivalent circuit that we introduced for the enhancement NMOS transistor applies to all of the other types of FETs. Table 5.1 gives equations for computing g_m , given the device parameters and operating point.

Many variations of bias circuits, common-source amplifiers, and source followers that we discussed earlier in this chapter can be designed using JFETs and *p*-channel devices. The problems at the end of this chapter give you a chance to practice your analytical skills on many variations of the basic circuits.

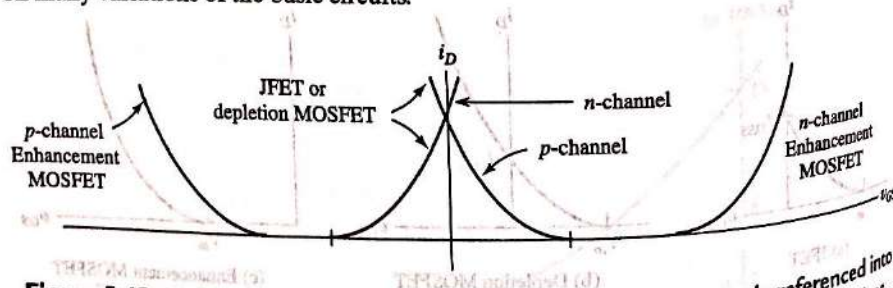


Figure 5.49 Drain current versus v_{GS} for several types of FETs. i_D is referenced into the drain terminal for *n*-channel devices and out of the drain for *p*-channel devices.

Table 5.1. FET summary.

Circuit symbol	n-Channel			p-Channel		
	Enhancement MOSFET	Depletion MOSFET	JFET	Enhancement MOSFET	Depletion MOSFET	JFET
V_{to}	+	-	-	-	+	+
K	$\frac{1}{2} \mu_n C_{ox} (W/L) = \frac{1}{2} KP(W/L)$			$\frac{1}{2} \mu_p C_{ox} (W/L) = \frac{1}{2} KP(W/L)$		
λ	+			-		
Cutoff region	$v_{GS} \leq V_{to}$ $i_D = 0$			$v_{GS} \geq V_{to}$ $i_D = 0$		
Triode region	$v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$ $i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2](1 + \lambda v_{DS})$			$v_{GS} \leq V_{to}$ and $0 \geq v_{DS} \geq v_{GS} - V_{to}$ $i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2](1 + \lambda v_{DS})$		
Saturation region	$v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ $i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$			$v_{GS} \leq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$ $i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$		
g_m (Assuming operation in saturation and $\lambda = 0$)	$g_m = 2\sqrt{KI_{DQ}}$ $g_m = \sqrt{2KP(W/L)I_{DQ}}$	$g_m = 2\sqrt{KI_{DQ}}$ $g_m = 2\frac{\sqrt{I_{DSS}I_{DQ}}}{ V_{to} }$		$g_m = 2\sqrt{KI_{DQ}}$ $g_m = \sqrt{2KP(W/L)I_{DQ}}$	$g_m = 2\sqrt{KI_{DQ}}$ $g_m = 2\frac{\sqrt{I_{DSS}I_{DQ}}}{ V_{to} }$	
SPICE parameters	VTO = V_{to} KP = $\mu_n C_{ox}$ L W LAMBDA = λ			VTO = V_{to} BETA = K LAMBDA = λ KP = $\mu_p C_{ox}$ L W LAMBDA = $ \lambda $		

SUMMARY

- The structure of an enhancement *n*-channel MOS transistor is shown in Figure 5.1 on page 288.
- The MOSFET is the primary device that underlies the rapid advances in digital electronics over the past several decades.
- In an NMOS transistor, when a sufficiently large (positive) voltage is applied to the gate relative to the source, electrons are attracted to the region under the gate, and a channel of *n*-type material is induced between the drain and the source.

Then, if voltage is applied between the drain and the source, current flows into the drain, through the channel, and out the source. Drain current is controlled by the voltage applied to the gate.

- MOSFETs operate in cutoff, in the triode region, or in saturation.
- Usually, μ_n and C_{ox} are determined by the fabrication process. However, in designing a circuit, we can modify the ratio W/L to obtain transistors best suited to various parts of the circuit.
- Simple amplifier circuits can be analyzed by using graphical (load-line) techniques.
- Distortion occurs in FET amplifiers because of the nonuniform spacing of the drain characteristics. Distortion is less pronounced for smaller signal amplitudes.
- For use as amplifiers, FETs are usually biased in the saturation region.
- Figure 5.16a on page 302 shows a good discrete bias circuit that is suitable for JFETs as well as MOSFETs. For Q -points that are nearly independent of variations in FET parameters, we want to choose a large value for V_G .
- In a small-signal midband analysis, a FET can be modeled by the equivalent circuit illustrated in Figure 5.23 on page 311.
- Transconductance is defined as

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{Q\text{-point}}$$

- Small-signal drain resistance of a FET is defined as

$$\frac{1}{r_d} = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{Q\text{-point}}$$

- In small-signal midband analysis of FET amplifiers, the coupling capacitors, bypass capacitors, and dc voltage sources are replaced by short circuits. The FET is replaced with its small-signal equivalent circuit. Then we write circuit equations and derive useful expressions for gains, input impedance, and output impedance.
- A clear understanding of small-signal equivalent-circuit analysis is very important to design engineers.
- To find the output resistance of an amplifier, we disconnect the load, replace the signal source by its internal resistance, and then find the resistance seen looking into the output terminals.
- The common-source amplifier is inverting and has a relatively large voltage gain.
- Unbypassed impedance between the FET source terminal and ground strongly reduces the gain of a common-source amplifier.
- The source follower has voltage gain slightly less than unity, high current gain, and relatively low output impedance. It is noninverting.
- We have considered three types of FETs: enhancement MOSFETs, depletion MOSFETs, and JFETs, each of which can be either n -channel or p -channel. A convenient summary is given in Table 5.1 on page 333. Enhancement MOSFETs are the most important type of FET in integrated circuits, especially those that are digital. JFETs are the predominant type of FET in discrete circuits.

PROBLEMS

Section 5.1: NMOS Transistors

- 5.1. Sketch the physical structure of an n -channel enhancement MOSFET. Label the channel length L , the width W , the terminals, and the channel region. Draw the corresponding circuit symbol.
- 5.2. Give the ranges of v_{GS} , v_{DS} , and v_{GD} in terms of the threshold voltage V_{to} for each region (cutoff, saturation, and triode) of an n -channel MOSFET.
- 5.3. A certain NMOS transistor has $V_{to} = 1$ V, $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0$, $L = 5 \mu\text{m}$, and $W = 50 \mu\text{m}$. For each set of voltages, state the region of operation and compute the drain current. (a) $v_{GS} = 4$ V and $v_{DS} = 10$ V; (b) $v_{GS} = 4$ V and $v_{DS} = 2$ V; (c) $v_{GS} = 0$ V and $v_{DS} = 10$ V.
- 5.4. An n -channel enhancement MOSFET has $V_{to} = 3$ V and $K = 0.5 \text{ mA}/\text{V}^2$. If $v_{GS} = 5$ V, for what range of v_{DS} is the device in the saturation region? In the triode region? Plot i_D against v_{GS} for operation in the saturation region.
- 5.5. Suppose that we have an NMOS transistor with $KP = 50 \mu\text{A}/\text{V}^2$, $V_{to} = 1$ V, $\lambda = 0$, $L = 10 \mu\text{m}$, and $W = 200 \mu\text{m}$. Sketch the drain characteristics for v_{DS} ranging from 0 to 10 V and $v_{GS} = 0, 1, 2, 3$, and 4 V. Check your hand-drawn sketches by using SPICE to plot the characteristic curves.
- 5.6. Consider an NMOS with $V_{to} = 1$ V. What is the region of operation (linear, saturation, or cutoff) if (a) $v_{GS} = 0$ V and $v_{DS} = 5$ V? (b) $v_{GS} = 3$ V and $v_{DS} = 1$ V? (c) $v_{GS} = 3$ V and $v_{DS} = 6$ V? (d) $v_{GS} = 5$ V and $v_{DS} = 10$ V?
- 5.7. An NMOS transistor is needed for which $i_D = 0.5$ mA when $v_{GS} = v_{DS} = 5$ V. Process constraints result in $KP = 50 \mu\text{A}/\text{V}^2$ and $V_{to} = 1$ V. Assume that $\lambda = 0$. Determine the width-to-length ratio needed for the transistor. If $L = 2 \mu\text{m}$, what is the value of W ? Repeat for $\lambda = 0.05$.
- 5.8. Suppose that, because of process constraints, L and W are required to be at least $0.5 \mu\text{m}$. Furthermore, to save chip area, we do not want L or W to exceed $2 \mu\text{m}$. Assume that $\lambda = 0$. How would you select L and W to obtain the least drain current for a given transistor? The greatest drain current? Assuming operation with identical voltages, what ratio of drain currents (between different transistors) can be achieved?
- 5.9. Suppose that, because of process constraints, L and W are required to be at least $0.5 \mu\text{m}$. Furthermore, to save chip area, we do not want L or W to exceed $2 \mu\text{m}$. Assume that $\lambda = 0.1/L$ where L is in μm , $V_{to} = 1$ V, and $KP = 50 \mu\text{A}/\text{V}^2$. How would you choose L and W to minimize the chip area consumed by the transistor? Plot the

drain characteristics of the minimum-area transistor to scale for v_{GS} and v_{DS} ranging from 0 to 5 V, either manually or by using SPICE.

5.10. Two points in the saturation region of a certain NMOS transistor are: ($v_{GS} = 2$ V, $i_D = 0.5$ mA) and ($v_{GS} = 3$ V, $i_D = 2$ mA). Assume that $\lambda = 0$. Determine the values of V_{to} and K for this transistor.

5.11. A certain NMOS transistor has $V_{to} = 1$ V. Two points on the characteristic curve for $v_{GS} = 3$ V are: ($v_{DS} = 5$ V, $i_D = 1$ mA) and ($v_{DS} = 10$ V, $i_D = 1.25$ mA). Determine the value of λ for this transistor.

5.12. What is "gate protection" for a MOSFET? Why is it necessary?

5.13. Assume that an NMOS transistor is operating with $v_{DS} \ll v_{GS} - V_{to}$, as illustrated in Figure 5.4. Find an expression for the resistance of the channel in terms of the device parameters and voltages. Assume that $\lambda = 0$. Given that $V_{to} = 1$ V and $K = 0.25 \text{ mA}/\text{V}^2$, compute the resistance for $v_{GS} = 0.5, 1, 1.5$, and 2 V.

Section 5.2: Load-Line Analysis of a Simple NMOS Amplifier

5.14. Why does distortion occur in FET amplifiers?

5.15. Draw the load lines on the i_D - v_{DS} axes for the circuit of Figure 5.13 for

(a) $R_D = 1 \text{ k}\Omega$ and $V_{DD} = 20$ V.

(b) $R_D = 2 \text{ k}\Omega$ and $V_{DD} = 20$ V.

(c) $R_D = 3 \text{ k}\Omega$ and $V_{DD} = 20$ V.

How does the position of the load line change as R_D increases in value?

5.16. Draw the load lines on the i_D - v_{DS} axes for the circuit of Figure 5.13 for

(a) $R_D = 1 \text{ k}\Omega$ and $V_{DD} = 5$ V.

(b) $R_D = 1 \text{ k}\Omega$ and $V_{DD} = 10$ V.

(c) $R_D = 1 \text{ k}\Omega$ and $V_{DD} = 15$ V.

How does the position of the load line change as V_{DD} increases in value?

5.17. Consider the circuit shown in Figure 5.13. The transistor characteristics are illustrated in Figure 5.14. Suppose that V_{GG} is changed to 0 V. Determine the values of V_{DSQ} , $V_{DS\min}$, and $V_{DS\max}$. What is the gain of the amplifier?

5.18. Consider the amplifier shown in Figure P5.18.

(a) Find $v_{GS}(t)$, assuming that the coupling capacitor is a short circuit for the ac signal.

(b) If the FET has $V_{to} = 1$ V and $K = 0.5 \text{ mA}/\text{V}^2$, sketch its drain characteristics to scale for $v_{GS} = 1, 2, 3$, and 4 V.

(c) Draw the load line for the amplifier on the characteristics.

(d) Find the values of V_{DSQ} , $V_{DS\min}$, and $V_{DS\max}$.

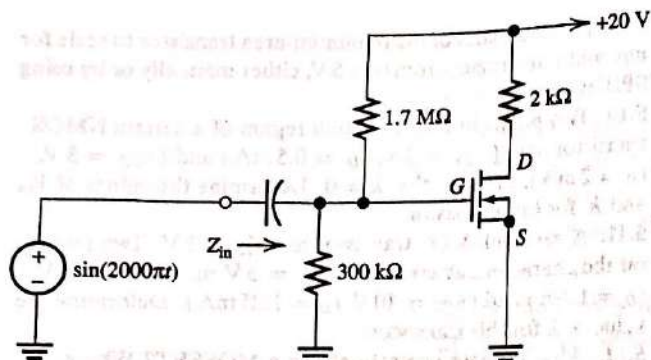


Figure P5.18

5.19. What is the largest value of R_D allowed in the circuit of Problem 5.18 if the instantaneous operating point is required to remain in the saturation region at all times?

5.20. The distorted signal shown in Figure 5.15 can be written as

$$v_{DS}(t) = V_{DC} + V_{1m} \sin(2000\pi t) + V_{2m} \cos(4000\pi t)$$

The term $V_{1m} \sin(2000\pi t)$ is the desired signal. The term $V_{2m} \cos(4000\pi t)$ is distortion, which in this case has twice the frequency of the input signal and is called second-harmonic distortion. Determine the values of V_{1m} and V_{2m} and the percentage of second-harmonic distortion, which is defined as $|V_{2m}/V_{1m}| \times 100\%$. (A high-quality audio amplifier has a distortion percentage less than 0.1%.)

Section 5.3: Bias Circuits

5.21. The fixed-plus self-bias circuit of Figure 5.16 has $V_{DD} = 15$ V, $R_1 = 2$ MΩ, $R_2 = 1$ MΩ, $R_S = 4.7$ kΩ, and $R_D = 4.7$ kΩ. The MOSFET has $V_{to} = 1$ V, $\lambda = 0$, and $K = 0.25$ mA/V². Determine the Q -point.

5.22. Find I_{DQ} and V_{DSQ} for the circuit shown in Figure P5.22. The MOSFET has $V_{to} = 1$ V, $\lambda = 0$, and $K = 0.25$ mA/V².

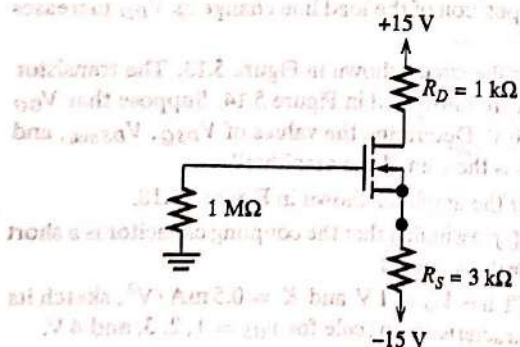


Figure P5.22

5.23. (a) Find the value of I_{DQ} for the circuit shown in Figure P5.23. Assume that $V_{to} = 4$ V, $\lambda = 0$, and $K = 1$ mA/V². (b) Repeat for $V_{to} = 2$ V, $\lambda = 0$, and $K = 2$ mA/V².

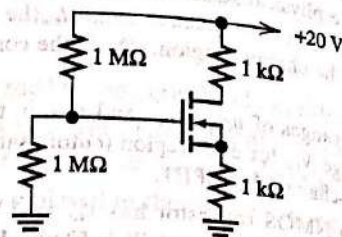


Figure P5.23

D5.24. Fixed-plus self-bias circuit design. Design a fixed-plus self-bias circuit for a common-source NMOS amplifier. Nominally, the transistor has $KP = 50$ μA/V², $W = 80$ μm, $L = 10$ μm, $\lambda = 0$, and $V_{to} = 1$ V. The circuit is to have $V_{DD} = 12$ V and $I_{DQ} \cong 1$ mA. We suggest these design guidelines for the NMOS bias circuit for the common-source amplifier: $R_D I_{DQ} = V_{DD}/4$, $V_{DSQ} = V_{DD}/2$; $R_S I_{DQ} = V_{DD}/4$.

D5.25. Fixed-plus self-bias circuit design. Design a fixed-plus self-bias circuit for an NMOS source follower. Nominally, the transistor has $KP = 50$ μA/V², $W = 80$ μm, $L = 10$ μm, $\lambda = 0$, and $V_{to} = 1$ V. The circuit is to have $V_{DD} = 12$ V and $I_{DQ} \cong 1$ mA. We suggest these design guidelines for the NMOS bias circuit for the source follower: $V_{DSQ} \cong V_{DD}/2$ and $R_S I_{DQ} = V_{DD}/2$.

5.26. Find I_{DQ} and V_{DSQ} for the circuit shown in Figure P5.26. The MOSFET has $V_{to} = 1$ V, $\lambda = 0$, and $K = 0.25$ mA/V².

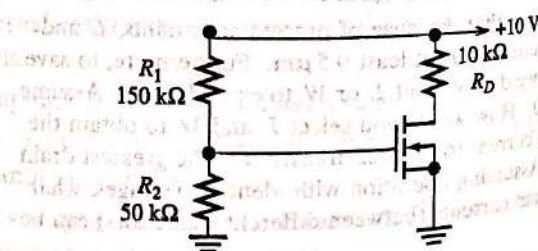


Figure P5.26

5.27. Find I_{DQ} and V_{DSQ} for the circuit displayed in Figure P5.27. The MOSFET has $V_{to} = 1$ V, $\lambda = 0$, and $K = 0.25$ mA/V².

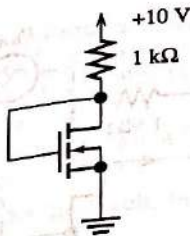


Figure P5.27

Section 5.4: Small-Signal Equivalent Circuits

- 5.28. Draw the small-signal equivalent circuit for a FET, including r_d .
- 5.29. Give definitions of g_m and r_d as partial derivatives.
- 5.30. A certain NMOS transistor has $\lambda = 0$. What is the value of r_d , assuming operation in the saturation region?
- 5.31. What is the value of g_m for $V_{DSQ} = 0$? Draw the small-signal equivalent circuit at this bias point. For what applications is the FET used at this bias point?
- 5.32. Derive an expression for g_m in terms of K , V_{io} , V_{GSQ} , and I_{DQ} for an NMOS transistor operating in the triode region. Assume that $\lambda = 0$.
- 5.33. Derive an expression for r_d in terms of K , V_{io} , V_{GSQ} , and V_{DSQ} for an NMOS transistor operating in the triode region. Assume that $\lambda = 0$.
- 5.34. A certain NMOS transistor has $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0.1$, $L = 2 \mu\text{m}$, $W = 100 \mu\text{m}$, and $V_{io} = 1 \text{ V}$.
- Use a SPICE program to produce a plot of the drain characteristics of this transistor for v_{DS} ranging from 0 to 10 V and v_{GS} ranging from 1 to 3 V.
 - Use the characteristics plotted in part (a) to graphically determine the values of g_m and r_d at the operating point defined by $V_{DSQ} = 8 \text{ V}$ and $V_{GSQ} = 2 \text{ V}$.
 - Devise a circuit for this transistor so that it operates at the Q -point defined in part (b). Use SPICE to perform an operating-point analysis of your circuit. Then find the values of g_m and r_d in the output file, and compare them with the values found in part b. (PSpice refers to $1/r_d$ as GDS.)
- 5.35. A certain NMOS transistor has $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0.1$, $L = 2 \mu\text{m}$, $W = 100 \mu\text{m}$, and $V_{io} = 1 \text{ V}$. Use SPICE to obtain a plot of g_m versus I_{DQ} for $V_{DSQ} = 8 \text{ V}$. Allow V_{GSQ} to range from 0 to 3 V. (Hint: Simulate the circuit shown in Figure 5.7 with $V_{DS} = 8 \text{ V}$. Sweep V_{GS} from 0 to 3 V. Then use Probe to obtain a plot of di_D/dv_{GS} versus i_D .)

Section 5.5: The Common-Source Amplifier

- 5.36. What is the function of coupling capacitors? With what are they replaced in a midband small-signal equivalent circuit? In general, what effect do coupling capacitors have on the gain of an amplifier as a function of frequency?
- 5.37. Draw the circuit diagram of a resistance-capacitance coupled common-source amplifier.
- 5.38. Consider the amplifier illustrated in Figure P5.38.
- Draw the small-signal midband equivalent circuit.
 - Assume that $r_d = \infty$, and derive expressions for the voltage gain, input resistance, and output resistance.
 - Find I_{DQ} if $R = 100 \text{ k}\Omega$, $R_f = 100 \text{ k}\Omega$, $R_D = 3 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, $V_{DD} = 20 \text{ V}$, $V_{io} = 5 \text{ V}$, and $K = 1 \text{ mA}/\text{V}^2$. Determine the value of g_m at the Q -point.
 - Evaluate the expressions found in part (b).
 - Find $v_o(t)$ if $v_i(t) = 0.2 \sin(2000\pi t)$.
 - Is this amplifier inverting or noninverting? Would you classify the input resistance as high, moderate, or low compared with that of other types of FET amplifier?

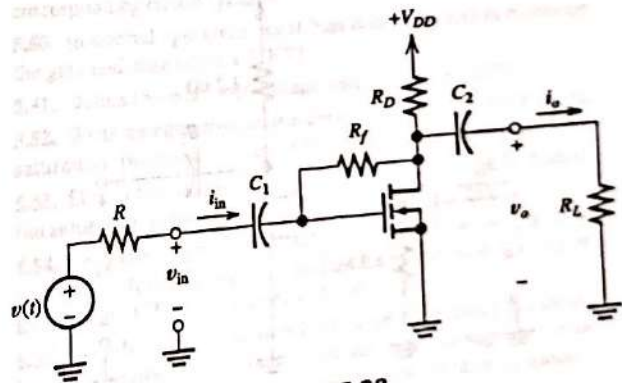


Figure P5.38

- 5.39. Find V_{DSQ} and I_{DQ} for the FET displayed in Figure P5.39, given that $V_{io} = 3 \text{ V}$ and $K = 0.5 \text{ mA}/\text{V}^2$. Find the value of g_m at the operating point. Draw the small-signal equivalent circuit, assuming that $r_d = \infty$. Derive an expression for the resistance R_o in terms of R_D and g_m . Evaluate the expression for the values given.

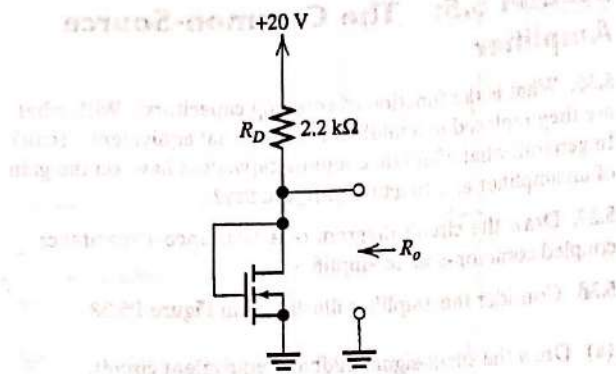


Figure P5.39

(Note: The following common-source problems require some knowledge of the various types of FET discussed in Section 5.7. Refer to Table 5.1 on page 333.)

5.40. Find the midband values of the voltage gain, input resistance, and output resistance for the common-source amplifier shown in Figure P5.40. The depletion-mode NMOS transistor has $V_{to} = -3$ V and $K = 1$ mA/V². Assume that $r_d = \infty$.

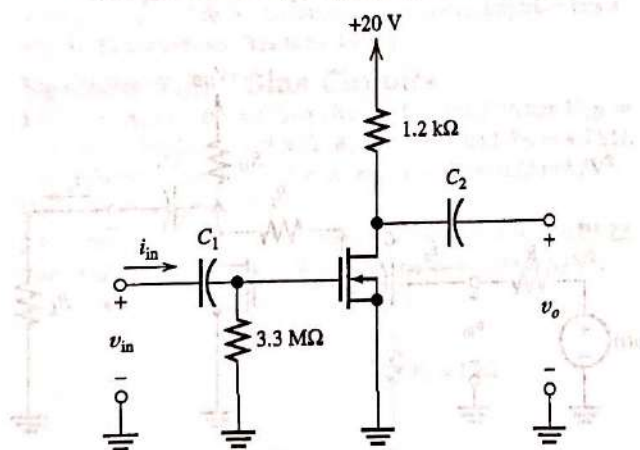
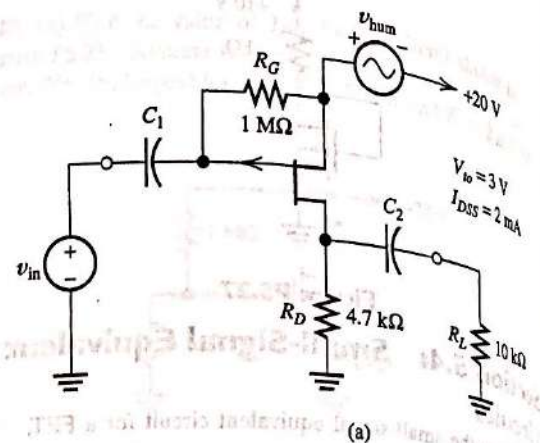
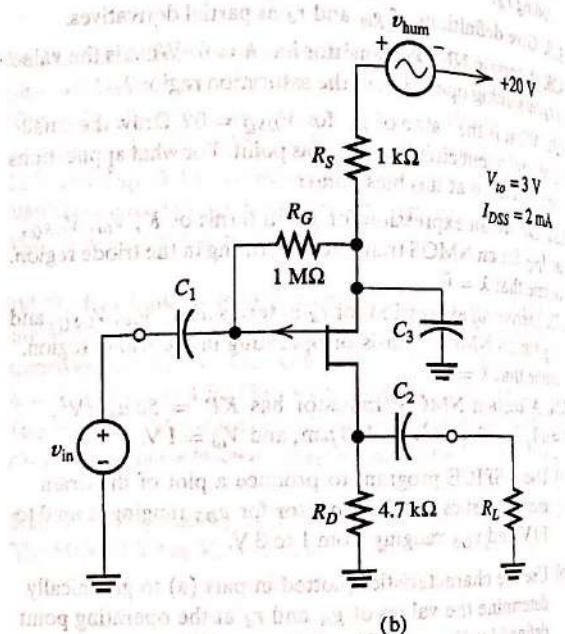


Figure P5.40

5.41. Draw the midband small-signal equivalent circuit for the amplifier shown in Figure P5.41a. Assume that $v_{hum} = 0$ and $r_d = \infty$. What type of amplifier is this? Derive an expression for the voltage gain $A_v = v_o/v_{in}$ in terms of g_m , R_D , and R_L . Evaluate the expression for the values shown in the figure.



(a)



(b)

Figure P5.41

5.42. Consider the circuit shown in Figure P5.41a. The ac voltage source v_{hum} represents power-supply ripple. Draw the small-signal equivalent circuit. Replace the signal source v_{in} by a short circuit, and derive an expression for the gain $A_{hum} = v_o/v_{hum}$. Evaluate the expression for the values given in the figure. If you have worked Problem 5.41, compare A_{hum} with A_v .

5.43. Draw the small-signal equivalent circuit for the circuit of Figure P5.41b. Assume that the capacitors are short circuits for the hum and the signal. Verify that the circuits of Figure P5.41

have the same small-signal equivalent circuit if $v_{hum} = 0$. What is the value of A_{hum} (see Problem 5.42) for the circuit of Figure P5.41b? Which of the two circuits of Figure P5.41 is better for use with a noisy power supply?

5.44. Consider the amplifier shown in Figure P5.44. The FET has $V_{to} = -4$ V and $K = 1$ mA/V².

(a) Find the Q -point for the circuit. In what region is the FET operating?

(b) Find the values of g_m and r_d at the Q -point found in part (a).

(c) Find the input resistance, voltage gain, and output resistance of the amplifier.

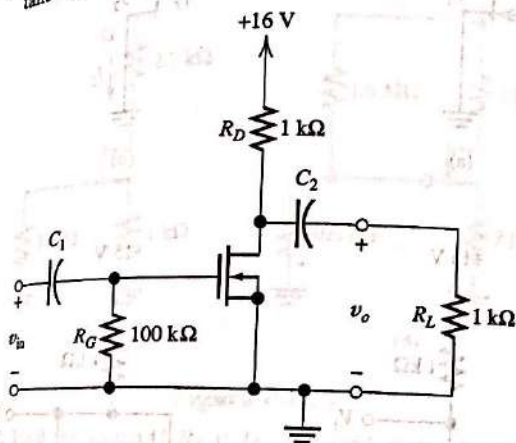


Figure P5.44

Section 5.6: The Source Follower

5.45. Draw the circuit diagram of a resistance-capacitance coupled source follower.

5.46. Consider the common-source amplifier and the source follower. Which amplifier would be used if a voltage gain magnitude larger than unity is needed? Which would be used to obtain low output resistance?

5.47. Consider the source follower shown in Figure 5.33, given that $V_{DD} = 15$ V, $R_L = 2$ kΩ, $R_1 = 1$ MΩ, and $R_2 = 2$ MΩ. The NMOS transistor has $KP = 50$ μA/V², $\lambda = 0$, $L = 10$ μm, $W = 160$ μm, and $V_{to} = 1$ V. Find the value required for R_S to achieve $I_{DQ} = 2$ mA. Then compute the voltage gain, input resistance, and output resistance of the circuit.

5.48. (This problem assumes knowledge of JFETs from Section 5.7. Refer to Table 5.1 on page 333.) Consider the source follower illustrated in Figure P5.48.

(a) Draw the small-signal equivalent circuit for the midband region. Assume that $r_d = \infty$.

(b) Derive expressions for the voltage gain, input resistance, and output resistance.

(c) Suppose that $R_G = 2$ MΩ, $R_S = 1$ kΩ, $R_L = 10$ kΩ, $V_{DD} = 15$ V, $R = 100$ kΩ, and the FET parameters are $K = 0.2$ mA/V² and $V_{to} = 2$ V. Find the operating point and the value of g_m .

(d) Use the values of part (c) to evaluate the expressions of part (b).

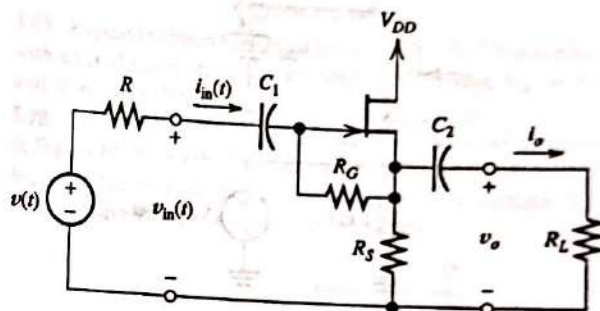


Figure P5.48 Source follower.

Section 5.7: JFETs, Depletion-Mode MOSFETs, and p -Channel Devices

5.49. Sketch the (simplified) physical structure of an n -channel JFET. Label the terminals and the channel region. Draw the corresponding circuit symbol.

5.50. In normal operation, what bias condition exists between the gate and channel of a JFET?

5.51. Define the pinch-off voltage and I_{DSS} of a JFET.

5.52. Write an equation for the drain current of a JFET in the saturation (pinch-off) region in terms of device voltages.

5.53. Sketch the characteristics of an n -channel JFET. Label the saturation (pinch-off), triode, and cutoff regions.

5.54. Give the ranges of v_{GS} and v_{GD} in terms of the pinch-off voltage V_{to} for each region (cutoff, saturation, and triode) of an n -channel JFET or depletion MOSFET.

5.55. Sketch the physical structure of an n -channel depletion MOSFET. Label the terminals and the channel region. Draw the corresponding circuit symbol. Repeat for a p -channel enhancement MOSFET.

5.56. An n -channel JFET has $V_{to} = -3$ V, $\lambda = 0$, and $I_{DSS} = 9$ mA. Assuming that the device is operating in the saturation region, what value of v_{GS} is required for $i_D = 4$ mA?

5.57. The JFET of Problem 5.56 has $v_{GS} = -1$ V. For what range of v_{DS} is the device in the saturation region? Repeat for $v_{GS} = -2$ V.

5.58. The JFET of Problem 5.56 has $v_{GS} = -1$ V and $v_{DS} = 1$ V. Determine the drain current. Repeat for $v_{GS} = -1$ V and $v_{DS} = 5$ V.

5.59. For what range of v_{GS} is the FET of Problem 5.56 in cutoff? Assume that $v_{DS} > 0$.

5.60. Consider the circuit shown in Figure P5.60. It is found that as V_{DD} is increased, the voltmeter reading increases until V_{DD} reaches 16 V, after which the reading is constant at 13 V. What are the values of I_{DSS} and V_{to} for the FET?

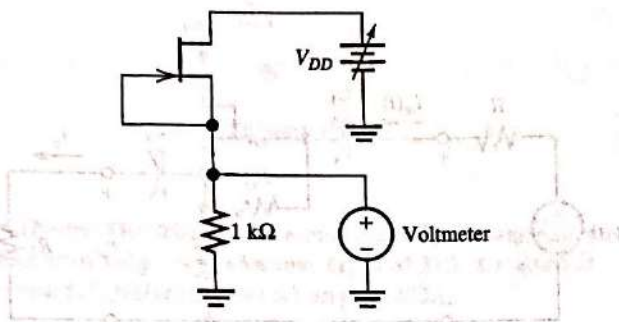


Figure P5.60

5.61. An n -channel depletion MOSFET has $V_{to} = -4$ V and $K = 0.25$ mA/V². Find the value of I_{DSS} . Plot the boundary between the triode region and the saturation region on the i_D - v_{DS} plane.

5.62. A p -channel JFET has $V_{to} = 4$ V and $I_{DSS} = 16$ mA. Sketch the drain characteristics to scale for v_{DS} ranging from 0 to -10 V. Show the curves for $v_{GS} = 0, 1, 2, 3$, and 4 V. Use SPICE to check your sketches. (Hint: In PSpice, specify VTO = -4 V.)

5.63. The voltmeters displayed in Figure P5.63 have very high impedances. Approximately what does the meter read for each circuit?

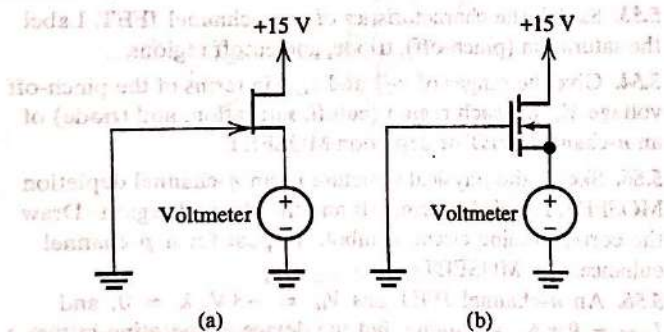


Figure P5.63

5.64. A p -channel enhancement MOSFET has $V_{to} = -2$ V and $K = 0.5$ mA/V². Assuming that the device is operating

in the saturation region, what value of v_{GS} is required for $i_D = 3$ mA?

5.65. For the circuits shown in Figure P5.65, find the currents and voltages labeled. For each FET, $|V_{to}| = 2$ V and $I_{DSS} = 8$ mA.

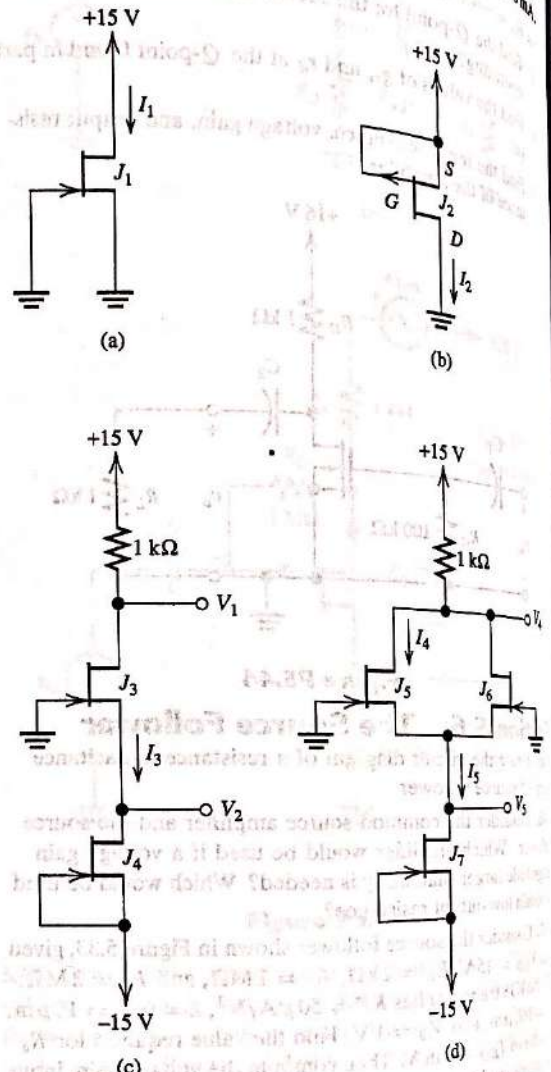


Figure P5.65

5.66. Find the values of I_{DQ} and V_{DSQ} for each of the circuits illustrated in Figure P5.66. Assume that $V_{to} = -4$ V and $I_{DSS} = 8$ mA for all FETs.

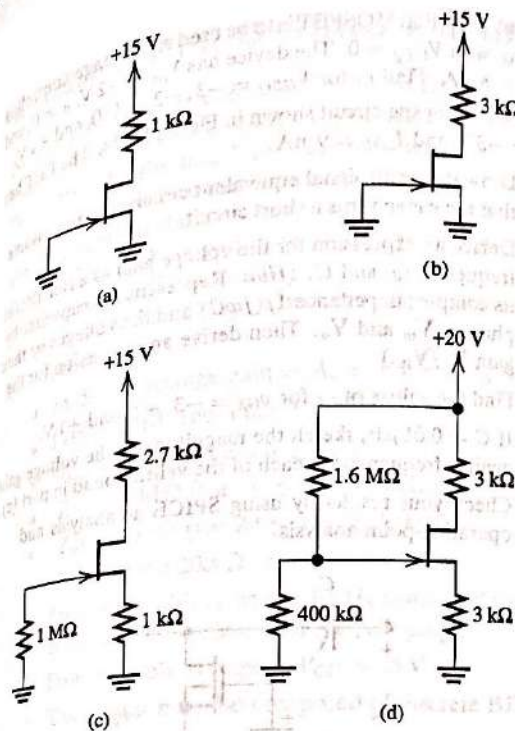


Figure P5.66

5.67. Find the value of R_S if $I_{DQ} = 4 \text{ mA}$ in the circuit of Figure P5.67. Assume that $V_{to} = -3 \text{ V}$, $I_{DSS} = 18 \text{ mA}$, and the circuit is operating in saturation. What is the largest value of R_D allowed if the operating point must remain in the saturation region?

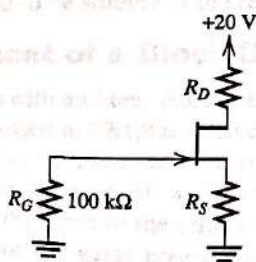


Figure P5.67

5.68. The FET of Figure P5.68 has $V_{to} = -2 \text{ V}$ and $I_{DSS} = 4 \text{ mA}$. If $I_{DQ} = 9 \text{ mA}$, find the value of R_2 , assuming that the device is operating in the saturation region. What is the largest value of R_D allowed if the operating point must remain in the saturation region?

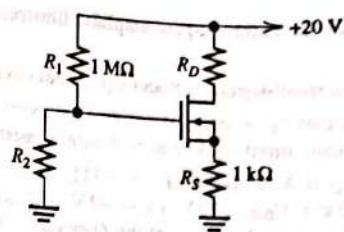


Figure P5.68

5.69. Repeat Problem 5.68 if the depletion MOSFET is replaced with an n -channel enhancement MOSFET having $V_{to} = 4 \text{ V}$ and $K = 1 \text{ mA/V}^2$.

5.70. Two identical JFETs are connected in parallel as shown in Figure P5.70. Each FET has the parameters g_m , I_{DSS} , and V_{to} . Find the parameters g_{m_e} , I_{DSS_e} , and V_{to_e} of a single JFET that is equivalent to the parallel combination.

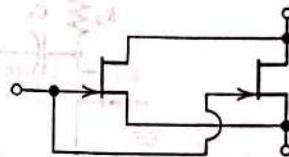


Figure P5.70

General Problems

5.71. Consider the three-stage amplifier shown in Figure P5.71. All of the FETs have $V_{to} = -3 \text{ V}$ and $I_{DSS} = 3 \text{ mA}$.

- What type (common-source or source follower) of amplifier is the J_1 stage? The J_2 stage? The J_3 stage?
- Find the Q -point drain current for each transistor. Find g_m for each transistor.
- Find midband values for the voltage gain, input resistance, and output resistance of the amplifier.

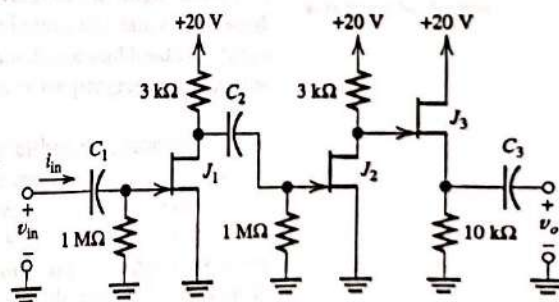


Figure P5.71 Three-stage RC-coupled JFET amplifier.

5.72. Consider the common-gate amplifier illustrated in Figure P5.72.

- Draw the small-signal midband equivalent circuit.
- Assume that $r_d = \infty$, and derive expressions for the voltage gain, input resistance, and output resistance.
- Find I_{DQ} if $R = 100 \Omega$, $R_S = 1 \text{ k}\Omega$, $R_D = 6.8 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, $V_{DD} = 20 \text{ V}$, $V_{io} = -2 \text{ V}$, and $I_{DSS} = 8 \text{ mA}$. Determine the value of g_m at the Q -point.
- Evaluate the expressions found in part (b).
- Find $v_o(t)$ if $v(t) = 0.1 \sin(2000\pi t)$.
- Is this amplifier inverting or noninverting? Would you classify the input resistance as high, moderate, or low compared with that of the common-source amplifier?

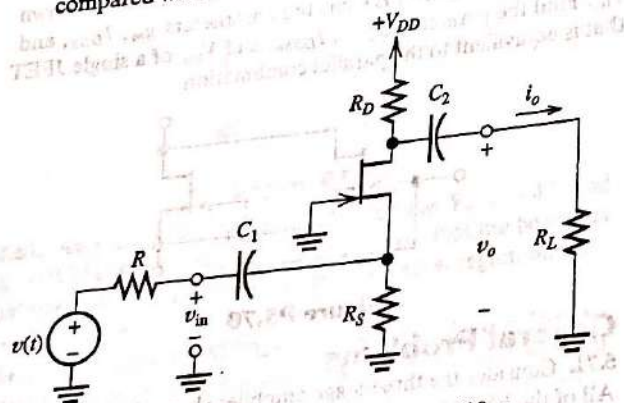


Figure P5.72 Common-gate amplifier.

5.73. A depletion MOSFET is to be used as a voltage-controlled resistor with $V_{DSQ} = 0$. The device has $V_{io} = -2 \text{ V}$, $\lambda = 0$, and $I_{DSS} = 8 \text{ mA}$. Find r_d for $V_{GSQ} = -3, -2, -1, 0$, and $+1 \text{ V}$.

5.74. Consider the circuit shown in Figure P5.74. The FET has $V_{io} = -3 \text{ V}$ and $I_{DSS} = 9 \text{ mA}$.

- Draw the small-signal equivalent circuit. Do not assume that the capacitor is a short circuit.
- Derive an expression for the voltage gain as a function of frequency, r_d , and C . (Hint: Represent the capacitor by its complex impedance $1/(j\omega C)$ and the voltages by their phasors V_{in} and V_o . Then derive an expression for the gain V_o/V_{in} .)
- Find the values of r_d for $v_{GS} = -3, -1$, and $+1 \text{ V}$.
- If $C = 0.01 \mu\text{F}$, sketch the magnitude of the voltage gain against frequency for each of the values found in part (c).
- Check your results by using SPICE ac analysis and operating-point analysis.

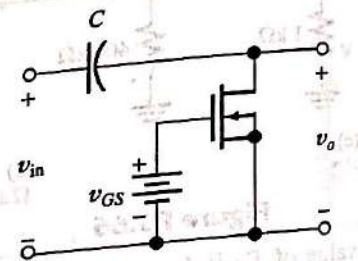


Figure P5.74

A DISCRETE MULTISTAGE AMPLIFIER

Now that we have become familiar with BJTs, FETs, biasing circuits, and basic single-stage amplifiers, we are ready to appreciate the design of a multistage amplifier. We will “look over the shoulder” of a designer who is in the process of designing a multistage amplifier intended for implementation in discrete form. Eventually, as a circuit designer, you will need to design integrated circuits; however, IC design is more difficult than discrete design. We need to walk before we run; later in the book, we will be ready to look at realistic IC designs.

We examine the design of a discrete multistage amplifier that is to meet the following specifications:

- Midband voltage gain $= A_v = 100 \pm 50\%$ (noninverting).
- Lower 3-dB frequency ≤ 20 Hz.
- Upper 3-dB frequency ≥ 20 kHz.
- $|Z_{in}| \geq 1 \text{ M}\Omega$ (for $20 \leq f \leq 20 \text{ kHz}$).
- $|Z_o| \leq 100 \Omega$ (for $20 \leq f \leq 20 \text{ kHz}$).
- The load is a $200\text{-}\Omega$ resistance.
- Output capability with a 1-kHz sinusoidal test signal must be at least 2.5-V peak without severe distortion (i.e., clipping).
- Power supply voltage is $V_{CC} = 15 \text{ V}$.
- The circuit must be composed of discrete BJTs, standard-value resistors, and capacitors.
- The amplifier must not allow dc current to flow through either the signal source or the load.

Do not be discouraged if this design problem seems to be difficult for you. Up till this point in the book, we have discussed only some of the issues that need to be addressed in this design. The main purpose here is for you to see how circuit designers do their work, to see how many of the concepts we have learned so far are useful, and to meet some issues that need to be studied in the remainder of the book.

Development of a Block Diagram

A design starts with an idea. Here, we decide to cascade several of the single-stage BJT amplifiers discussed in Chapter 4. Because a relatively high input impedance is needed, an emitter follower is used for the first stage. The output impedance and load resistance are relatively low, so we plan to reduce the resistance values as we progress through the amplifier from the input to the output.

To attain voltage gains greater than unity, we can use either common-emitter or common-base stages. Because the input impedance of the common-base stage is low, we decide to use common-emitter stages. To attain a noninverting gain, we will cascade two common-emitter stages, each having a gain of approximately -10 . We plan to use a partially unbypassed emitter resistance in each of the common-emitter stages so that the gain is less dependent on transistor parameters, as discussed in Section 4.7. Finally, to achieve low output impedance, we choose an emitter follower as the output stage. The block diagram of the circuit to be designed is illustrated in Figure AD2.1.

Eventually, as a circuit designer, you will need to design integrated circuits; however, IC design is more difficult than discrete design. We need to walk before we run; later in the book, we will be ready to look at realistic IC designs.

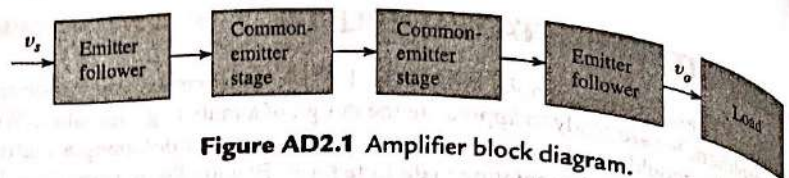


Figure AD2.1 Amplifier block diagram.

A first cut at the detailed circuit diagram is shown in Figure AD2.2, where we simply have cascaded the four stages with coupling capacitors (C_1 , C_2 , C_4 , C_6 , and C_7). Q_1 and Q_4 are emitter-follower stages, while Q_2 and Q_3 are common-emitter amplifiers with unbypassed emitter resistances (R_6 and R_{11}). Capacitors C_3 and C_5 are bypass capacitors. This first cut at the circuit diagram has been selected so that you can clearly see that it is composed of the amplifier stages displayed in Figures 4.36a and 4.37a. We will see that several of the resistors and capacitors can be eliminated.

Selecting a Transistor

We will use the 2N2222 transistor for all four stages. This is a popular device, and the evaluation versions of OrCAD software include models for it. For most of the design, we need to know only the β value of the transistor, which is typically in excess of 100 for the 2N2222. In general, better performance is obtained with higher values of β , and we will design conservatively by assuming that $\beta = 50$.

Data sheets for the 2N2222 (or the nearly identical 2N2222A and PN2222A devices) can be found at the Web sites www.fairchildsemi.com and www.diodes.com. (The online catalog at www.digikey.com is a good place to find current links to manufacturers of specific devices.)

The data sheet for the 2N2222A is also reproduced in Appendix B.

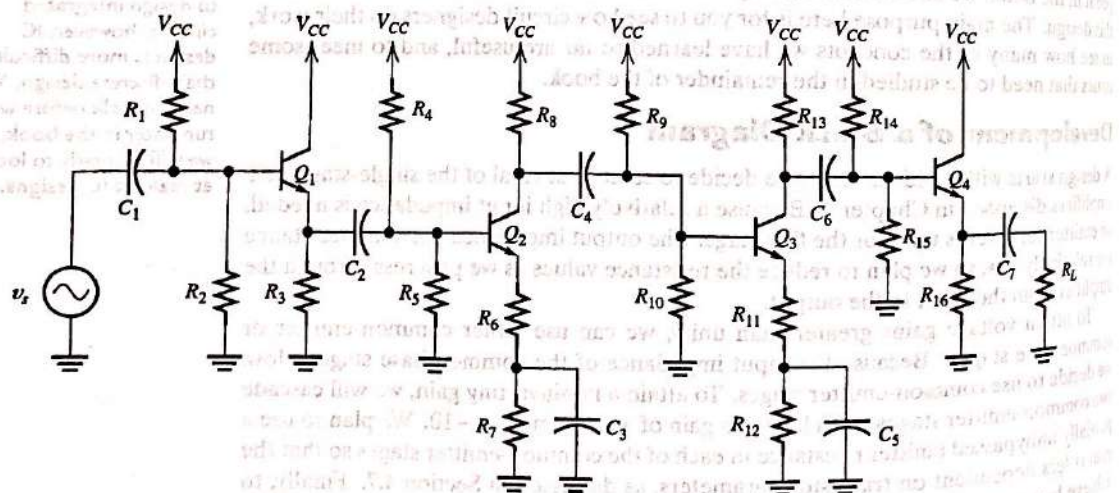


Figure AD2.2 Proposed circuit.

The Input Stage

First, let us consider the input stage (Q_1 and associated components). The resistors R_1 and R_2 act as a voltage divider, establishing the voltage at the base of Q_1 , which should be nearly independent of the base current of Q_1 . Because we need to have a 1-M Ω input impedance, we should select values for R_1 and R_2 of at least several megohms. Suppose we select

$$R_1 = 9.1 \text{ M}\Omega \text{ and } R_2 = 6.2 \text{ M}\Omega$$

These are standard 5%-tolerance values that are high enough to allow us to achieve our objective for Z_{in} . Furthermore, neglecting the base current, they establish a voltage of

$$V_{B1} = 15 \frac{R_2}{R_1 + R_2} \cong 6 \text{ V}$$

at the base of Q_1 . (Recall from Section 4.5 that in discrete bias circuits, we want to set the base voltage of the BJTs at one-third to one-half of the power-supply voltage.)

Also, we should design the bias circuit so that the currents through R_1 and R_2 are much greater than the base current. In our circuit, we have $I_{R2} = (6 \text{ V})/(6.2 \text{ M}\Omega) \cong 1 \mu\text{A}$. Thus, we should have the base bias current $I_{B1} \cong 0.1 \mu\text{A}$ or less, and then the emitter and collector bias currents are $I_{E1} \cong I_{C1} = \beta I_{B1} \cong 5 \mu\text{A}$. The dc voltage across R_3 is $V_{E1} = V_{B1} - V_{BE1} \cong 6 - 0.6 \cong 5.4 \text{ V}$. Hence, we need $R_3 = V_{E1}/I_{E1} = (5.4 \text{ V})/(5 \mu\text{A}) \cong 1 \text{ M}\Omega$.

Elimination of the Coupling Capacitor Between Q_1 and Q_2

Next, we consider the bias circuit for Q_2 , which consists of the four resistances R_4 , R_5 , R_6 , and R_7 . The function of R_4 and R_5 is to establish a voltage of about one-third of the power-supply voltage at the base of Q_2 . However, we have already designed the first stage to achieve a voltage of approximately 5.4 V at the emitter of Q_1 . Therefore, there is no need for the coupling capacitor C_2 and the resistors R_4 and R_5 . Accordingly, we will eliminate these components and connect the emitter of Q_1 directly to the base of Q_2 .

Bias for the Output Stage

Now let us consider the bias point required for the output stage. The specifications call for a peak output voltage swing of 2.5 V across a 200- Ω load. The collector-to-emitter bias voltage for Q_4 must be greater than 2.5 V, or else clipping due to saturation will occur before the desired output amplitude is reached. We will design for $V_{CE4} \cong 5 \text{ V}$.

The peak output current is required to be $(2.5 \text{ V})/(200 \Omega) = 12.5 \text{ mA}$. The bias current for Q_4 must be greater than the peak signal current, or else clipping will occur due to cutoff of Q_4 . Additional signal current will flow through R_{16} , and we need to allow some design margin. Thus, we decide to design for a bias current $I_{C4} \cong 30 \text{ mA}$. This can be achieved by choosing the voltage at the base of Q_4 to be about 10 V and $R_{16} = 300 \Omega$.

Furthermore, 10 V is a suitable bias voltage at the collector of Q_3 , so we can eliminate R_{14} , R_{15} , and C_6 and connect the base of Q_4 directly to the collector of Q_3 .

The revised circuit (including the component values that we have selected so far and the ones yet to be determined) is shown in Figure AD2.3.

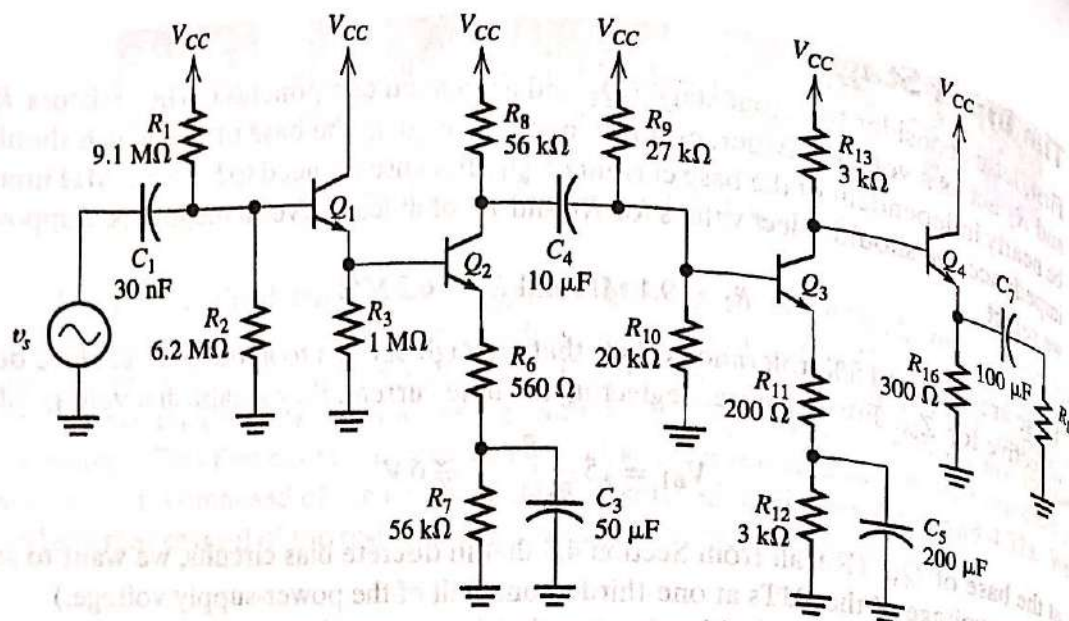


Figure AD2.3 Final circuit.

Impedance Levels

Notice that we have much larger currents and smaller resistances in the output stage than in the input stage. The ratio of the currents is $I_{C4}/I_{C1} = (30 \text{ mA})/(5 \mu\text{A}) \cong 6000$. Of course, low currents imply high impedances, and high currents imply low impedances. If we connect a low-impedance stage to the output of a high-impedance stage, the voltage gain will be reduced severely due to loading effects. Therefore, we plan to reduce resistances and increase the bias currents gradually from stage to stage. We need to increase the bias current by a factor of $\sqrt[3]{6000} \cong 18$ from one stage to the next. Thus, we choose the bias current of Q_2 to be 18 times higher than that of Q_1 , the bias current of Q_3 to be 18 times higher than that of Q_2 , etc. Corresponding bias resistances will decrease by a factor of approximately 18 from each stage to the next.

To summarize, we have decided to design for bias currents of

$$I_{C1} = 5 \mu\text{A}, \quad I_{C2} = 90 \mu\text{A}, \quad I_{C3} = 1.6 \text{ mA}, \quad \text{and} \quad I_{C4} = 30 \text{ mA}$$

and collector-to-emitter voltages of

$$V_{CE1} \cong 10 \text{ and } V_{CE2} \cong V_{CE3} \cong V_{CE4} \cong 5 \text{ V}$$

These bias points establish the following resistance values:

$$R_6 + R_7 = R_3/18 \cong 56 \text{ k}\Omega$$

$$R_8 \cong R_6 + R_7 = 56 \text{ k}\Omega$$

$$R_9 = R_1/(18 \times 18) \cong 27 \text{ k}\Omega$$

$$R_{10} = R_2/(18 \times 18) \cong 20 \text{ k}\Omega$$

$$R_{11} + R_{12} = (R_6 + R_7)/18 \cong 3 \text{ k}\Omega$$

$$R_{13} = R_{11} + R_{12} = 3 \text{ k}\Omega$$

Input Impedance of Stage Four

Using Equation (4.37), we compute the r_π value for Q_4 :

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{50(26 \text{ mV})}{30 \text{ mA}} = 43 \Omega$$

Stage four is an emitter follower similar to the circuit that we analyzed in Section 4.8. The effective load impedance is

$$R'_{L4} = R_L || R_{16} = 200 || 300 = 120 \Omega$$

Then, from Equation (4.60), we compute the impedance seen looking into the base of Q_4 :

$$Z_{it4} = r_{\pi 4} + (1 + \beta)R'_{L4} = 43 + (1 + 50)120 \cong 6200 \Omega$$

The effective load resistance for Q_3 is therefore

$$R'_{L3} = R_{13} || Z_{it4} = 3000 || 6200 \cong 2000 \Omega$$

From the equivalent-circuit analysis of Section 4.7, the voltage gain of stage 3 is $A_{v3} \cong -R'_{L3}/R_{11}$. Recall that we are designing for $A_{v3} \cong -10$. Hence, solving for R_{11} and substituting values, we obtain

$$R_{11} = -R'_{L3}/A_v \cong 2000/10 \cong 200 \Omega$$

Then, since biasing considerations required that $R_{11} + R_{12} \cong 3000 \Omega$, we can choose

$$R_{12} = 3 \text{ k}\Omega.$$

In a similar fashion, we obtain

$$R_6 = 510 \Omega \text{ and } R_7 = 56 \text{ k}\Omega$$

Selecting Values for the Capacitors

We have not discussed frequency response issues as yet. (They will be covered in Chapter 8.) However, we can anticipate that the coupling and bypass capacitors cause the gain to roll off at low frequencies. (See Section 1.10.) We will see that, as a general rule, the roll-off due to a given capacitor begins at roughly the frequency for which the capacitive impedance is equal to the resistance R seen looking back into the circuit to which the capacitor is connected. Mathematically, we have

$$R = \frac{1}{2\pi f C}$$

where R is the resistance seen by the capacitor and f is the frequency at which the roll-off begins. Solving for C , we obtain

$$C = \frac{1}{2\pi f R}$$

(AD2.1)

Because we have several coupling and bypass capacitors, each of which will tend to reduce the gain at low frequencies, we need to allow considerable design margin.

If we replace the signal source with its internal resistance (assumed to be zero), the resistance "seen" by C_1 is $0 + R_{in} = 1 \text{ M}\Omega$. Substituting into Equation (AD2.1), we get

$$C = \frac{1}{2\pi f C} = \frac{1}{2\pi(20)10^6} = 0.00795 \mu\text{F}$$

Allowing ample design margin and selecting a standard nominal value, we finally settle on

$$C_1 = 0.03 \mu\text{F}$$

Similarly, we estimate the values needed for the other capacitors as follows:

$$C_3 = 50 \mu\text{F}$$

$$C_4 = 10 \mu\text{F}$$

$$C_5 = 200 \mu\text{F}$$

$$C_7 = 100 \mu\text{F}$$

This completes our design. To verify that the desired specifications are met, we simulate the circuit with PSpice software. The schematic is stored in the file named FigAD2.3. We find, from the simulations, that all of the specifications are met.

Alternative Designs

In practice, design does not proceed smoothly. For example, on a first cut I did not allow enough bias current for Q_4 , and later I had to revise the values I selected. In the interest of saving space, I have presented the final design without detailing the missteps that invariably occur.

If the specifications had been different, we might not have been able to meet them with the circuit configuration we selected. For example, if the bandwidth had been required to be 1 MHz, our design would have failed. After you have studied Chapter 8 and gained some experience, you will anticipate that BJTs biased at very small currents (like Q_1 and Q_2) have poor high-frequency response, and you will look for a different circuit configuration.

Digital Logic Circuits

So far, we have mainly considered analog circuits, such as amplifiers and waveshapers. In this chapter, we review some basic digital concepts and consider digital circuits at the device level.

A group of prepackaged ICs based on the same fabrication technology and designed to be mutually compatible is called a **logic family**. There are several IC families in current use for each of these technologies: **transistor-transistor logic (TTL)**, **complementary metal-oxide semiconductor logic (CMOS)**, and **emitter-coupled logic (ECL)**. CMOS is the most important technology for future systems and is the one on which we will concentrate.

Many standard logic functions (such as logic gates, shift registers, digital adders, and so forth) are available in a given logic family. Earlier digital systems were constructed by interconnecting these standard ICs on a printed-circuit board. However, a better approach is **application-specific integrated circuits (ASICs)**, which contain nearly all of the digital and analog circuits and their interconnections for a given application on a single chip. ASICs are the best way to design complex electronic products, such as cellular phones, personal digital assistants, and GPS receivers, that have small size, high capability, and reasonable cost.

The advent of ASICs has made it even more important for electronic-circuit designers to be knowledgeable about the internal design of digital ICs. The goal of this chapter is to give you much of the basic knowledge that you will need.

6

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6.1 BASIC CONCEPTS

We assume that you are somewhat familiar with digital systems from other courses. However, in this section, we will review the basic principles needed later in the chapter.

Logic Variables and Digital Words

In digital systems, information is represented by **logic variables** that can assume values of logic 1 or logic 0. The logic value 1 is also called **high**, **true**, or **on**. Logic 0 is also called **low**, **false**, or **off**. Signals in logic systems switch between high and low as the information being represented changes. We often denote logic variables by uppercase letters such as A , B , and C .

A single binary digit (0 or 1), called a **bit**, represents a very small amount of information. For example, a logic variable R could be used to represent whether or not it is raining in a particular location (say, $R = 1$ if it is raining, and $R = 0$ if it is not raining).

In order to represent more information, we resort to using groups of logic variables, called **digital words**. For example, the word RWS could be formed in which R represents rain, W is 1 if the wind velocity is greater than 15 miles per hour, and W is 0 if there is less wind. S could be 1 for sunny conditions and 0 for cloudy conditions. Then the digital word 110 would tell us that it is rainy, windy, and cloudy. A **byte** is a word consisting of eight bits, and a **nibble** is a four-bit word.

The AND Gate

One important logic function is called the **AND operation**. The AND operation on two logic variables, A and B , is represented as AB , read as "A and B." A **truth table** is simply a listing of all of the inputs to a logic operation, together with the corresponding outputs. The truth table for the AND operation of two variables is displayed in Figure 6.1a. Notice that AB is 1 only if A and B are both 1. For the AND operation, we can write the following relations:

A	B	$C = AB$
0	0	0
0	1	0
1	0	0
1	1	1

(a) Truth table



(b) Symbol for two-input AND gate



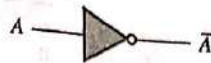
(c) Symbol for three-input AND gate

Figure 6.1
AND operation.

Figure 6.2
NOT operation.

A	$\bar{A}$
0	1
1	0

(a) Truth table



(b) Symbol for an inverter

$$AA = A$$

$$A1 = A$$

$$A0 = 0$$

$$AB = BA$$

$$A(BC) = (AB)C = ABC$$

Circuit symbols for AND gates (i.e., circuits that produce an output equal to the result of the AND operation for all of the inputs) are illustrated in Figures 6.1b and 6.1c.

The Logic Inverter

The NOT operation on a logic variable is represented by placing a bar over the symbol for the variable. The symbol $\bar{A}$ is read as "not A" or as "A inverse." If A is 0, $\bar{A}$ is 1. Similarly, if A is 1, $\bar{A}$ is 0.

Circuits that perform the NOT operation are called **inverters**. The truth table and circuit symbol for an inverter are displayed in Figure 6.2.

The following results can be established for the NOT operation:

$$A\bar{A} = 0$$

$$\bar{\bar{A}} = A$$

Key relationships for the AND operation.

The OR Gate

The OR operation applied to logic variables is written as $A + B$, which is read as "A or B." The truth table for the OR operation and the circuit symbol for the OR gate are shown in Figure 6.3. Notice that $A + B$ is 1 if A or B (or both) are 1. For the OR operation, we have

$$(A + B) + C = A + (B + C) = A + B + C$$

$$A(B + C) = AB + AC$$

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + \bar{A} = 1$$

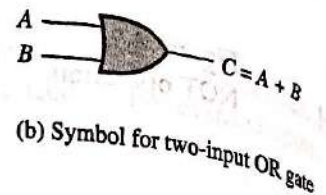
$$A + A = A$$

Key relationships for the OR operation.

A	B	$C = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Figure 6.3
OR operation.

(a) Truth table



Boolean Algebra

The basic logical operations in Boolean algebra are AND, OR, and NOT.

Using Boolean algebra, one can often find alternative implementations for a given logic function.

Although we use the addition sign (+) to represent the OR operation, manipulation of logic variables by the AND, OR, and NOT operations is different from ordinary algebra. The mathematical theory of logic variables and operations is called **Boolean algebra**, named for the mathematician George Boole.

Using Boolean algebra, one can often find alternative implementations for a given logic function. Methods are available for finding the implementation using the fewest gates of a given type. We will not consider minimization techniques, because our main concern is with transistor-level design. We leave digital-system design considerations (i.e., the best ways to connect digital building blocks together) for other courses.

NAND, NOR, and XOR Gates

Some additional logic gates are shown in Figure 6.4. The NAND gate is equivalent to an AND gate followed by an inverter. Notice that the symbol is the same as that for an AND gate, but with a circle at the output terminal to indicate that the output has been inverted after the AND operation. Similarly, the NOR gate is equivalent to an OR gate followed by an inverter.

The *exclusive-OR* (XOR) operation for two logic variables A and B is represented by $A \oplus B$ and is defined by

$$0 \oplus 0 = 0$$

$$1 \oplus 0 = 1$$

$$0 \oplus 1 = 1$$

$$1 \oplus 1 = 0$$

Notice that the XOR operation yields 1 if A is 1 or if B is 1, but yields 0 if both A and B are 1. The XOR operation is also known as **modulo-two addition**.

Definition of the XOR operation.

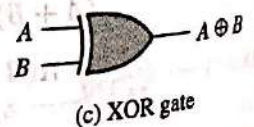


Figure 6.4 Additional logic-gate symbols.

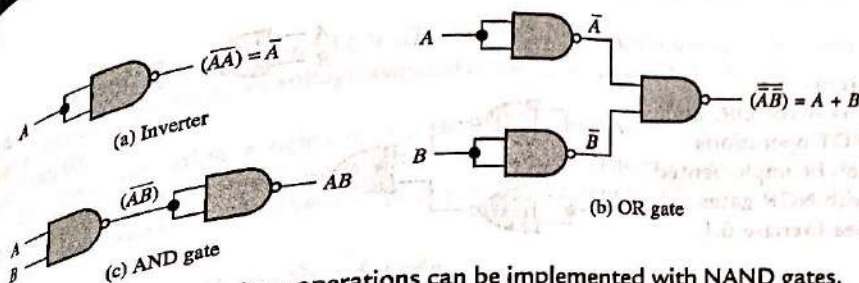


Figure 6.5 Basic Boolean operations can be implemented with NAND gates. Therefore, any Boolean function can be implemented by the use of NAND gates alone.

A buffer has a single input and produces an output with the same value as the input. (Specially designed buffers are used to provide large currents when a logic signal must be applied to a low-impedance load such as a large capacitance.)

The **equivalence gate** produces a high output only if both inputs have the same value. In effect, it is an XOR followed by an inverter, as the symbol of Figure 6.4e implies.

Logical Sufficiency of NAND Gates and of NOR Gates

Two important results in Boolean algebra are De Morgan's laws, which state that

$$AB = \overline{\overline{A} + \overline{B}} \quad (6.1)$$

Key Equations: De Morgan's Laws.

and

$$A + B = \overline{\overline{A} \overline{B}} \quad (6.2)$$

Another way to express these laws is as follows: If the variables in a logic expression are replaced by their inverses, and if the AND operation is replaced by OR, the OR operation is replaced by AND, and the expression is inverted, the resulting logic expression yields the same values as before the changes.

If the inputs to a NAND are tied together, an inverter results. This is true because

$$\overline{(AA)} = \overline{A}$$

Also, as shown by Equation (6.2), the OR operation can be realized by inverting the input variables and combining the results in a NAND gate. This is illustrated in Figure 6.5, in which the inverters are formed from NAND gates. Finally, a NAND followed by an inverter results in an AND gate. Since the basic logic functions (AND, OR, and NOT) can be realized by using only NAND gates, we conclude that NAND gates are sufficient to realize any combinational logic function.

Similarly, NOR gates are sufficient to realize any combinational logic function.

If the variables in a logic expression are replaced by their inverses, and if the AND operation is replaced by OR, the OR operation is replaced by AND, and the expression is inverted, the resulting logic expression yields the same values as before the changes.

... NAND gates are sufficient to realize any combinational logic function.

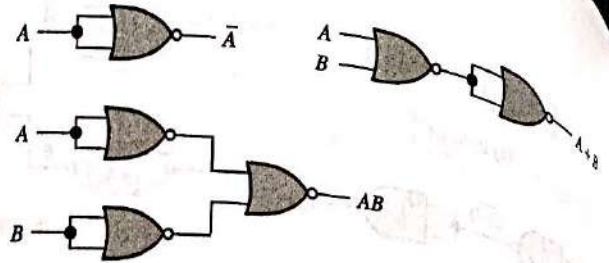
... NOR gates are sufficient to realize any combinational logic function.

EXERCISE

6.1 Show how to realize the AND, OR, and NOT functions using only NOR gates.

Answer See Figure 6.6.

Figure 6.6
The AND, OR, and NOT operations can be implemented with NOR gates. See Exercise 6.1.



EXERCISE

6.2 Write the truth table for each of the logic circuits shown in Figure 6.7. Then find an equivalent gate for each circuit.

Answer Each circuit is the equivalent of an exclusive-OR gate.

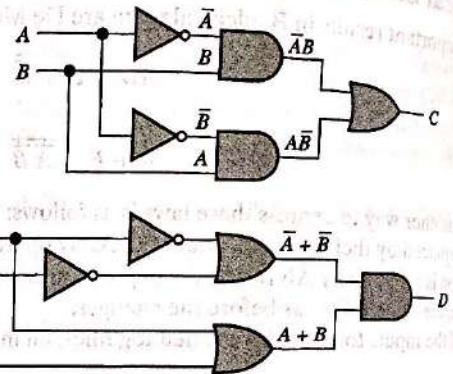


Figure 6.7
Circuits for Exercise 6.2.

6.2 ELECTRICAL SPECIFICATIONS FOR LOGIC GATES

In the last section, we considered the ideal operation of logic gates, concentrating on the Boolean operations performed on the input logic values. In this section, we consider specifications for the actual voltages and currents in logic gates. We reference most of our discussion to the inverter, but the concepts apply to other gates as well.

Logic Ranges

For a given logic family, one range of output voltages represents logic 1, and another range of voltages represents logic 0. For example, the output voltage ranges are illustrated in Figure 6.8 for a particular family of TTL circuits. Any output voltage higher than 3.0 V represents logic 1, and any voltage lower than 0.5 V represents logic 0. Voltages in the

For a given logic family, one range of output voltages represents logic 1, and another range of voltages represents logic 0. For proper operation, a logic circuit only needs to produce a voltage somewhere in the correct range.

transition region between 0.5 and 3.0 V occur only for very short intervals, when the logic value changes. The ranges of voltage assigned to logic 1 and logic 0 are different for each logic family.

For proper operation, a logic circuit only needs to produce a voltage somewhere in the correct range. Thus, component values in digital circuits do not need to be as precise as in analog circuits, for which each amplitude has a different significance.

Positive Versus Negative Logic

Usually, the higher amplitude in a binary system represents 1, and the lower amplitude represents 0. In this case, we say that we have **positive logic**. On the other hand, it is possible to represent 1 by the lower amplitude and 0 by the higher amplitude, resulting in **negative logic**. Unless stated otherwise, we assume positive logic throughout this book.

... component values in digital circuits do not need to be as precise as in analog circuits...

In positive logic, the higher amplitude in a binary system represents 1, and the lower amplitude range represents 0.

Transfer Characteristics of Logic Inverters

Suppose that we have an inverter operating from a power-supply voltage of V_{SS} , as shown in Figure 6.9a. The transfer characteristic of the inverter is a plot of the output voltage v_O versus the input voltage v_I . The transfer characteristics for an ideal inverter and for a real inverter are shown in Figure 6.9b. The ideal inverter recognizes any input voltage less than half of the supply voltage as logic 0 and produces an output voltage equal to the supply voltage V_{SS} . Similarly, any voltage higher than $V_{SS}/2$ is recognized as logic 1, and the output voltage is zero. On the other hand, the output voltage of a real inverter makes a more gradual transition as the input voltage is raised from zero to V_{SS} .

Noise Margins

Noise consists of undesired fluctuations in the actual voltage of a logic signal. The fluctuations are caused by power-supply-voltage variations or stray capacitive coupling of other rapidly changing signals. Noise is virtually unavoidable in electronic systems.

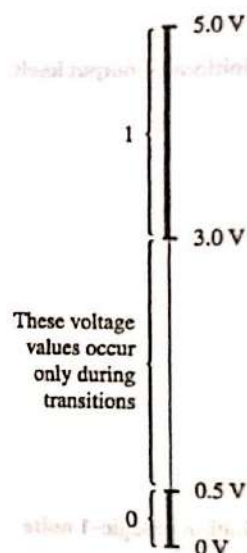


Figure 6.8 Output voltage ranges for the 7400 ALS TTL logic family.

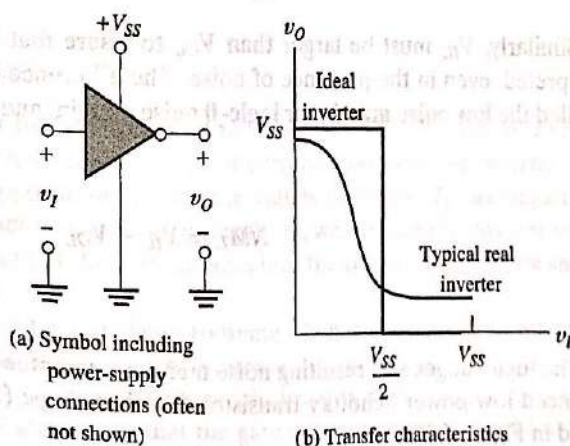


Figure 6.9 Logic inverter.

If the output voltage levels of an inverter (or other logic gate) are close together, it is easy for noise to cause an error in the logic value. To avoid this problem, the output voltage levels should be as far apart as possible. Thus, the ideal logic inverter characteristic of Figure 6.9b has an output voltage equal to the supply voltage for logic 1 and equal to 0 V for logic 0.

Also, because of possible noise added to the input signals, it is desirable for the inverter to accept wide ranges of input voltages as valid logic variables. Notice, in the characteristic of Figure 6.9b, that the ideal inverter accepts the voltage range from zero to $V_{SS}/2$ as logic 0 and accepts voltages from $V_{SS}/2$ to V_{SS} as logic 1.

Manufacturers of logic gates specify values for the following input and output voltages:

- V_{IL} is the highest input voltage guaranteed to be accepted as logic 0.
- V_{IH} is the lowest input voltage guaranteed to be accepted as logic 1.
- V_{OL} is the highest logic-0 output voltage produced (provided that the input voltages are higher than V_{IH} or lower than V_{IL}).
- V_{OH} is the lowest logic-1 output voltage produced (provided that the input voltages are lower than V_{IL} or higher than V_{IH}).

It is important for V_{IH} to be less than V_{OH} , because we want the lowest output voltage for logic 1 to be properly interpreted by gates connected to the output of the inverter, even when some noise has been added. The difference between these voltages is called the **high noise margin**, or **logic-1 noise margin**, which is given by

$$NM_H = V_{OH} - V_{IH} \quad (6.3)$$

Similarly, V_{IL} must be larger than V_{OL} to insure that logic-0 outputs are properly interpreted, even in the presence of noise. The difference between the logic-0 voltages is called the **low noise margin**, or **logic-0 noise margin**, and is given by

$$NM_L = V_{IL} - V_{OL} \quad (6.4)$$

The logic ranges and resulting noise margins guaranteed for a logic family known as advanced low-power Schottky transistor-transistor logic (ALS TTL) circuits are illustrated in Figure 6.10.

Definitions of output levels.

Definition of logic-1 noise margin.

Large noise margins are important in avoiding problems associated with noise in logic circuits.

Definition of logic-0 noise margin.

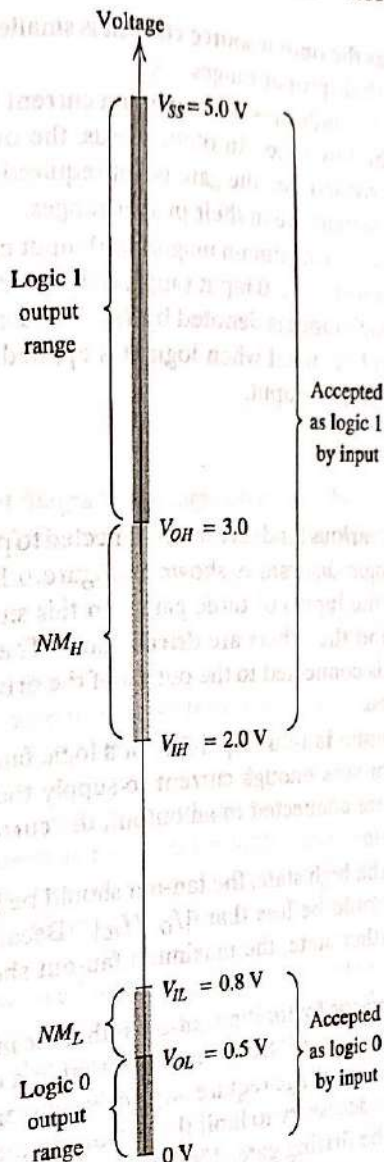


Figure 6.10
Input and output
voltage ranges for
the 7400 ALS TTL
logic family oper-
ated from a +5-V
supply.

Input and Output Currents

The reference directions for the input and output currents of an inverter are shown in Figure 6.11. Note that the reference directions for currents point into the inverter. If the actual currents are in the opposite directions, the values of I_I and I_O are negative. If current flows out of the output terminal (I_O is negative), we say that the inverter sources the current. On the other hand, if the current flows into the output terminal, we say that the output sinks the current.

The current that the output is capable of sourcing when it is high is denoted by I_{OH} . (I_{OH} has a negative value due to the choice of reference direction.) As the output is called upon to source more current, the output voltage falls because of the output resistance of the gate. The manufacturer guarantees that the gate output voltage will not fall below

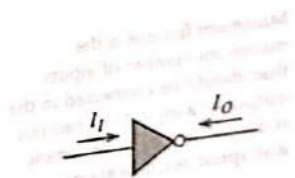


Figure 6.11 Reference
directions for input and
output currents. (I_O has a
negative value if the output
sources current.)

V_{OH} , as long as the output source current is smaller in magnitude than I_{OH} and the input signals are in their proper ranges.

Similarly, I_{OL} indicates the maximum current that the output can sink when the gate output is in the low state. In other words, the output voltage is guaranteed to remain below V_{OL} , provided that the gate is not required to sink a current greater than I_{OL} and that the input signals are in their proper ranges.

The worst-case (maximum magnitude) input current, provided that the input voltage is in the acceptable logic-0 input range, is denoted by I_{IL} . Similarly, the worst-case input current for a high input is denoted by I_{IH} . For some types of logic circuits, current flows out of the input terminal when logic 0 is applied. Current usually flows into the input terminal for a logic-1 input.

Fan-Out

Logic gates of various kinds are interconnected to perform Boolean operations. A portion of a typical logic diagram is shown in Figure 6.12. Notice that the inverter output is connected to the inputs of three gates. In this situation, we say that the inverter is the **driving gate** and the others are **driven gates**. The **fan-out** for a driver is the number of input terminals connected to the output of the driver. For the inverter in Figure 6.12, the fan-out is three.

If the fan-out is too high, the current required exceeds the capability of the driving gate.

The maximum fan-out capability of a logic family is limited because the gate output must source or sink enough current to supply the inputs of all the driven gates. If too many inputs are connected to an output, the current required exceeds the capability of the driving gate.

Thus, for the high state, the fan-out should be less than $|I_{OH}/I_{IH}|$. For the low state, the fan-out should be less than $|I_{OL}/I_{IL}|$. Because we require the circuit to function properly in either state, the maximum fan-out should be less than the smaller of these ratios.

Another reason for limiting fan-out is that the input of a logic gate presents a capacitive load to the driving gate. Because the current in a capacitance is given by $i = C(dv/dt)$, fast transitions in voltage require large drive currents. In systems for which fast switching is desired, it is necessary to limit the fan-out so that the current required remains within the limits of the driving gate. Usually, manufacturers suggest a maximum fan-out to be used with a particular logic family. In designing an ASIC, we need to keep the problems associated with fan-out in mind.

Maximum fan-out is the maximum number of inputs that should be connected to the output of a logic gate. Fan-out is determined by drive current and speed considerations.

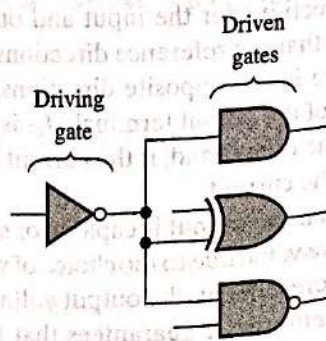
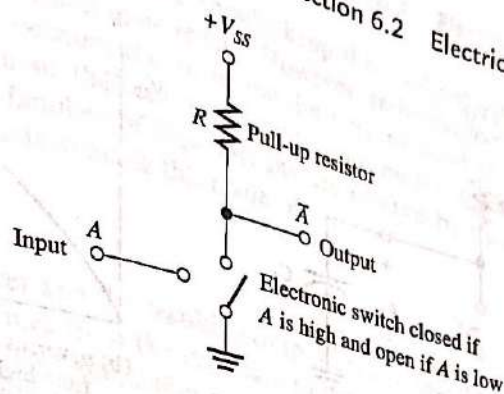


Figure 6.12
Portion of a logic circuit. The inverter has a fan-out of 3 (i.e., the inverter drives 3 inputs).

Figure 6.13
Simplified circuit
for a logic inverter.



Power Considerations

Figure 6.13 shows the simplified circuit diagram of a logic inverter. The electronic switch is open if the input signal A is low, and the switch is closed if the input is high. With the switch open, there is no voltage drop across R , and the output voltage is equal to the supply voltage. Thus, if the input is low, the output is high. Similarly, if A is high, the switch is closed, and the output voltage is zero. (In Chapters 4 and 5, we learned how to implement electronic switches with transistors.)

Notice that if the switch is closed, current is drawn from the power supply. The power delivered by the power supply when the logic levels are constant is called the **static power** or **quiescent power**. For this particular circuit, static power is consumed in the low state, but in the high state the static power is zero (provided that the load is an open circuit). For some logic technologies, static power is required for both states, but the value can be different for the high state than for the low state. Static power requirements range from less than a microwatt to nearly 100 milliwatts per gate for logic technologies in current use.

In the design of a digital system, we need to estimate the requirements for the power supply. In the case of an ASIC, power dissipation is important because the temperature of the chip must remain within certain bounds. A worst-case estimate of the total static power of a chip can be obtained by assuming that all gates are in the maximum power state. However, if we have good reason to assume that only a fraction of the gates will be in the high power state at any time, we can reduce our estimate of static power requirements accordingly.

As long as other system specifications can be met, we want to design logic circuits for minimum power dissipation. This leads to a lower cost for the power supply, a lower operating temperature, resulting in higher reliability, and less cost for heat sinks and forced ventilation.

Dynamic Power Dissipation

Often, the output of a gate must drive a significant load capacitance associated with the input circuits of the driven gates and with the wiring. Such a load capacitance is illustrated in Figure 6.14a. Suppose that the input logic level A has been high and that it switches low at $t = 0$. The resulting output voltage is shown in Figure 6.14b. Because the switch is closed before $t = 0$, the capacitor voltage starts at zero and increases toward V_{ss} . (In theory, the output voltage reaches V_{ss} after the switch is opened. Eventually, the output voltage reaches V_{ss} . (In theory, the

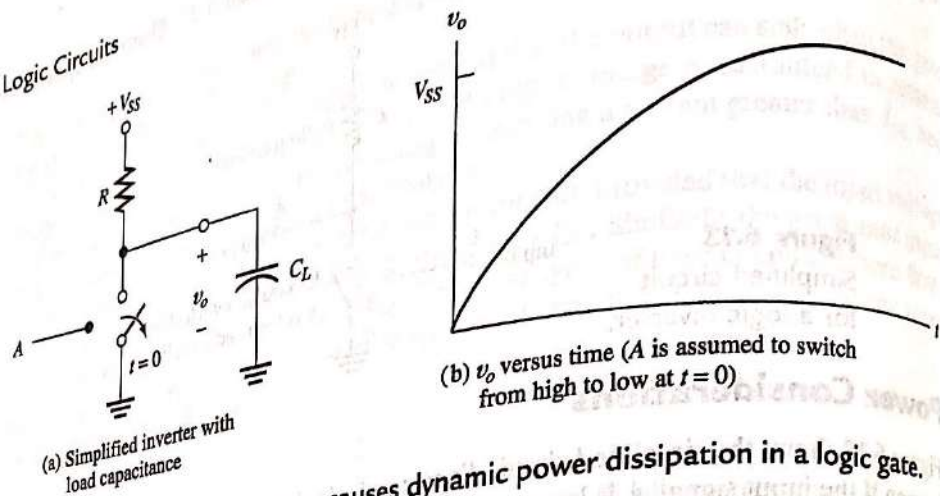


Figure 6.14 Load capacitance causes dynamic power dissipation in a logic gate. capacitor does not reach V_{SS} , but only approaches it. However, for practical purposes, the capacitor voltage can be assumed to have reached V_{SS} after about five time constants.) The resistor is called a **pull-up resistor**, because it “pulls the output voltage up.” The resulting charge stored on the capacitor is given by

$$Q = C_L V_{SS} \quad (6.5)$$

This charge must be provided by the power supply. The energy that is delivered is the product of the charge and the voltage:

$$E = C_L V_{SS}^2 \quad (6.6)$$

Half of this energy is dissipated in the resistor R and half is stored in the capacitor.

When the input logic signal goes high, the electronic switch closes, discharging the capacitor. In practice, the electronic switch behaves as a variable resistance that takes a short time interval to change from an open circuit to a short circuit. The energy stored in the capacitor is dissipated in the switch resistance as heat. Thus, in each switching cycle of the inverter from low to high and back to low, a quantity of energy given by Equation (6.6) is dissipated as heat in the internal circuits of the gate. If the output of the inverter cycles at a frequency f , the power dissipated is

$$P_{\text{dynamic}} = f C_L (V_{SS})^2 \quad (6.7)$$

This power is called **dynamic power dissipation**, because it occurs only when the output cycles between states.

Dynamic power dissipation is not a severe problem in low-speed logic circuits such as we might find in a cardiac pacemaker or in a watch, because the frequencies are at most only several tens of kilohertz. On the other hand, a high-speed computer or communication system can have logic signals that cycle in excess of one gigahertz, and then dynamic power dissipation is a very significant problem.

Key equation for dynamic power.

To reduce dynamic power dissipation, we should keep the load capacitance small and restrict the voltage swing between logic levels. However, reducing the logic swing increases susceptibility to noise, because the noise margins become smaller. Thus, compromise is necessary, and, of course, the best trade-off depends on the application. For this and other reasons, several families of logic circuits are offered by manufacturers. Similarly, the ASIC designer needs to make this trade-off.

Propagation Delay

The input pulse to a logic inverter and the resulting output are displayed in Figure 6.15. Notice that the input pulse changes from the low state to the high state gradually. The input signals are provided by other circuits that must drive the input capacitance of the inverter, so instantaneous changes in input voltage do not occur in practice.

The **rise time** t_r of the input signal is defined as the interval between the point at which 10% of the transition has been made, up to the 90% point. This is illustrated in Figure 6.15. The **fall time** t_f of the input pulse is defined in a similar fashion for the transition from high to low. Rise and fall times are defined analogously for transitions of the output signal.

The output transitions are delayed compared with the corresponding input transitions. This is called **propagation delay**, and it can have a different value for the transition from high to low than for the opposite transition. As indicated in the figure, t_{PHL} is the delay

To reduce dynamic power dissipation, we should keep the load capacitance small and restrict the voltage swing between logic levels.

Logic circuits consume power that is converted into heat. Power dissipation can be divided into static and dynamic components.

The rise time t_r of the input signal is defined as the interval between the point at which 10% of the transition has been made, up to the 90% point.

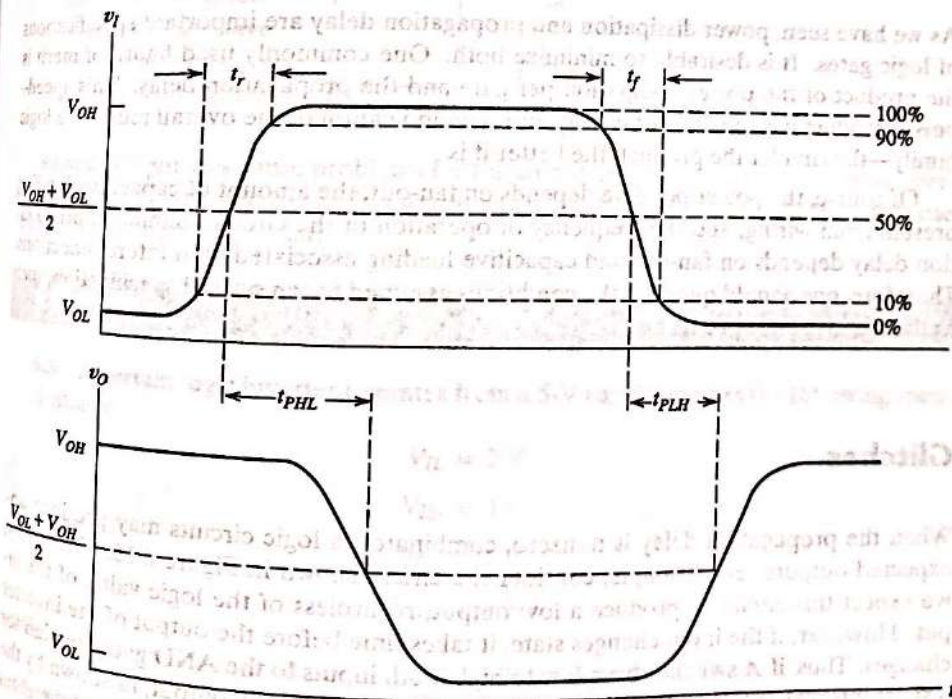


Figure 6.15 Input pulse and output of a typical inverter.

t_{PHL} is the delay measured between the 50% points of the transitions for the high-to-low transition of the output. Similarly, t_{PLH} is the propagation delay for the low-to-high transition of the output signal.

measured between the 50% points of the transitions for the high-to-low transition of the output. Similarly, t_{PLH} is the propagation delay for the low-to-high transition of the output signal. Manufacturers sometimes specify the *average* propagation delay, which is given by

$$t_{PD} = \frac{t_{PHL} + t_{PLH}}{2} \quad (6.8)$$

Propagation delays range upward from a fraction of a nanosecond for logic technologies in current use.

Of course, it is desirable to minimize propagation delay if high-frequency operation is required. When designing digital systems consisting of premanufactured logic gates, we select a logic family with the desired speed (i.e., with small enough propagation delays). Then we design the mechanical layout to minimize wiring capacitance. For an ASIC, in addition to layout, the designer has other options (such as transistor sizes) that affect propagation delay.

Speed-Power Product

As we have seen, power dissipation and propagation delay are important specifications of logic gates. It is desirable to minimize both. One commonly used figure of merit is the product of the power dissipation per gate and the propagation delay. This **speed-power product** has the units of energy and is an indication of the overall merit of a logic family—the smaller the product, the better it is.

Of course, the power per gate depends on fan-out, the amount of capacitive loading present from wiring, and the frequency of operation of the circuit. Similarly, propagation delay depends on fan-out and capacitive loading associated with interconnections. Therefore, one should question the conditions assumed for an overall specification, such as the speed-power product.

Glitches

When the propagation delay is nonzero, combinatorial logic circuits may produce unexpected outputs. For example, consider the circuit shown in Figure 6.16. Ordinarily, we expect this circuit to produce a low output, regardless of the logic value of the input. However, if the input changes state, it takes time before the output of the inverter changes. Thus, if A switches from low to high, both inputs to the AND gate are high for a short interval. This condition leads to a short high pulse at the output, as shown by the waveforms in Figure 6.16. Such an output caused by the propagation delay of the gates in a system is called a **glitch**.

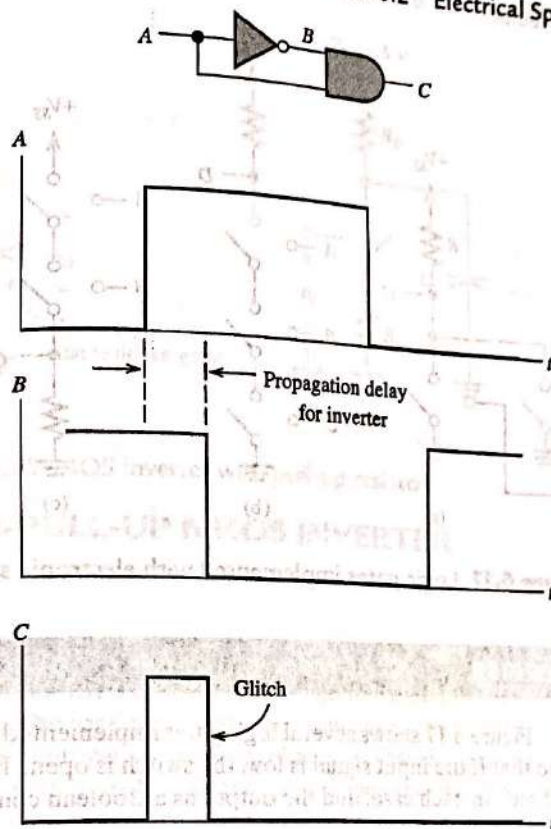


Figure 6.16
A glitch in the output of the AND gate caused by propagation delay in the inverter. Note that we have assumed zero delay for the AND gate.

Sometimes glitches cause problems for the circuit designer, because the circuit operates in a manner different from what was intended. Other times, we make deliberate use of glitches in designing a circuit.

EXERCISE

6.3 A certain logic inverter operates from a 5-V supply and has the following specifications:

$$V_{IL} = 2 \text{ V}$$

$$V_{IH} = 4 \text{ V}$$

$$V_{OL} = 1 \text{ V}$$

$$V_{OH} = 4.5 \text{ V}$$

Find values for the logic-0 noise margin and the logic-1 noise margin.

Answer $NM_H = 0.5 \text{ V}$ and $NM_L = 1 \text{ V}$.

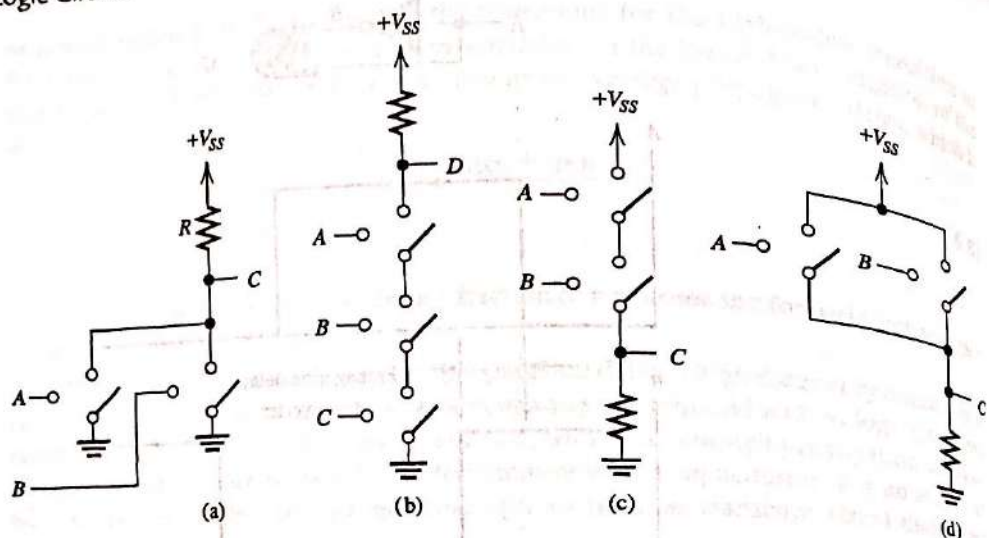


Figure 6.17 Logic gates implemented with electronic switches. See Exercise 6.4.

EXERCISE

6.4 Figure 6.17 shows several logic gates implemented with electronic switches. Assume that if the input signal is low, the switch is open. If the input is high, the switch is closed. In each case, find the output as a Boolean combination of the inputs.

Answer (a) $C = \overline{A + B}$; (b) $D = \overline{ABC}$; (c) $C = AB$; (d) $C = A + B$.

EXERCISE

6.5 A logic inverter switches between high and low at a frequency of 100 MHz. The power-supply voltage is 5 V and the output levels are 5 V and 0 V. The inverter drives a 2-pF load capacitance. Find the dynamic power dissipation.

Answer $P_{\text{dynamic}} = 5 \text{ mW}$.

EXERCISE

6.6 A certain computer chip contains 50,000 gates that have zero static power dissipation. Under worst-case conditions, the output of each gate cycles at 200 MHz. The total allowable dynamic power dissipation for the chip is 10 W. The supply voltage is $V_{SS} = 5 \text{ V}$. Determine the load capacitance allowed for each gate.

Answer $C_L = 40 \text{ fF} = 40 \times 10^{-15} \text{ F}$.

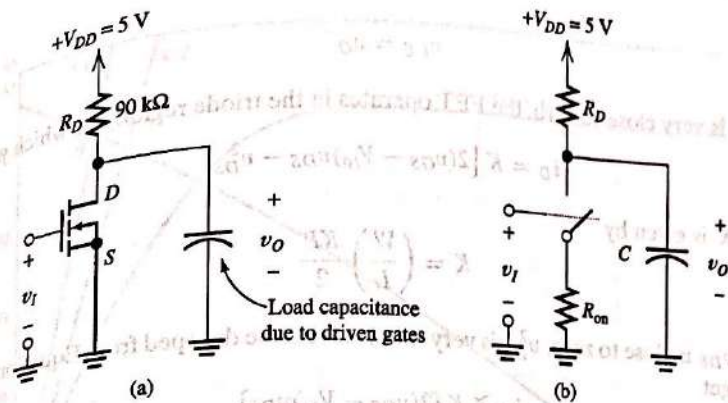


Figure 6.18 MOS inverter with pull-up resistor.

6.3 THE RESISTOR-PULL-UP NMOS INVERTER

Basic Operation

As a start toward understanding digital MOS circuits, we discuss the simple inverter circuit illustrated in Figure 6.18a. The transistor is an n -channel enhancement MOSFET with a threshold voltage V_{to} . The load represents the input capacitance of driven gates. Figure 6.18b shows a simplified equivalent circuit in which the NMOS transistor has been replaced by a switch in series with a small resistance R_{on} . When the input voltage is low, the NMOS is in cutoff, the switch is open, and the load capacitance is charged through the pull-up resistor R_D . When the input voltage is high, the output voltage eventually reaches the supply voltage V_{DD} . Thus, the output voltage in the high state is

$$V_{OH} = V_{DD} \quad (6.9)$$

On the other hand, when the input voltage is high ($v_I = V_{DD}$), the NMOS conducts, and the switch is closed, discharging the load capacitance so that the output voltage falls, eventually reaching a value given by

$$V_{OL} = V_{DD} \frac{R_{on}}{R_D + R_{on}} \quad (6.10)$$

We want V_{OL} to be very close to zero in order to maximize the noise margins of the inverter. Thus, we design the resistor-pull-up NMOS inverter so that the on resistance of the FET (R_{on}) is much smaller than the pull-up resistance R_D .

The On Resistance of the NMOS Transistor

Let us now consider how the on resistance is related to the NMOS parameters. First, notice that the drain-to-source voltage of the FET is equal to the output voltage and that the gate-to-source voltage is equal to the input voltage; that is,

$$v_{GS} = v_I \quad (6.11)$$

... we design the resistor-pull-up NMOS inverter so that the on resistance of the FET (R_{on}) is much smaller than the pull-up resistance R_D .

and

$$v_{DS} = v_O \quad (6.12)$$

When v_O is very close to zero, the FET operates in the triode region, for which we have

$$i_D = K [2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] \quad (6.13)$$

in which K is given by

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} \quad (6.14)$$

Because v_{DS} is close to zero, v_{DS}^2 is very small and can be dropped from Equation (6.13). Then we get

$$i_D \cong K [2(v_{GS} - V_{to})v_{DS}]$$

The on resistance of the transistor is

$$R_{on} = \frac{v_{DS}}{i_D} = \frac{1}{2K(v_{GS} - V_{to})} = \frac{1}{2K(v_I - V_{to})} \quad (6.15)$$

To attain a small on resistance, we want

$$K = \frac{KP}{2} \left(\frac{W}{L}\right)$$

The designer can lower R_{on} by choosing a larger value for W/L .

to be large, which the circuit designer can achieve by selecting a sufficiently large value for W/L .

Load-Line Analysis

We can gain a better understanding of the resistor-pull-up inverter by considering a load-line analysis. As an example, we assume that $R = 90 \text{ k}\Omega$ and that the NMOS parameters are $V_{to} = 1 \text{ V}$, $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $W/L = 1/2$.

The drain characteristics of the NMOS transistor are illustrated in Figure 6.19. For the moment, we assume that the load capacitance is an open circuit. Using the values $R_D = 90 \text{ k}\Omega$ and $V_{DD} = 5 \text{ V}$, we construct the load line shown in Figure 6.19.

Notice that if the input voltage is less than the threshold voltage of the transistor ($V_{to} = 1 \text{ V}$), the transistor is cut off. Then the circuit operates at point A, and the output voltage is $V_{OH} = V_{DD}$.

As the input voltage is raised above the threshold, the point of operation moves up the load line. When $v_I = V_{DD}$, the circuit operates at point B, the output voltage is low, and the transistor is operating in the triode region.

Design of the Resistor-Pull-Up MOS Inverter

In selecting the value of the pull-up resistor R_D , we encounter conflicting objectives. On the one hand, we want to make the resistor large, because this leads to a small current when the transistor is on. This, in turn, means a smaller demand on the power supply and less heating of the circuit. On the other hand, we want to make R_D small so that the load capacitance is quickly charged when the FET switches off.

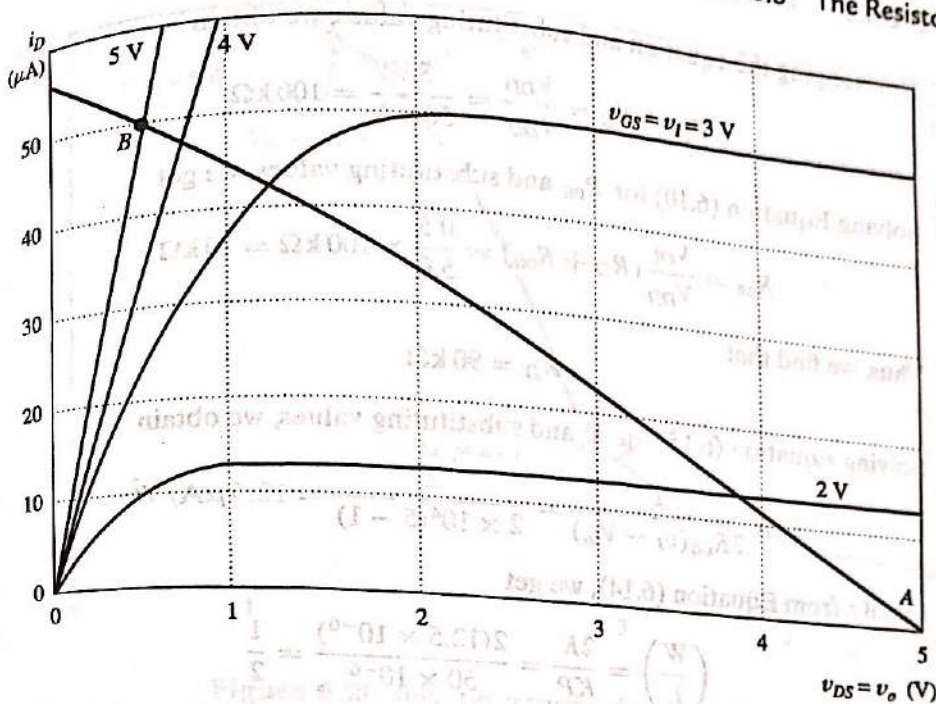


Figure 6.19 Load-line analysis for the circuit of Figure 6.18a.

Example 6.1 Resistor-Pull-Up-MOS-Inverter Design

Design a resistor-pull-up MOS inverter to meet the following objectives:
Static power consumption in low output state = 0.25 mW

$$V_{OL} = 0.5 \text{ V}$$

$$V_{OH} = V_{DD} = 5 \text{ V}$$

Transistor: $V_{to} = 1 \text{ V}$, $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0$.

SOLUTION We need to specify the value of the pull-up resistor and W/L for the transistor. When the output is in the low state, the static power consumption is

$$P_{\text{static}} = 0.25 \times 10^{-3} = I_{DD} V_{DD}$$

Since we are given $V_{DD} = 5 \text{ V}$, we can solve for I_{DD} :

$$I_{DD} = \frac{P_{\text{static}}}{V_{DD}} = 50 \mu\text{A}$$

Next, with the output low, we have

$$I_{DD} = \frac{V_{DD}}{R_{\text{on}} + R_D}$$

Rearranging the equation and substituting values, we obtain

$$R_{on} + R_D = \frac{V_{DD}}{I_{DD}} = \frac{5 \text{ V}}{50 \mu\text{A}} = 100 \text{ k}\Omega$$

Solving Equation (6.10) for R_{on} and substituting values, we get

$$R_{on} = \frac{V_{OL}}{V_{DD}}(R_D + R_{on}) = \frac{0.5}{5.0} \times 100 \text{ k}\Omega = 10 \text{ k}\Omega$$

Thus, we find that

$$R_D = 90 \text{ k}\Omega$$

Solving Equation (6.15) for K and substituting values, we obtain

$$K = \frac{1}{2R_{on}(v_I - V_{to})} = \frac{1}{2 \times 10^4(5 - 1)} = 12.5 \mu\text{A/V}^2$$

Finally, from Equation (6.14), we get

$$\left(\frac{W}{L}\right) = \frac{2K}{KP} = \frac{2(12.5 \times 10^{-6})}{50 \times 10^{-6}} = \frac{1}{2}$$

This completes the design. The circuit is the one shown in Figure 6.18, and its load-line analysis is illustrated in Figure 6.19.

The Transfer Characteristic

and Determination of V_{IL} and V_{IH}

The transfer characteristic of a logic inverter is a plot of the output voltage v_O versus the input voltage v_I .

Example 6.2 Transfer Characteristic using SPICE

Use SPICE to obtain the transfer characteristic of the inverter that we designed in Example 6.1. Assume that the load capacitance is zero.

SOLUTION After drawing the circuit, we select the transistor and use the **edit/model/edit instance model** command to bring up the window in which we specify the model name and the parameters for the NMOS transistor ($KP = 50 \times 10^{-6}$, $V_{TO} = 1$, $LAMBDA = 0$). Then we double click the left button of the mouse with the cursor on the NMOS symbol and enter the channel length $L = 10^{-6}$ and width $W = 2 \times 10^{-6}$. We use the **analysis/setup/dc sweep** commands to bring up the **DC Sweep** window. We choose v_I as the sweep variable and set up for a sweep from 0 to 5 V in 0.01-V increments. Then we use the **analysis/simulate** command to start the simulation, after which Probe starts and displays the inverter transfer characteristic shown in Figure 6.20. (The circuit schematic is stored in the file named Fig6.18, which can be found on the website.)

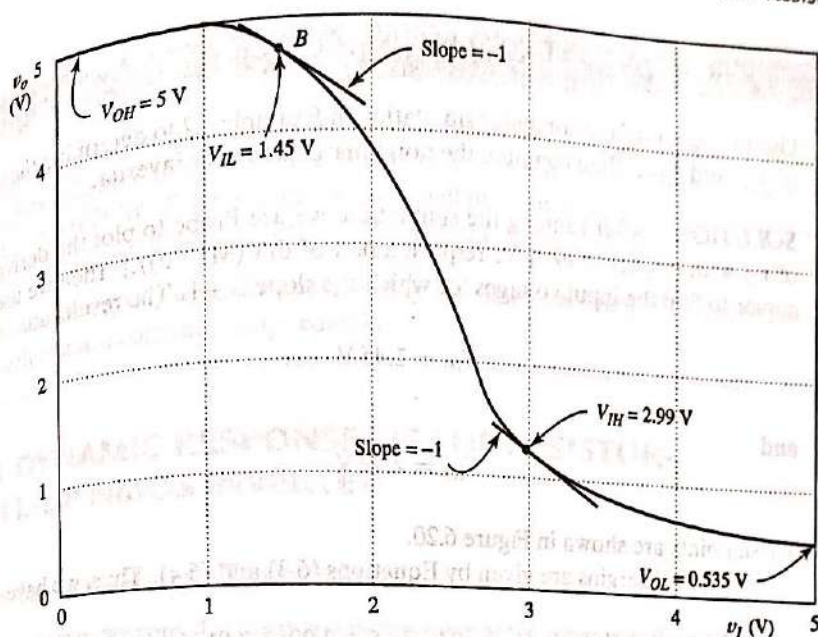


Figure 6.20 Inverter transfer characteristic.

Using the cursor in the Probe program, we find that $V_{OL} = 0.535\text{ V}$, which is very close to our design objective of 0.5 V . (The reason for the discrepancy is the fact that the on resistance of the FET is nonlinear. In other words, the drain characteristics are curved in the triode region.)

Using SPICE to Determine Noise Margins

Recall that for standard logic families, V_{IL} is the highest input voltage guaranteed by the manufacturer to be accepted as logic 0. Similarly, V_{IH} is the lowest input guaranteed to be accepted as logic 1. In setting these specifications, a manufacturer must consider variations in temperature and in the manufacturing process. As the temperature changes over the specified operating range, the FET parameters and resistances change slightly, resulting in slightly different transfer characteristics. Process parameters (the doping level, diffusion temperatures, and so forth) can be different for each circuit, culminating in additional variation in the transfer characteristics.

It is difficult to anticipate what variations can be expected in the processes that you may be using several years from now. We need a simple, but meaningful, way to define V_{IL} and V_{IH} so that we can compare the noise margins of different designs. Toward that end, we define V_{IL} and V_{IH} to be the input voltages for which the slope of the inverter transfer characteristic is -1 , as illustrated in Figure 6.20. A reason for choosing this definition is that if v_I is higher than V_{IH} and a slight variation occurs in v_I due to noise, the resulting variation in v_O will be smaller than the variation in v_I . A similar statement can be made when v_I is lower than V_{IL} . Thus, when v_I is lower than V_{IL} or higher than V_{IH} , noise is attenuated rather than being amplified by the inverter.

To compare the noise margins of different designs in this book, we define V_{IL} and V_{IH} to be the input voltages for which the slope of the inverter transfer characteristic is -1 .

Example 6.3 Determination of Noise Margin

Use the results of the computer simulation in Example 6.2 to determine the values of V_{IL} and V_{IH} . Then compute the noise margins for this inverter.

SOLUTION After running the simulation, we use Probe to plot the derivative of v_O with respect to v_I . [We request a plot of $d(V(M1 : d))$.] Then we use the cursor to find the input voltages for which the slope is -1 . The results are

$$V_{IL} = 1.45 \text{ V}$$

and

$$V_{IH} = 2.99 \text{ V}$$

These points are shown in Figure 6.20.

The noise margins are given by Equations (6.3) and (6.4). Thus, we have

$$NM_H = V_{OH} - V_{IH} = 5 - 2.99 = 2.01 \text{ V}$$

and

$$NM_L = V_{IL} - V_{OL} = 1.45 - 0.5 = 0.95 \text{ V}$$

Notice that the noise margins are not equal. In general, it is desirable for the noise margins to be equal and as large as possible. The best noise margins possible are $V_{DD}/2$. □

EXERCISE

6.7 Repeat Example 6.1 for $V_{OL} = 0.25 \text{ V}$. Assume that the other design objectives remain the same as in the example.

Answer $R_D = 95 \text{ k}\Omega$; $W/L = 1/1$.

EXERCISE

6.8 Use SPICE to determine V_{IH} , V_{IL} , and the noise margins for the inverter designed in Exercise 6.7.

Answer $V_{IH} = 2.47 \text{ V}$; $V_{IL} = 1.21 \text{ V}$; $NM_H = 2.53 \text{ V}$; $NM_L = 0.96 \text{ V}$. Notice that these noise margins are larger than those of the inverter designed and analyzed in Examples 6.1, 6.2, and 6.3.

EXERCISE

6.9 Suppose that a certain IC is to be composed of logic gates, each of which consumes 0.25 mW of static power. The maximum static power dissipation allowed for the chip is 20 W. (This amount is in the ball park for dissipation of computer chips.) What is the maximum number of gates that the chip can contain?

Answer 80,000, which is considerably less than the number of gates that high-performance computer chips contain.

6.4 DYNAMIC RESPONSE OF THE RESISTOR-PULL-UP NMOS INVERTER

The Low-to-High Transition

In this section, we consider the dynamic response of the resistor-pull-up NMOS inverter. First, let us consider the simplest situation, which is illustrated in Figure 6.21. The input to the inverter is high until $t = 0$ and then switches low. Thus, the transistor is on until $t = 0$, at which time it switches off. Then the load capacitance charges through the pull-up resistor. The equivalent circuit is shown in Figure 6.21b.

The output voltage is given by

$$v_O(t) = V_{DD} - \Delta V \exp(-t/R_D C) \quad (6.16)$$

which is illustrated in Figure 6.21c. Notice that ΔV is the difference between the output logic levels:

$$\Delta V = V_{OH} - V_{OL} = V_{DD} - V_{OL} \quad (6.17)$$

We want to find expressions for the following:

t_{10} = time at which 10% of the transition has been completed;

t_{90} = time at which 90% of the transition has been completed;

$t_r = t_{90} - t_{10}$ = rise time;

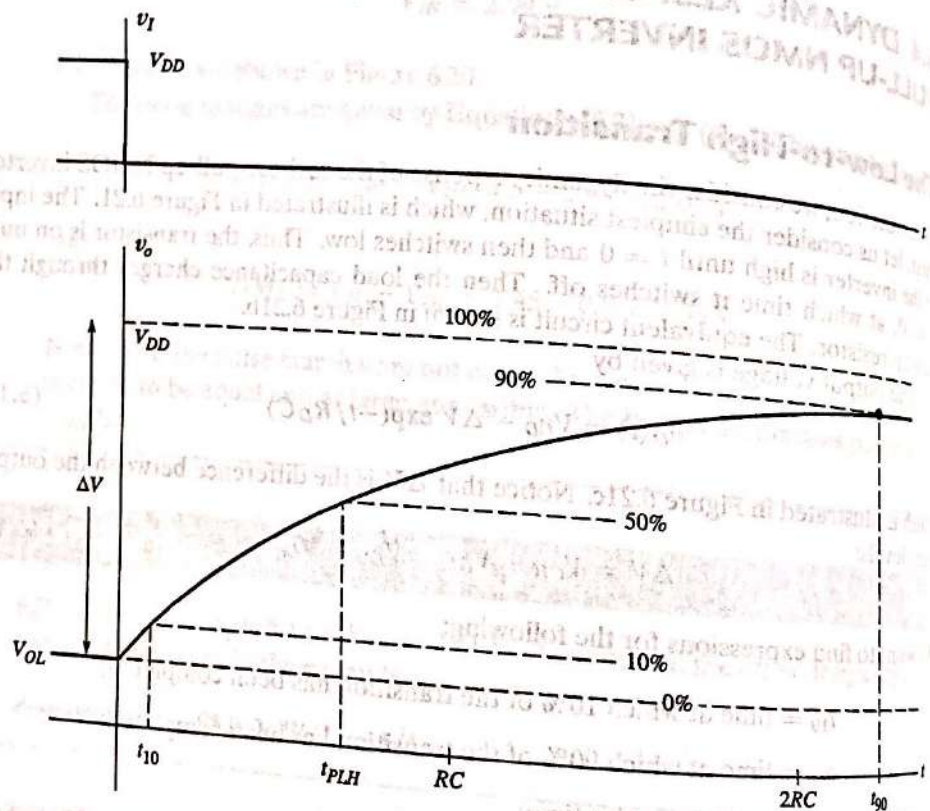
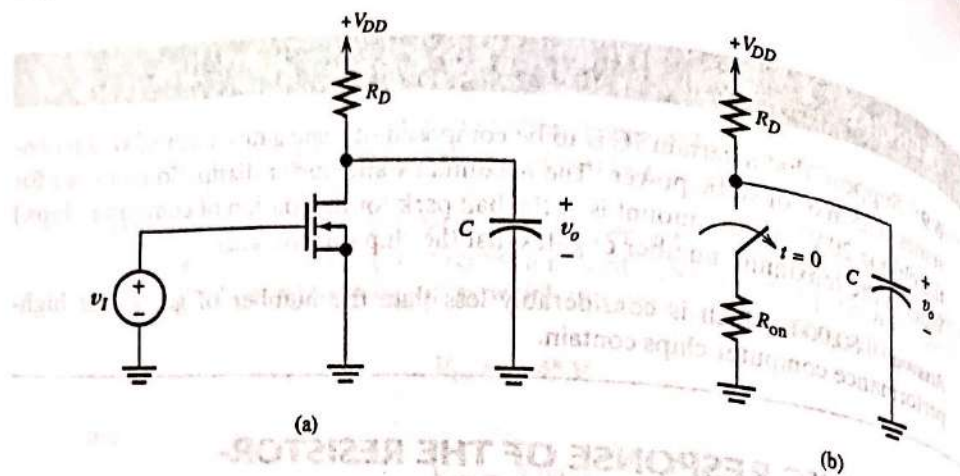
t_{PLH} = time at which 50% of the transition has been completed.

To determine t_{10} , we note that the output voltage at that time is equal to $V_{OL} + 0.1\Delta V$. Thus, Equation (6.16) becomes

$$v_O(t_{10}) = V_{OL} + 0.1\Delta V = V_{DD} - \Delta V \exp(-t_{10}/R_D C)$$

Rearranging this equation, we have

$$V_{OL} - V_{DD} + 0.1\Delta V = -\Delta V \exp(-t_{10}/R_D C) \quad (6.18)$$



(c) Input and output waveforms

Figure 6.21 The low-to-high output transition of the resistor pull-up NMOS inverter.

However, from Equation (6.17), we have $\Delta V = V_{DD} - V_{OL}$, so Equation (6.18) becomes

$$0.9 = \exp(-t_{10}/R_D C) \quad (6.19)$$

Taking the natural logarithm of both sides of Equation (6.19) and rearranging, we obtain

$$t_{10} = -R_D C \ln(0.9) = 0.1054 R_D C \quad (6.20)$$

In a similar manner, we can establish that

$$t_{90} = -R_D C \ln(0.1) = 2.3025 R_D C \quad (6.21)$$

Then the rise time is given by

$$t_r = t_{90} - t_{10} = R_D C [\ln(0.1) - \ln(0.9)] = 2.20 R_D C \quad (6.22)$$

In the same way that we found t_{10} , we can determine

$$t_{PLH} = -R_D C \ln(0.5) = 0.6931 R_D C \quad (6.23)$$

Example 6.4 Determination of t_{PLH} for the Resistor-Pull-Up NMOS Inverter

Compute the rise time and t_{PLH} for the inverter of Example 6.1 (which has $R_D = 90 \text{ k}\Omega$). Assume that the load capacitance is 1 pF .

SOLUTION Substituting into Equations (6.22) and (6.23), we have

$$t_r = 2.20 R_D C = 198 \text{ ns}$$

and

$$t_{PLH} = 0.6931 R_D C = 62.4 \text{ ns}$$

□

The High-to-Low Transition

Now let us consider the situation in which the input is low and then switches high. The load-line construction for the circuit of Example 6.4 is shown in Figure 6.22. Initially, the transistor is off and the circuit is operating at point A. When the input switches high, the transistor begins to conduct. Because of the load capacitance, the output voltage (which is equal to v_{DS}) cannot change instantaneously. Thus, the operating point moves vertically to point B. Because of the current taken by the transistor, the output voltage falls and the instantaneous operating point moves along the characteristic curve, ending up in steady state at point C.

NMOS

18) becomes

(6.19)

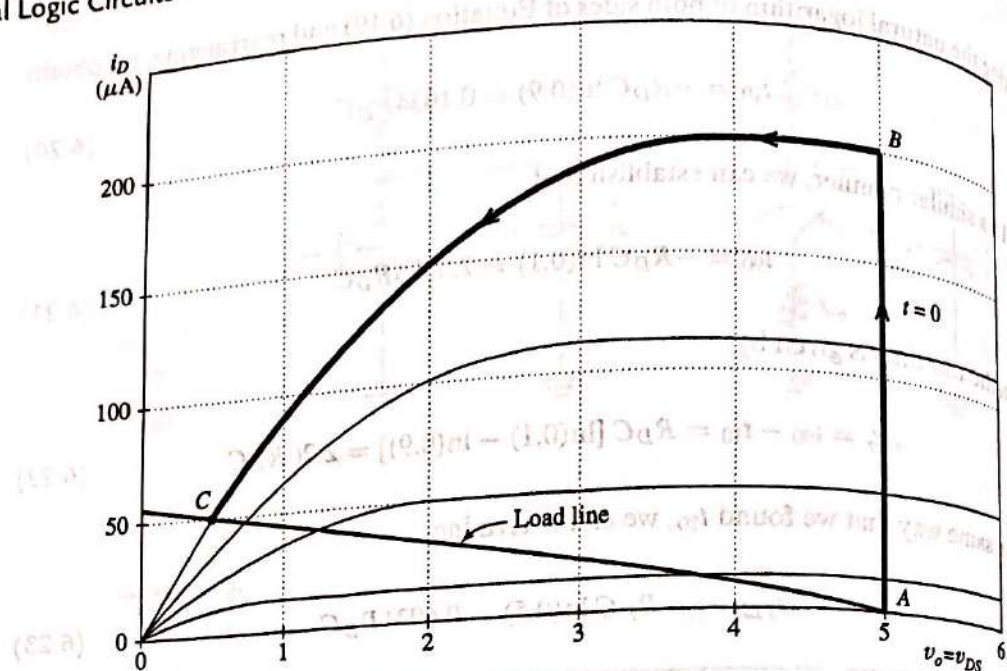


Figure 6.22 Load-line analysis of the high-to-low transition.

The current conducted by the transistor during the high-to-low transition (of v_o) is much larger than the current in the resistor during the low-to-high transition. In our sample circuit, the maximum current through the resistor is

$$\frac{V_{DD} - V_{OL}}{R_D} = \frac{5 - 0.5}{90 \text{ k}\Omega} = 50 \mu\text{A}$$

On the other hand, looking at point B in Figure 6.22, we see that the maximum current in the NMOS device is $200 \mu\text{A}$.

Therefore, we conclude that the high-to-low transition of the output occurs much faster than the opposite transition. Another way to comprehend this fact is to recall that we designed the inverter so R_{on} is much smaller than R_D . The load capacitance charges through R_D and discharges through R_{on} . Of course, smaller resistance leads to faster transitions.

In digital design, it is mainly the slowest transition that sets performance limits. Thus, for the resistor-pull-up NMOS inverter, t_{PHL} is not as significant as t_{PLH} is. Furthermore, the analytical search for an expression for t_{PHL} is complicated by the nonlinear behavior of the NMOS transistor. Rather than relying on approximate analysis by using simplifying assumptions, we can use simulation to determine rise times and propagation delays.

Actually, the analysis that we carried out to determine t_{PLH} was also approximate, because we assumed that the input voltage switched instantaneously. In real digital circuits, inverters are driven by the output of other gates, and the input transition is more gradual. The NMOS does not turn off instantly, as we assumed in the analysis.

In a resistor-pull-up NMOS inverter, the high-to-low transition of the output occurs much faster than the opposite transition.

In digital design it is mainly the slowest transition that sets performance limits.

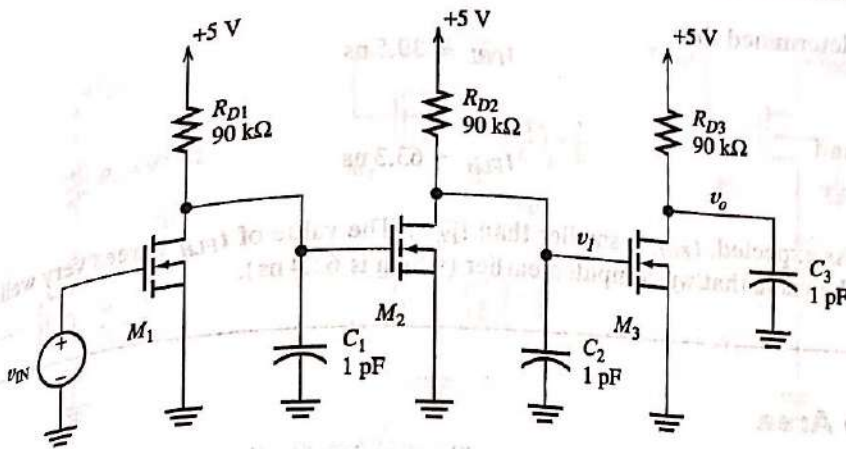


Figure 6.23 Cascade of three inverters.

Example 6.5 Determination of Propagation Delay with SPICE

Use PSpice to simulate the propagation delay of the NMOS inverter of Example 6.1. Cascade three inverters, each with a load capacitance of 1 pF, and determine the propagation delays for the last inverter in the chain.

SOLUTION The circuit is displayed in Figure 6.23. We set up the input source to produce a 600-ns 5-V pulse that starts at 100 ns. The input and output waveforms for the third inverter are shown in Figure 6.24. Using the Probe cursor, we

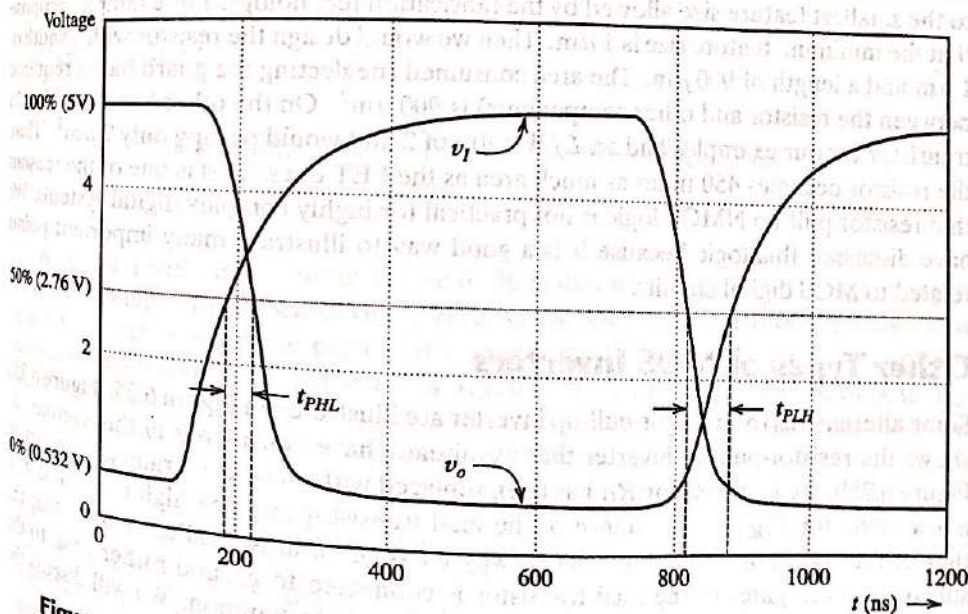


Figure 6.24 Input and output waveforms for the third stage of Figure 6.23.

determined that

$$t_{PHL} = 39.5 \text{ ns}$$

and

$$t_{PLH} = 63.3 \text{ ns}$$

As expected, t_{PHL} is smaller than t_{PLH} . The value of t_{PLH} agrees very well with the value that we computed earlier (which is 62.4 ns).

Chip Area

Let us consider the chip area consumed by a resistor-pull-up NMOS inverter. We discussed integrated resistors in Section 2.5, where we introduced the following expression for resistance:

$$R = R_{\square} \frac{L}{W}$$

Here, L is the length of the resistor, W is its width, and $R_{\square}$ is the sheet resistance of the layer used to fabricate the resistor. Suppose that the resistor for the inverter of our previous example is constructed with material having $R_{\square} = 100 \Omega/\square$. Then the 90-k Ω resistor requires that

$$\frac{L}{W} = \frac{R_D}{R_{\square}} = \frac{90 \text{ k}\Omega}{100 \Omega} = 900$$

To conserve area in IC layout, we select the minimum dimension of a component equal to the smallest feature size allowed by the fabrication technology. For example, suppose that the minimum feature size is $1 \mu\text{m}$. Then we would design the resistor with a width of $1 \mu\text{m}$ and a length of $900 \mu\text{m}$. The area consumed (neglecting the guard bands required between the resistor and other components) is $900 \mu\text{m}^2$. On the other hand, the NMOS transistor for our examples had an L/W ratio of 2 and would occupy only $2 \mu\text{m}^2$. Thus, the resistor occupies 450 times as much area as the FET does. This is one of the reasons that resistor-pull-up NMOS logic is not practical for highly complex digital systems. We have discussed this logic because it is a good way to illustrate many important points related to MOS digital circuits.

Because resistors consume excessive chip area, resistor-pull-up NMOS logic is not practical for highly complex digital systems.

Other Types of MOS Inverters

Some alternatives to a resistor-pull-up inverter are illustrated in Figure 6.25. Figure 6.25a shows the resistor-pull-up inverter that we already have considered in this section. In Figure 6.25b, the load resistor R_D has been replaced with an NMOS transistor. To attain a low value for V_{OL} , the resistance of the load transistor must be high compared with that of the switching transistor. That is why its W/L ratio is smaller. Notice that the substrate (back gate) of the load transistor is connected to ground rather than to the source, because the substrates for all of the transistors are common. We will discuss the implications of this fact shortly.

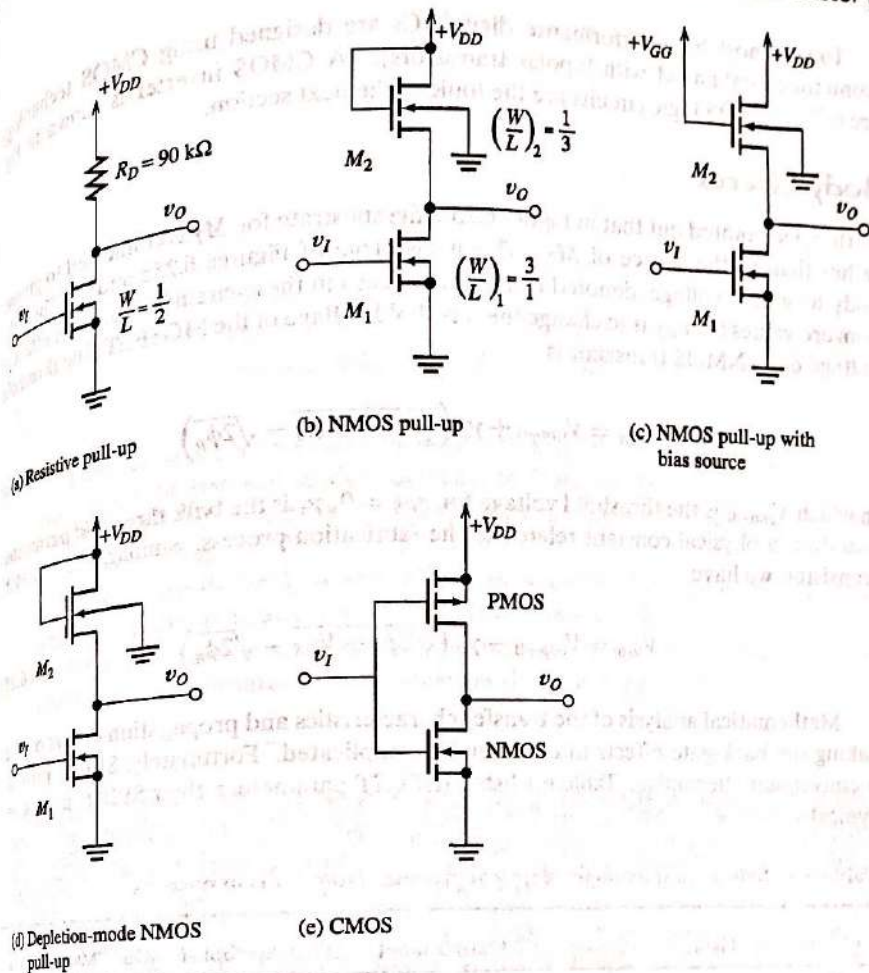


Figure 6.25 Several types of MOS inverter circuits.

A problem with the circuit of Figure 6.25b is that when the output is high, the gate-to-source voltage of the load device is zero, so the load transistor is off, and the output is not held high when noise current is injected into the output terminal by capacitive coupling. A solution to the problem is to return the gates of the load devices to V_{GG} , which is higher in value than V_{DD} , as shown in Figure 6.25c. A problem with this circuit is that the distribution of V_{GG} complicates the chip layout.

A better solution is to replace the load transistor with a depletion-mode MOSFET, as shown in Figure 6.25d. (Recall that a depletion-mode NMOS transistor has a negative threshold voltage and conducts with $v_{GS} = 0$.) An additional ion implantation step is needed in the fabrication of the circuit to dope the channels of the loads, but improvements in performance justify the cost. NMOS logic with enhancement load devices was an important technology during the early 1980s and was used in the original IBM PC.

Today, most high-performance digital ICs are designed using CMOS technology (sometimes enhanced with bipolar transistors).

Today, most high-performance digital ICs are designed using CMOS technology (sometimes enhanced with bipolar transistors). A CMOS inverter is shown in Figure 6.25e. CMOS logic circuits are the topic of the next section.

Body Effects

Earlier, we pointed out that in Figure 6.25b, the substrate for M_2 is connected to ground rather than to the source of M_2 . This is also true of Figures 6.25c and d. Thus, the body-to-source voltage, denoted as v_{BS} , is nonzero in these circuits. The main effect of nonzero values for v_{BS} is to change the threshold voltage of the MOSFET. The threshold voltage of an NMOS transistor is

$$V_{ton} = V_{ton-0} + \gamma_n \left(\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p} \right) \quad (6.24)$$

in which V_{ton-0} is the threshold voltage for $v_{BS} = 0$, γ_n is the **bulk threshold parameter**, and ϕ_p is a physical constant related to the fabrication process. Similarly, for a PMOS transistor, we have

$$V_{top} = V_{top-0} - \gamma_p \left(\sqrt{2\phi_n + V_{BS}} - \sqrt{2\phi_n} \right) \quad (6.25)$$

Mathematical analysis of the transfer characteristics and propagation delays of gates taking the back-gate effects into account is complicated. Fortunately, SPICE provides a convenient alternative. Table 6.1 lists MOSFET parameters, their SPICE names, and typical values.

Table 6.1. SPICE parameters for a typical process. Note: L is in microns.

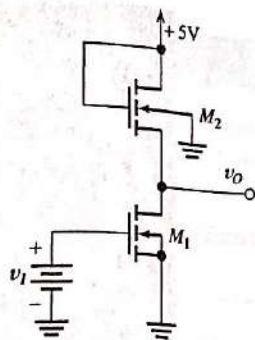
Name	Math Symbol	SPICE Symbol	NMOS	PMOS	Units
Transconductance parameter	KP_n or KP_p	KP	50	25	$\mu A/V^2$
Threshold voltage	V_{ton-0} or V_{top-0}	VTO	1	-1	V
Channel-length modulation parameter	λ_n or λ_p	LAMBDA	$0.1/L$	$0.1/L$	V^{-1}
Bulk threshold parameter	γ_n or γ_p	GAMMA	0.6	0.6	$\sqrt{V}$
Surface potential	ϕ_n or ϕ_p	PHI	0.8	0.8	V

Example 6.6 Transfer Characteristic of an NMOS-Pull-Up Inverter

Utilize PSpice to plot the transfer characteristic for the inverter illustrated in Figure 6.25b using the transistor parameters given in Table 6.1. Assume that the minimum feature size of each transistor is $1 \mu m$.

SOLUTION First we use Schematics to draw the circuit as shown in Figure 6.26. For M_1 , we have $W_1 = 3 \mu m$ and $L_1 = 1 \mu m$. On the other hand, for M_2 , we have $W_2 = 1 \mu m$ and $L_2 = 3 \mu m$. By double clicking on each transistor's icon, we bring up the attribute windows in which we enter L and W .

Figure 6.26
Circuit for
Example 6.6.



Then we select a transistor by single clicking on its icon, and use the **edit/model/edit instance model** command to bring up the window in which we can enter the model name and the parameter values. The model window for M_2 is shown in Figure 6.27.

Next, we use the **analysis/setup/dc sweep** command to bring up the window in which we specify the parameters for the input source, as illustrated in Figure 6.28.

Finally, we use the **analysis/simulate** command to start the simulation, after which the transfer characteristic appears as shown in Figure 6.29.

Attach a voltage marker to the output terminal so Probe will display the output voltage automatically.

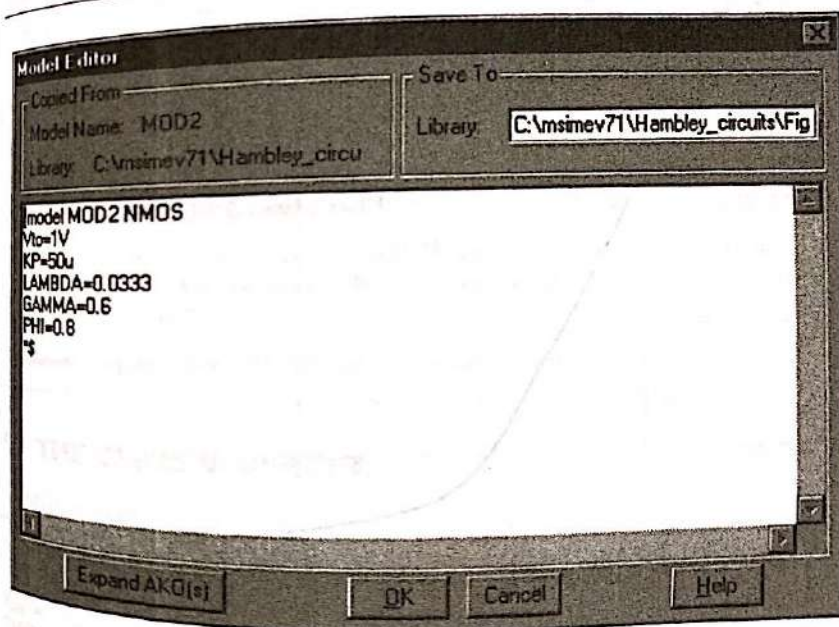


Figure 6.27 Model window for M_2 .

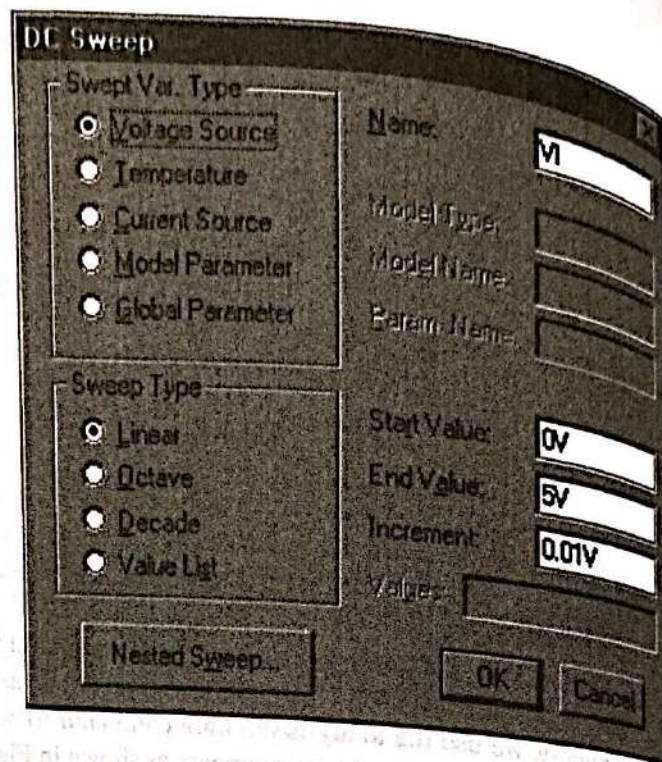


Figure 6.28
Setup window for
DC sweeps.

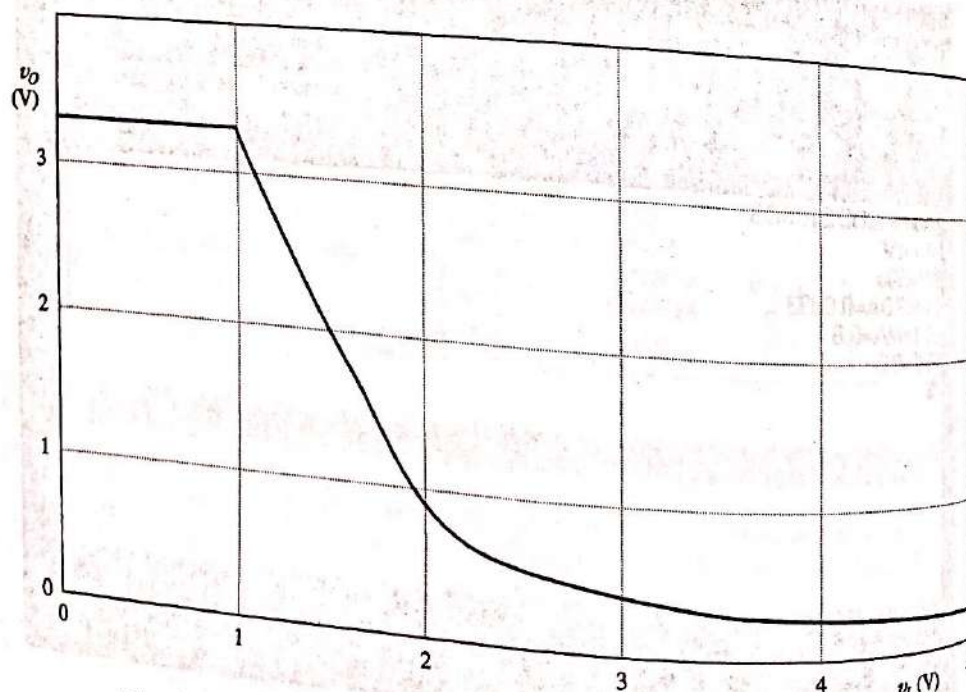


Figure 6.29 Transfer characteristic of the NMOS pull-up inverter.

EXERCISE

6.10 Use SPICE to determine t_{PHL} and t_{PLH} for a resistor-pull-up NMOS inverter with $R = 95 \text{ k}\Omega$, $W/L = 1 \mu\text{m}/1 \mu\text{m}$, $V_{to} = 1 \text{ V}$, $K_P = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and a load capacitance of 1 pF .

Answer The circuit schematic is stored in the file named Exer6.10. For this circuit, $t_{PHL} = 19 \text{ ns}$ and $t_{PLH} = 68.0 \text{ ns}$.

EXERCISE

6.11 Consider a resistor-pull-up NMOS inverter. What effect (an increase, a decrease, or none) will increasing R_D have on (a) t_{PLH} ? (b) t_{PHL} ? (c) V_{OH} ? (d) V_{OL} ? (e) the chip area?

Answer (a) increase; (b) none; (c) none; (d) decrease; (e) increase.

EXERCISE

6.12 Consider a resistor-pull-up NMOS inverter. What effect (an increase, a decrease, or none) will increasing W/L have on (a) t_{PLH} ? (b) t_{PHL} ? (c) V_{OH} ? (d) V_{OL} ?

Answer (a) none; (b) decrease; (c) none; (d) decrease.

EXERCISE

6.13 Consider a resistor-pull-up NMOS inverter. What effect (an increase, a decrease, or none) will increasing the load capacitance have on (a) t_{PLH} ? (b) t_{PHL} ? (c) V_{OH} ? (d) V_{OL} ?

Answer (a) increase; (b) increase; (c) none; (d) none.

6.5 THE CMOS INVERTER

A CMOS inverter is illustrated in Figure 6.30a, and simple equivalent circuits are shown in Figures 6.30b and 6.30c. The capacitance C_L is the load presented by the driven gates and the interconnects. When the input voltage is low, the NMOS transistor is off and the PMOS transistor is on. Thus, the output voltage is held high by the PMOS transistor, and $V_{OH} = V_{DD}$. Notice that because the NMOS is off, the static power consumed by the CMOS inverter is zero.

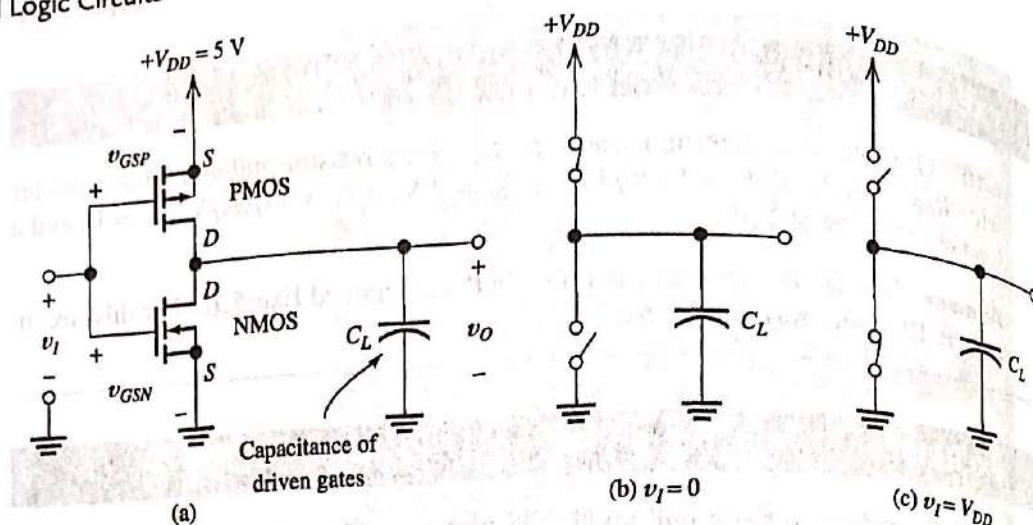


Figure 6.30 CMOS inverter.

Zero static power consumption is a very important advantage of CMOS circuits compared with circuits based on other technologies.

When the input voltage is high, the PMOS transistor is off and the NMOS is on. Thus, the output voltage is held low by the NMOS transistor, and $V_{OL} = 0$. Again, the static power is zero. Zero static power consumption is a very important advantage of CMOS circuits compared with circuits based on other technologies. This is the chief reason that complex digital ICs are based on CMOS design.

Graphical Analysis

In the discussion that follows, we assume that, except for differences in voltage polarity and current direction, the NMOS and PMOS transistors have identical characteristics. Recall that

$$K = \left(\frac{W}{L}\right) \frac{KP}{2}$$

We will use the subscript p to denote the parameters of the PMOS transistor and the subscript n to indicate the NMOS device. Typically, PMOS devices have a KP_p value that is about half of KP_n . (The exact ratio of KP_p to KP_n depends on the manufacturing process.) Hence, to achieve devices with identical characteristics (i.e., with $K_p = K_n$) we need to choose

$$\left(\frac{W}{L}\right)_p = 2 \left(\frac{W}{L}\right)_n$$

Because PMOS devices have a KP_p value that is about half of KP_n , we need to choose $(W/L)_p = 2(W/L)_n$ to achieve a symmetrical transfer characteristic for a CMOS inverter.

The threshold of the NMOS device is V_{ton} , which is a positive value, whereas the threshold voltage of the PMOS is $V_{top} = -V_{ton}$. Also, we assume, as is often the case, that the supply voltage V_{DD} is greater than twice the threshold voltage magnitude.

Notice in Figure 6.30a that the source terminal of the PMOS is connected to V_{DD} and the drain is connected to the inverter output. The gate-to-source voltage of the PMOS transistor is

$$v_{GSP} = v_I - V_{DD}$$

When $v_I = V_{DD}$, the gate-to-source voltage of the PMOS is zero and it is therefore cut off. Then, virtually no current flows from the supply. On the other hand, when $v_I = 0$, we have $v_{GSP} = -V_{DD}$, and the PMOS can deliver a large drain current to charge the load capacitance. Because the NMOS is cut off for $v_{GSN} = v_I = 0$, no current flows after the capacitance is charged.

Next, we will graphically analyze a CMOS inverter having $V_{DD} = 5\text{ V}$ and the following parameter values:

$$\begin{array}{ll} V_{ton} = 1\text{ V} & V_{top} = -1\text{ V} \\ KP_n = 50\text{ }\mu\text{A/V}^2 & KP_p = 25\text{ }\mu\text{A/V}^2 \\ \left(\frac{W}{L}\right)_n = \frac{4\text{ }\mu\text{m}}{1\text{ }\mu\text{m}} & \left(\frac{W}{L}\right)_p = \frac{8\text{ }\mu\text{m}}{1\text{ }\mu\text{m}} \\ \lambda_n = 0 & \lambda_p = 0 \end{array}$$

These values yield $K_n = K_p = 100\text{ }\mu\text{A/V}^2$.

Let us consider load-line constructions for the CMOS inverter. Recall that in the case of a resistive load, the load line is straight, corresponding to the volt-ampere characteristic of a resistor. However, for a CMOS inverter, the load line is not straight; instead, it is one of the characteristic curves of the PMOS. Furthermore, the resistor results in a fixed load line, but the line (actually, it is a curve) for the PMOS pull-up changes as v_I changes. The load lines are shown for several values of v_I on the characteristics of the NMOS in Figure 6.31.

For $v_I = 0$, the PMOS is highly conductive, but the NMOS is cut off, and the circuit operates at point A. [See Part (a) of the figure.] Point B illustrates the operating point for a value of v_I greater than the threshold voltage of the NMOS, but less than $V_{DD}/2$. At point B the NMOS is in saturation, and the PMOS is in the triode region.

When $v_I = V_{DD}/2 = 2.5\text{ V}$, the load line and the NMOS characteristic intersect not at a single point, but along the line from C to D in Figure 6.31b. Thus, as v_I increases through $V_{DD}/2$, the operating point switches abruptly from C to D.

Point E illustrates an operating point for a value of v_I between $V_{DD}/2$ and $V_{DD} - V_{ton}$. At point E the PMOS is in saturation, whereas the NMOS is in the triode region. For $v_I = V_{DD}$, the PMOS is cut off, and operation is at point F.

Transfer Characteristic

The transfer characteristic of the CMOS inverter is shown in Figure 6.32. Notice that the output voltage is 0 if v_I is higher than $V_{DD} - |V_{top}|$. Similarly, the output is V_{DD} if the input is less than V_{ton} . The transfer characteristic falls abruptly at $v_I = V_{DD}/2$. The CMOS inverter closely approximates the ideal transfer characteristic for a logic inverter (illustrated in Figure 6.9).

The CMOS inverter closely approximates the ideal transfer characteristic for a logic inverter.

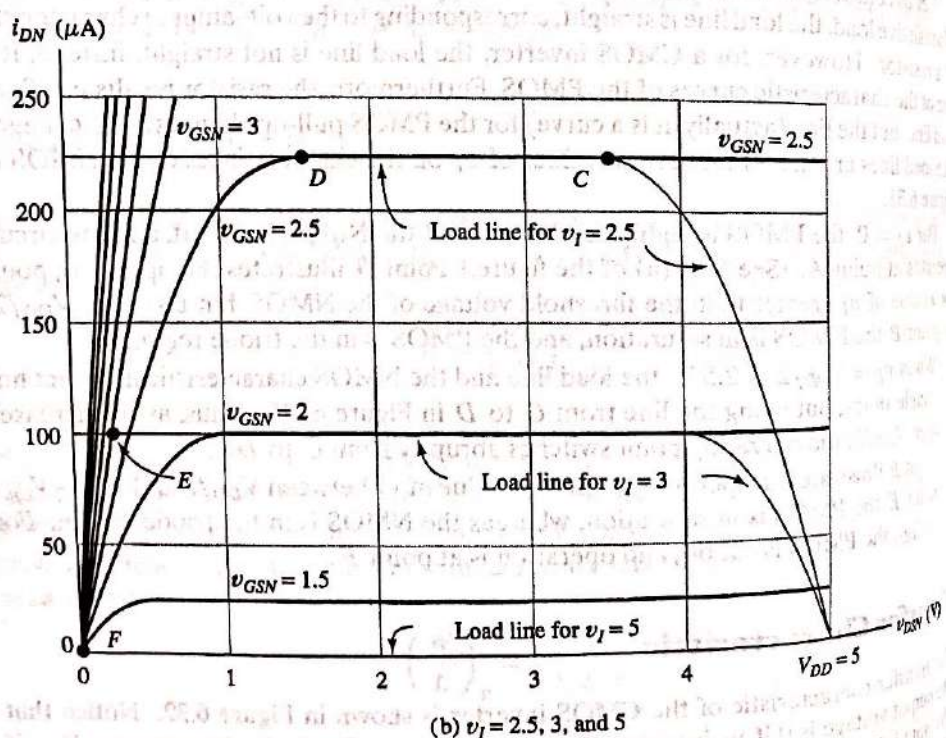
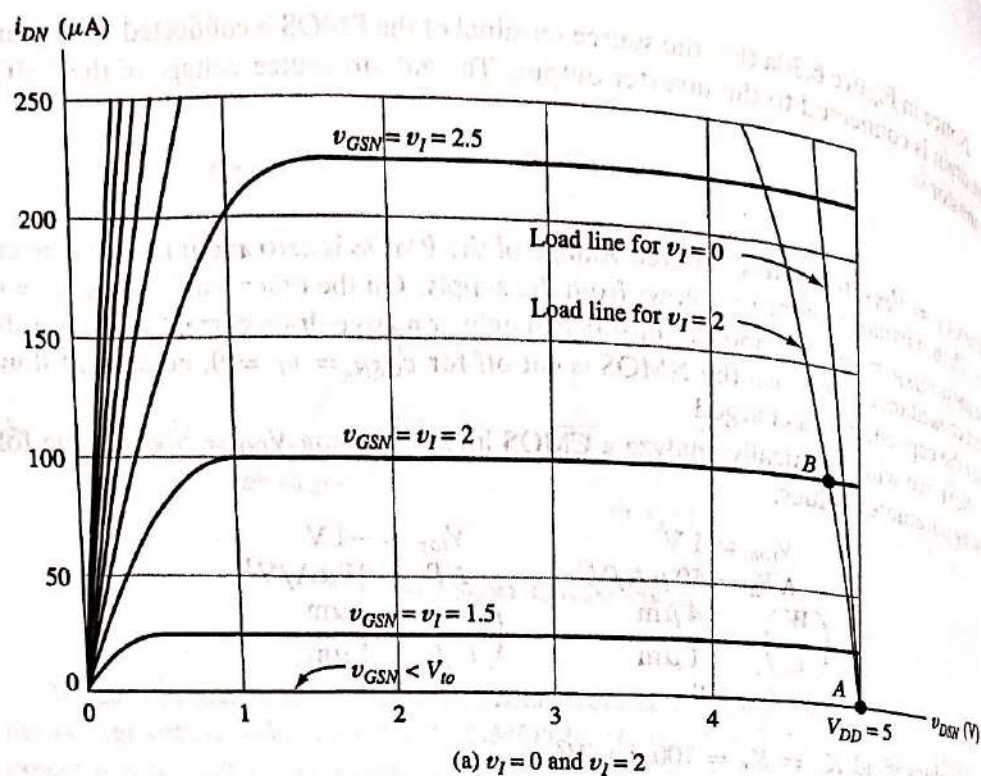


Figure 6.31 Graphical analysis of the CMOS inverter.

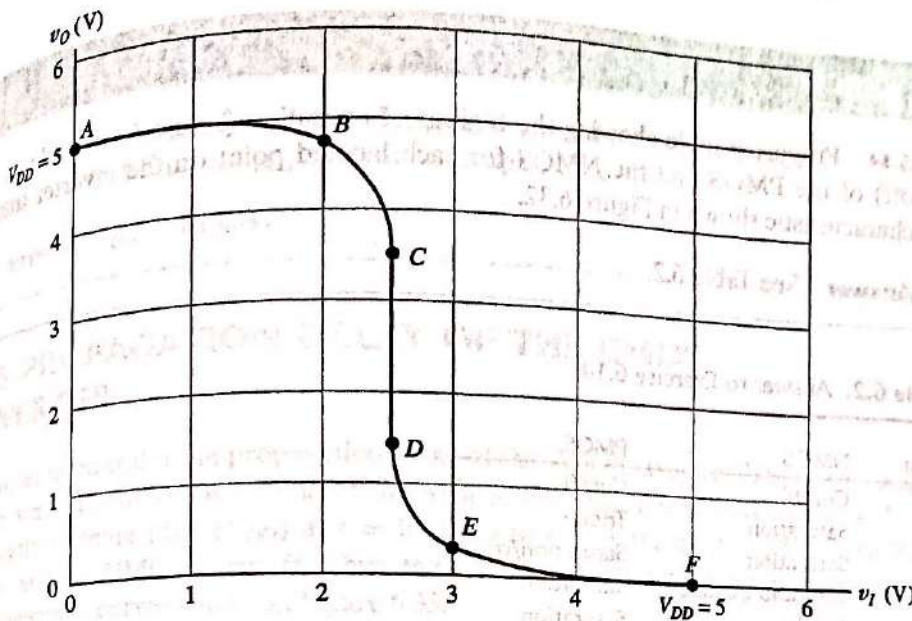


Figure 6.32 Transfer characteristic of a typical CMOS inverter. The lettered points correspond to the points of Figure 6.31.

The current flowing from the supply through the transistors of the CMOS inverter, assuming an open-circuit load, is shown in Figure 6.33. Notice that if $v_I = 0$ or $v_I = V_{DD}$, the current is zero. Maximum current flow occurs for $v_I = V_{DD}/2$. The maximum current value depends on the supply voltage and on the value of K_n and K_p .

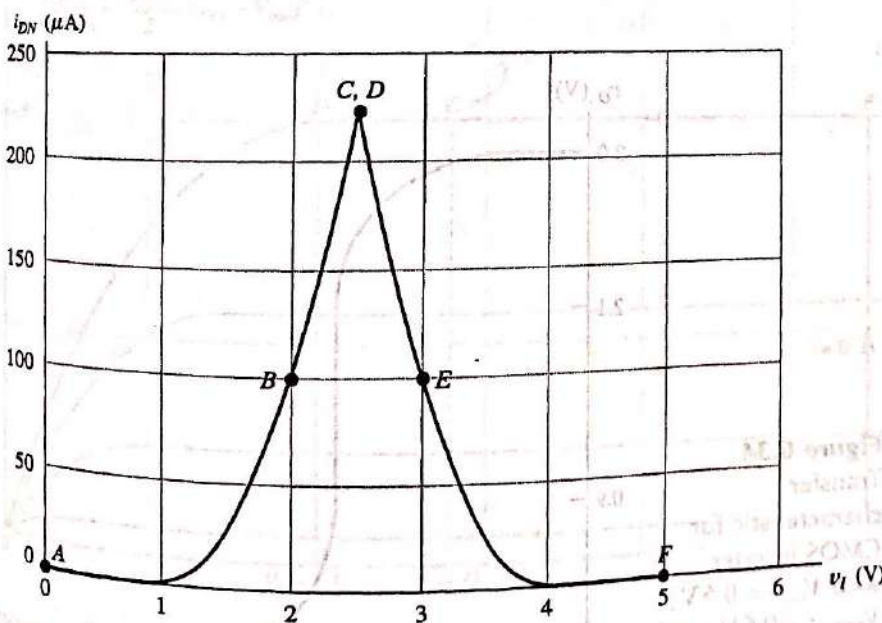


Figure 6.33 Supply current for a CMOS inverter.

EXERCISE

6.14 Prepare a table showing the regions of operation (saturation, triode, or cutoff) of the PMOS and the NMOS for each labeled point on the inverter transfer characteristic shown in Figure 6.32.

Answer See Table 6.2.

Table 6.2. Answer to Exercise 6.14.

Point	NMOS	PMOS
A	Cutoff	Cutoff
B	Saturation	Triode
C	Saturation	Saturation/triode
D	Saturation/triode	Saturation
E	Triode	Saturation
F	Cutoff	Cutoff

EXERCISE

6.15 A CMOS inverter is constructed with symmetrical devices having $V_{ton} = 0.6\text{ V}$ and $V_{top} = -0.6\text{ V}$. Sketch the transfer characteristic to scale if $V_{DD} = 3\text{ V}$.

Answer See Figure 6.34.

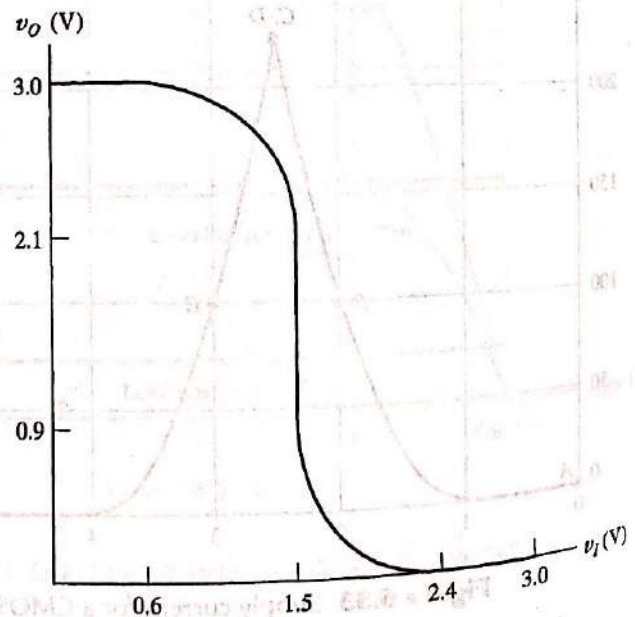


Figure 6.34
Transfer characteristic for CMOS inverter with $V_{ton} = 0.6\text{ V}$, $V_{top} = -0.6\text{ V}$, and $V_{DD} = 3\text{ V}$.

EXERCISE

6.16 If the devices have $|K| = 100 \mu\text{A}/\text{V}^2$, find the current through the inverter of Exercise 6.15 if $v_I = V_{DD}/2$. Assume an open-circuit load.

Answer $i_{DN} = 81 \mu\text{A}$.

6.6 PROPAGATION DELAY OF THE CMOS INVERTER

Next, let us consider the propagation delay of the CMOS inverter. (The circuit diagram is shown in Figure 6.30a.) To start, we assume that the input is initially low (0 V) and instantly switches high (V_{DD}) at $t = 0$. Prior to $t = 0$, the output is high, the PMOS is on, and the NMOS is cutoff. Thus, the NMOS transistor operates at point A on the characteristic curves shown in Figure 6.35.

When the input switches high, the PMOS switches off and the NMOS switches on. Because the voltage across the load capacitance cannot change instantly, the output voltage immediately after $t = 0$ is $v_O(0+) = V_{DD}$. At $t = 0+$, the NMOS device has $v_{GSN} = v_I = V_{DD}$ and $v_{DSN} = v_O$. Therefore, the instantaneous operating point moves to point B at $t = 0+$. Subsequent to $t = 0$, the NMOS drain current discharges the load capacitance.

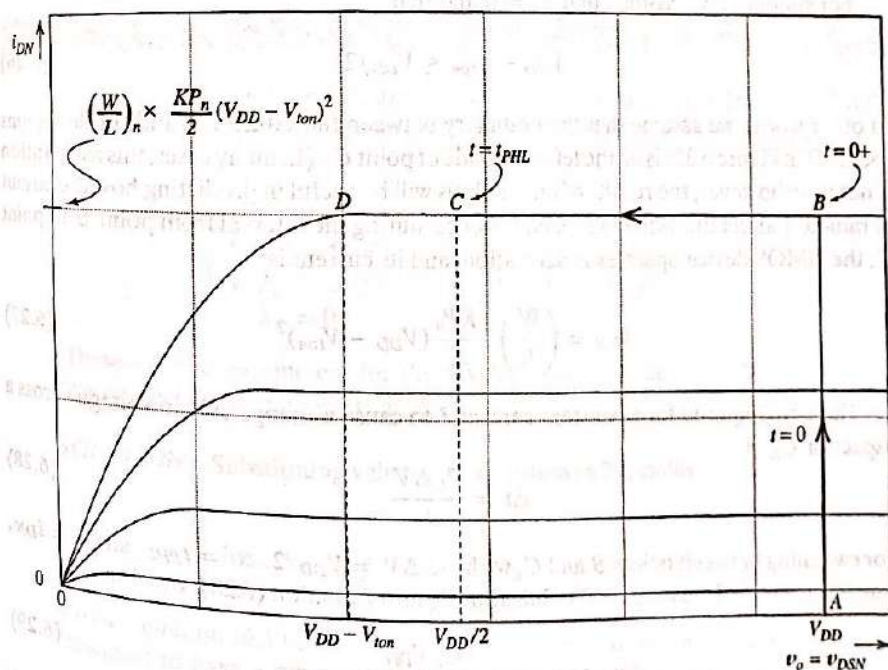


Figure 6.35 The high-to-low transition of the CMOS inverter.

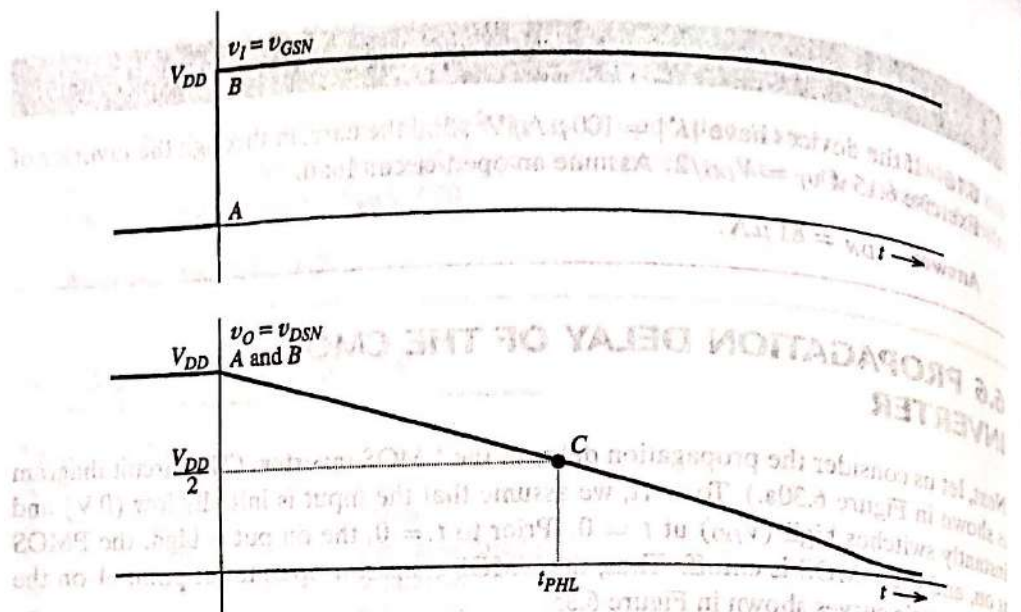


Figure 6.36 Idealized waveforms for the high-to-low transition of the CMOS inverter.

The input and output waveforms are displayed in Figure 6.36. The labeled points on the waveforms (points A, B, and C) correspond to the points on the drain characteristics illustrated in Figure 6.35. The high-to-low propagation delay t_{PHL} is indicated.

For simplicity, we assume that $\lambda_n = 0$ and that

$$V_{DD} - V_{ton} \leq V_{DD}/2 \quad (6.26)$$

In other words, we assume that the boundary between the saturation and triode regions (point D in Figure 6.35) is on the left-hand side of point C. (In many cases, this assumption is not true; however, the results of our analysis will be useful in predicting how the circuit parameters affect the switching speed.) Hence, during the interval from point B to point C, the NMOS device operates in saturation, and its current is

$$i_{DN} = \left(\frac{W}{L}\right)_n \frac{KP_n}{2} (V_{DD} - V_{ton})^2 \quad (6.27)$$

The time required for a constant current I to cause a change ΔV in voltage across a capacitor C_L is

$$\Delta t = \frac{C_L \Delta V}{I} \quad (6.28)$$

For switching between points B and C, we have $\Delta V = V_{DD}/2$, $\Delta t = t_{PHL}$, and $I = i_{DN}$, which is given by Equation (6.27). Substituting into Equation (6.28), we obtain

$$t_{PHL} = \frac{C_L V_{DD}}{(W/L)_n KP_n (V_{DD} - V_{ton})^2} \quad (6.29)$$

Key equation for the CMOS inverter high-to-low transition time.

Similarly, we have

$$t_{PLH} = \frac{C_L V_{DD}}{(W/L)_p K P_p (V_{DD} - |V_{top}|)^2} \quad (6.30)$$

Key equation for the CMOS inverter low-to-high transition time.

Examining Equations (6.29) and (6.30), we see that for fast switching of a CMOS inverter, we want the load capacitance C_L to be small, W/L to be large for both transistors, and KP to be large for both transistors [which in turn implies high surface mobilities (μ_n and μ_p), as well as a thin gate oxide layer]. Furthermore, the threshold voltages V_{ton} and V_{top} should be small in magnitude and the supply voltage V_{DD} should be high.

Besides the relationships given in Equations (6.29) and (6.30), there are many other circuit and process design issues to consider. For example, a high W/L implies a large chip area and a larger load capacitance for the driving gate. A high supply voltage is not compatible with thinner oxide because of breakdown. Taking all factors into account, smaller devices, thinner gate oxide, and a lower supply voltage lead to higher performance digital CMOS ICs. These are some of the major factors that drive the improvement in computer technology that we have experienced over the past decade and expect to continue for the next several decades.

Usually, the design process fixes the values of V_{DD} , KP_n , KP_p , V_{ton} , and V_{top} . The circuit designer can vary W/L for each of the transistors in a circuit, making sure to keep the smallest values of W and L larger than the minimum specified for the process. Also, the circuit designer can engineer the circuit layout to minimize load capacitance, especially for critical logic paths.

Taking all factors into account, smaller devices, thinner gate oxide, and a lower supply voltage lead to higher performance digital CMOS ICs.

Example 6.7 Calculation of CMOS Inverter Propagation Delay

Use Equations (6.29) and (6.30) to calculate the propagation delay for a CMOS inverter with $V_{DD} = 5\text{ V}$, $C_L = 1\text{ pF}$, and the following parameter values:

$$\begin{array}{ll} V_{ton} = 1\text{ V} & V_{top} = -1\text{ V} \\ KP_n = 50\text{ }\mu\text{A/V}^2 & KP_p = 25\text{ }\mu\text{A/V}^2 \\ \left(\frac{W}{L}\right)_n = \frac{4\text{ }\mu\text{m}}{1\text{ }\mu\text{m}} & \left(\frac{W}{L}\right)_p = \frac{8\text{ }\mu\text{m}}{1\text{ }\mu\text{m}} \\ \lambda_n = 0 & \lambda_p = 0 \end{array}$$

(These are the parameters for the CMOS inverter of Section 6.5 that has a symmetrical transfer characteristic.)

SOLUTION Substituting values into Equation (6.29) yields

$$t_{PHL} = \frac{C_L V_{DD}}{(W/L)_n K P_n (V_{DD} - V_{ton})^2} = 1.56\text{ ns}$$

From Equation (6.30), we obtain $t_{PLH} = 1.56\text{ ns}$. Notice that CMOS inverters designed to have a symmetrical transfer characteristic also have $t_{PHL} = t_{PLH}$. $\square$

In practice, a reasonable rule of thumb is to double the values computed with Equations (6.29) and (6.30).

Equations (6.29) and (6.30) are approximate because we assumed that the input voltage switches instantaneously. In actual digital circuits, inverters are driven by the output of other gates, and the input transitions are more gradual. Also, we assumed that $\lambda = 0$, which is not accurate for short-channel MOSFETs (L of a few microns or less). Finally, in many circuits point C (of Figure 6.35) falls on the left-hand side of point D , and the charge/discharge currents fall below the values we assumed in deriving the equations, resulting in slower transition times. In practice, a reasonable rule of thumb is to double the values computed with Equations (6.29) and (6.30).

Example 6.8 SPICE Simulation of CMOS Inverter Propagation Delay

Use PSpice to simulate the propagation delay of the CMOS inverter of Example 6.7. Cascade three inverters, each with a load capacitance of 1 pF, and determine the propagation delays of the output signal for the last inverter in the chain.

The file name for the simulation is Fig6.37.

SOLUTION The circuit is shown in Figure 6.37. We have set up the pulse input source to produce a 15-ns-wide 5-V pulse that starts at 1 ns. The input and output waveforms for the third inverter are illustrated in Figure 6.38. Using the Probe cursor, we find that $t_{PHL} = t_{PLH} = 2.97$ ns. This value is approximately double the value that we computed earlier (1.56 ns), due mainly to the fact that the input waveform does not switch instantly. As we mentioned earlier, a good rule of thumb for real circuits is to double the values computed from Equations (6.29) and (6.30).

EXERCISE

6.17 Use SPICE to determine t_{PHL} and t_{PLH} for the first inverter shown in Figure 6.37. Make sure that the rise and fall times of the pulse source are very short (say, 0.1 ns).

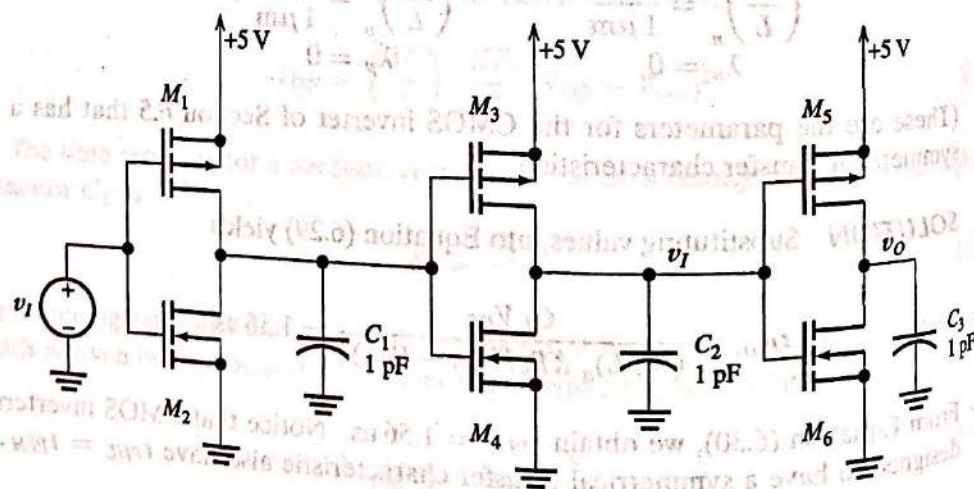


Figure 6.37 Cascade of three CMOS inverters.

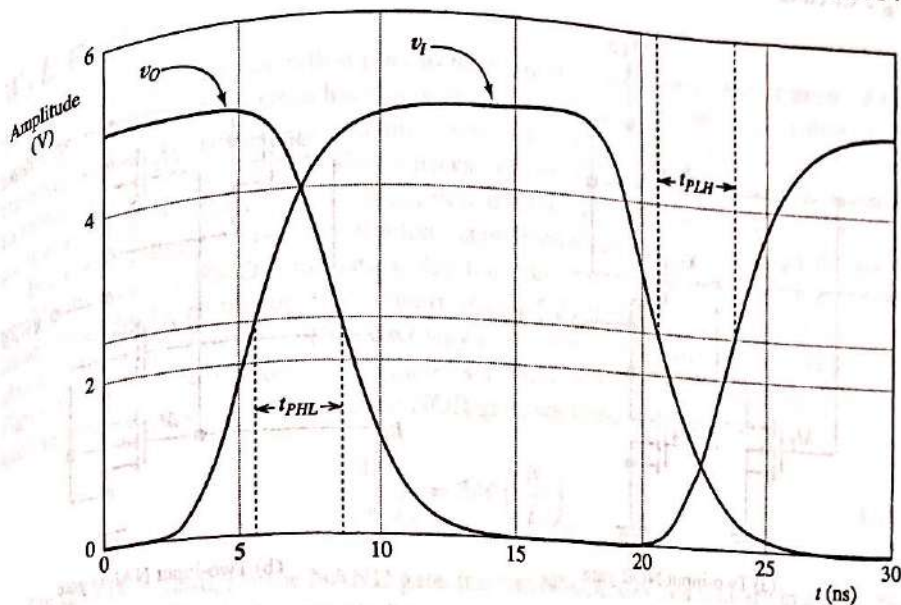


Figure 6.38 Waveforms for stage three of Figure 6.37.

Answer $t_{PHL} = t_{PLH} = 1.62$ ns. Notice that this value is in good agreement with the calculations of Example 6.7, because the input transitions are very fast.

EXERCISE

6.18 Repeat Example 6.8, setting $\lambda_n = \lambda_p = 0.1 \text{ V}^{-1}$. Determine the delays.

Answer $t_{PHL} = t_{PLH} = 2.33$ ns. The circuit schematic is stored in the file Exer6.18.

EXERCISE

6.19 Make approximate sketches versus time of the current through C_3 , the drain current of M_6 , and the drain current of M_5 , for the circuit of Figure 6.37.

Answer Verify your answers with the use of PSpice. Keep in mind that PSpice references currents into device terminals.

6.7 CMOS NOR and NAND GATES

The circuit diagram of a two-input CMOS NOR gate is shown in Figure 6.39a. If both inputs (A and B) are low, the PMOS transistors (M_1 and M_2) are conductive, and the NMOS transistors (M_3 and M_4) are cut off. Consequently, the output is high.

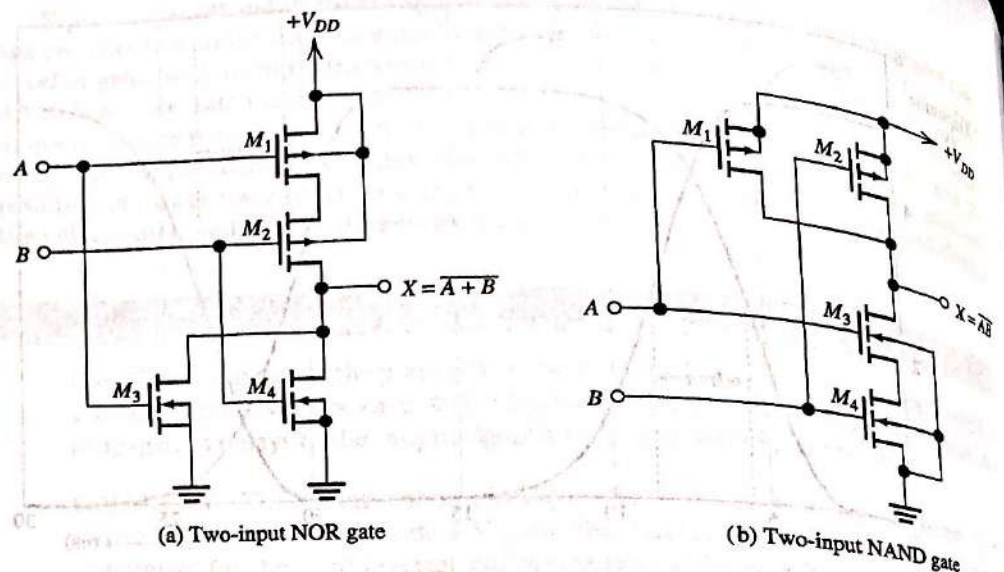


Figure 6.39 CMOS logic gates.

On the other hand, if either A or B (or both) are high, one (or both) of the PMOS devices is cut off. Furthermore, at least one of the NMOS devices is conductive. Consequently, the output is low. Thus, the circuit performs the NOR logic function.

A two-input CMOS NAND gate is shown in Figure 6.39b. By connecting more transistors in series and parallel, NAND and NOR gates with more than two inputs can be obtained. For example, Figure 6.40 shows a three-input NOR gate.

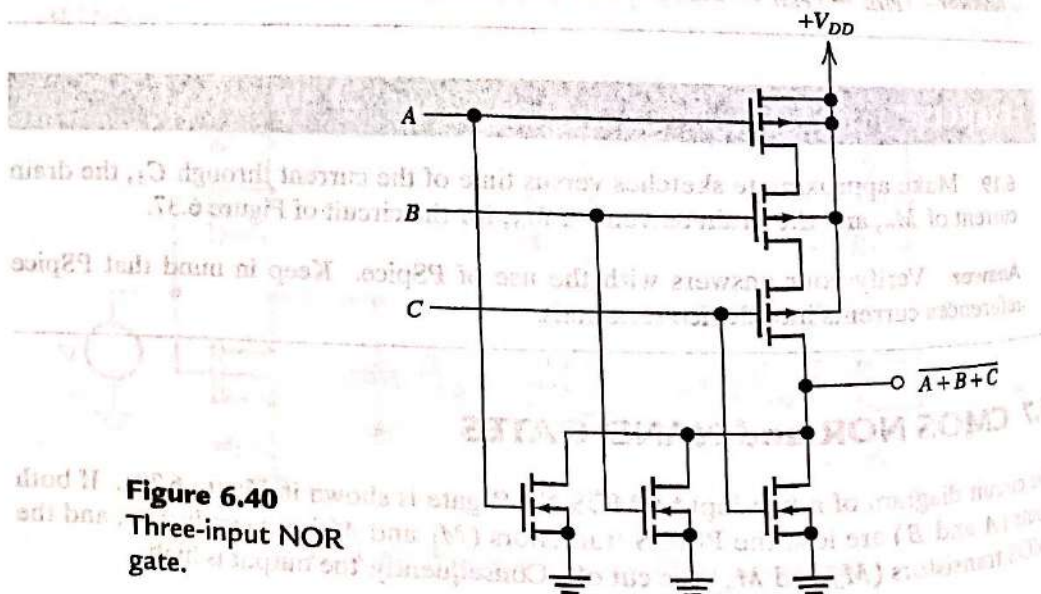


Figure 6.40 Three-input NOR gate.

CMOS NAND and NOR gates can be implemented with series- and parallel-connected NMOS and PMOS transistors.

W/L Ratios

To achieve symmetrical operation (i.e., to have $v_O = V_{DD}/2$ when one or more of the inputs is equal to $V_{DD}/2$ and to have $t_{PHL} = t_{PLH}$), we must select the W/L ratios of the transistors properly. Recall that to achieve symmetry in the case of the inverter, we need to select $(W/L)_p \cong 2(W/L)_n$. This is necessary because the electron surface mobility μ_n is approximately twice as large as the hole mobility μ_p , resulting in $KP_n \cong 2KP_p$.

For the two-input NOR gate, the load capacitance must charge through the series combination of two PMOS transistors. On the other hand, sometimes the load capacitance must discharge through only one of the NMOS transistors. Therefore, we must choose $(W/L)_p \cong 4(W/L)_n$. (Another way to see this is to realize that M_1 and M_2 of Figure 6.39a are in series, and they behave as a single device that is double the length of each separate device.) For an M -input NOR gate, we need to design for

$$\left(\frac{W}{L}\right)_p = 2M \left(\frac{W}{L}\right)_n \quad (6.31)$$

On the other hand, for the NAND gate, it is the NMOS devices that are in series. For an M -input NAND gate, we need to have

$$\left(\frac{W}{L}\right)_p = \frac{2}{M} \times \left(\frac{W}{L}\right)_n \quad (6.32)$$

Usually, one of the dimensions of each transistor is selected to be the minimum value allowed by the fabrication process in use. Thus, a large (W/L) ratio (compared to unity) requires a large die area. In general, to attain symmetrical characteristics, NAND gates require less chip area than NOR gates do. For this reason, most CMOS logic is based on NAND gates (and inverters), rather than NOR gates. (Recall that combinatorial logic circuits can be constructed of either NAND or NOR gates exclusively.)

Propagation Delay

In a manner parallel to the analysis of the propagation delay of an inverter, we can determine the propagation delays of the CMOS NAND gate. The delays are approximately

$$t_{PHL} = \frac{MC_L V_{DD}}{(W/L)_n KP_n (V_{DD} - V_{ton})^2} \quad (6.33)$$

and

$$t_{PLH} = \frac{C_L V_{DD}}{(W/L)_p KP_p (V_{DD} - |V_{top}|)^2} \quad (6.34)$$

The expression for t_{PLH} assumes that C_L is being charged through a single PMOS transistor, because that is the worst-case scenario. Therefore, the expression for t_{PLH} for the NAND gate is the same as for the inverter. On the other hand, C_L must discharge through a series connection of M NMOS devices, and that is the reason for the factor M in the numerator of the expression for t_{PHL} .

To attain a symmetrical transfer characteristic and $t_{PHL} = t_{PLH}$ for an M -input CMOS NOR gate, we must have $(W/L)_p = 2M(W/L)_n$. For a NAND gate, $(W/L)_p = (2/M)(W/L)_n$.

In general, to attain symmetrical characteristics, NAND gates require less chip area than NOR gates do. For this reason, most CMOS logic is based on NAND gates (and inverters), rather than NOR gates.

In a similar fashion, for the M -input NOR gate, we have

$$t_{PHL} = \frac{C_L V_{DD}}{(W/L)_n K P_n (V_{DD} - V_{ton})^2} \quad (6.35)$$

and

$$t_{PLH} = \frac{M C_L V_{DD}}{(W/L)_p K P_p (V_{DD} - |V_{top}|)^2} \quad (6.36)$$

Example 6.9 CMOS-NAND-Gate Design

Design a two-input CMOS NAND gate that has symmetrical transition times equal to 200 ps. The total load capacitance is $C_L = 200$ fF. (Recall that 1 fF = 1 femtofarad = 10^{-15} F.) This is a typical load capacitance for a gate with its load internal to the IC. Assume that $K P_n = 50 \mu\text{A}/\text{V}^2$, $K P_p = 25 \mu\text{A}/\text{V}^2$, $V_{DD} = 5$ V, and $V_{ton} = |V_{top}| = 1$ V.

SOLUTION Solving Equation (6.33) for $(W/L)_n$ and substituting values, we have

$$\begin{aligned} \left(\frac{W}{L}\right)_n &= \frac{M C_L V_{DD}}{t_{PHL} K P_n (V_{DD} - V_{ton})^2} \\ &= \frac{2(200 \times 10^{-15})5}{(200 \times 10^{-12})(50 \times 10^{-6})(5 - 1)^2} \\ &= 12.5 \end{aligned}$$

Now, using Equation (6.32), we obtain

$$\left(\frac{W}{L}\right)_p = \frac{2}{M} \times \left(\frac{W}{L}\right)_n = 12.5$$

Example 6.10 Effects of Back-Gate and Channel-Length Modulation

Use SPICE to plot the transfer characteristics for the NAND gate designed in Example 6.9, taking back-gate and channel-length modulation effects into account. Assume that the dimensions of all devices are $L = 1 \mu\text{m}$ and $W = 12.5 \mu\text{m}$. Use the typical values of the device parameters given in Table 6.1.

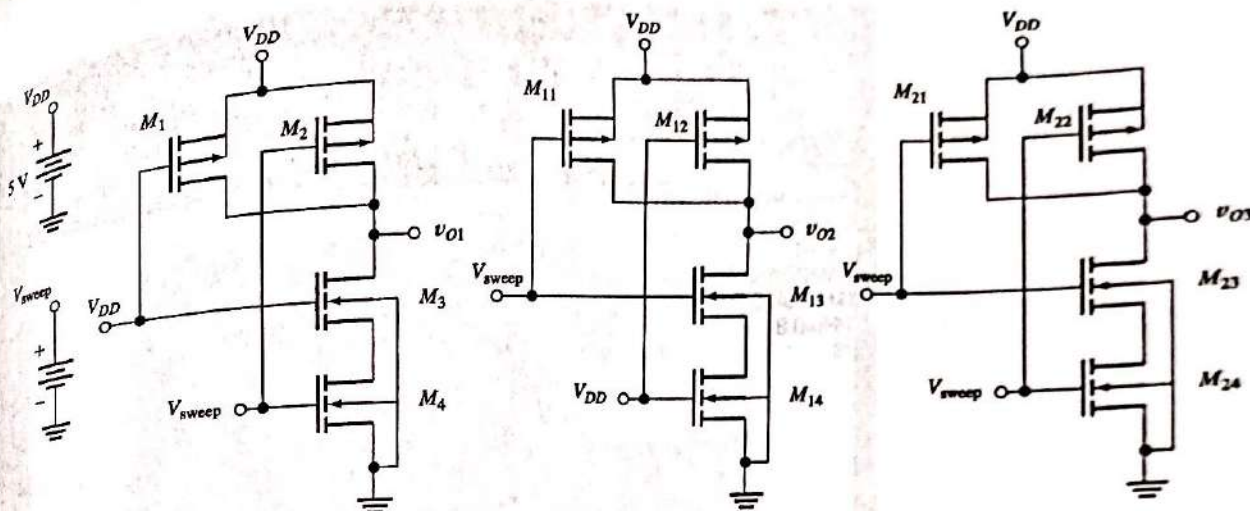


Figure 6.41 Circuits used to plot the transfer characteristics of a two-input NAND gate.

SOLUTION Because either of the inputs may switch while the other is high, or both may switch simultaneously, we need to plot three transfer characteristics:

- v_O versus v_A while v_B is high;
- v_O versus v_B while v_A is high;
- v_O versus v_B or v_A for $v_A = v_B$.

We have used Schematics to set up three versions of the circuit as illustrated in Figure 6.41. If we click on one of the PMOS devices to select it (it then turns red on the computer screen) and use the **edit/model/edit instance model** command, we bring up the window shown in Figure 6.42. Here, we enter the model parameters for the PMOS transistors. This process is repeated for the NMOS model. Then we double click on M_1 which brings up the window displayed in Figure 6.43. We then enter the length and width for M_1 and repeat the process for the remaining transistors.

Next, we use the **analysis/setup/dc sweep** command to bring up the window shown in Figure 6.44 to set up the parameters for sweeping the dc source V_{sweep} from 0 to 5 V in 0.01-V increments. Then we use the **analysis/simulate** command to initiate the simulation, after which Probe starts. Then we displayed the transfer characteristics illustrated in Figure 6.45. (This circuit is too large to run on the evaluation versions of PSpice. However, you can simulate two of the gates.)

Notice that the transfer characteristics are different, depending on which input(s) is (are) switching. This is partly due to short-channel effects ($\lambda \neq 0$) and body effects ($\phi \neq 0$ and $\gamma \neq 0$). Nevertheless, the transfer characteristics make their most rapid transitions close to an input voltage of $V_{DD}/2$, as desired. □

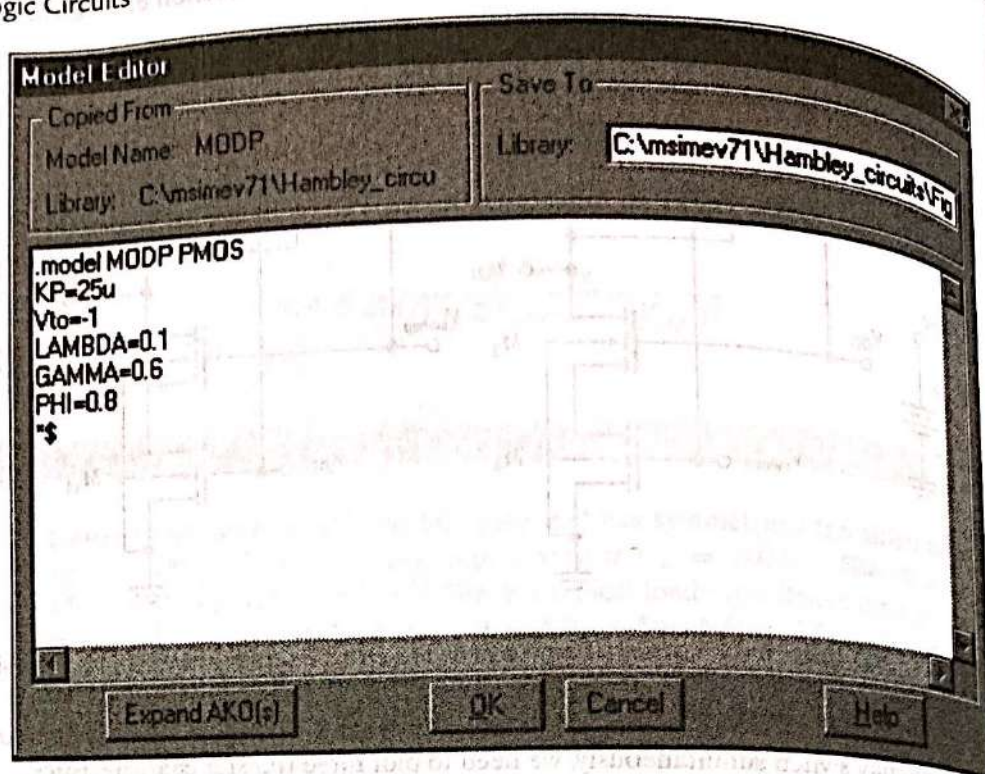
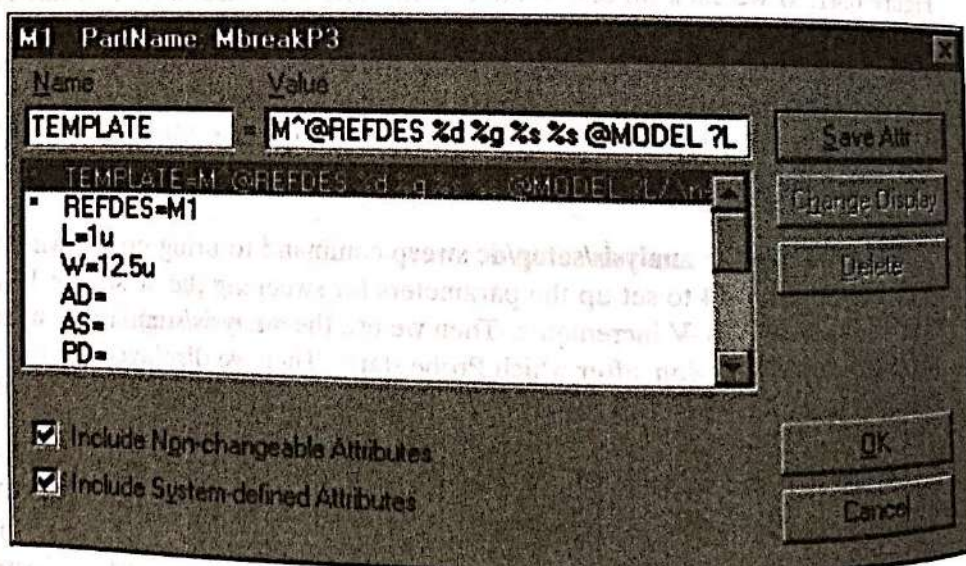


Figure 6.42 Model window.

Figure 6.43 Part window for M_1 .

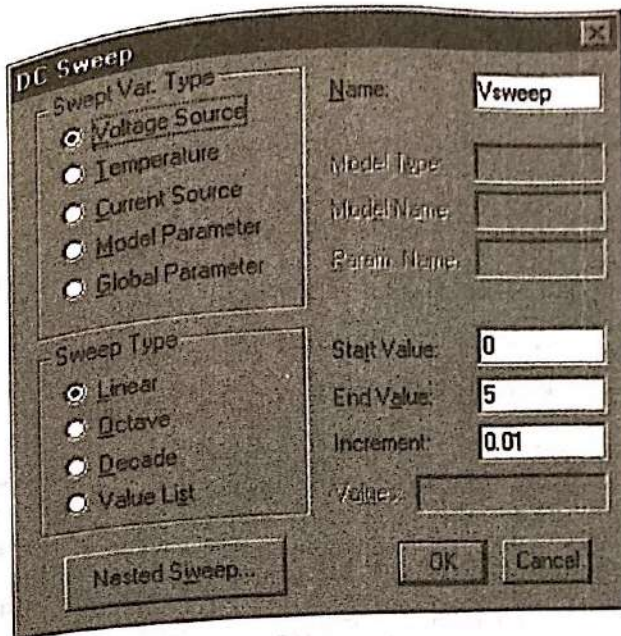


Figure 6.44 Setup window for V_{sweep} .

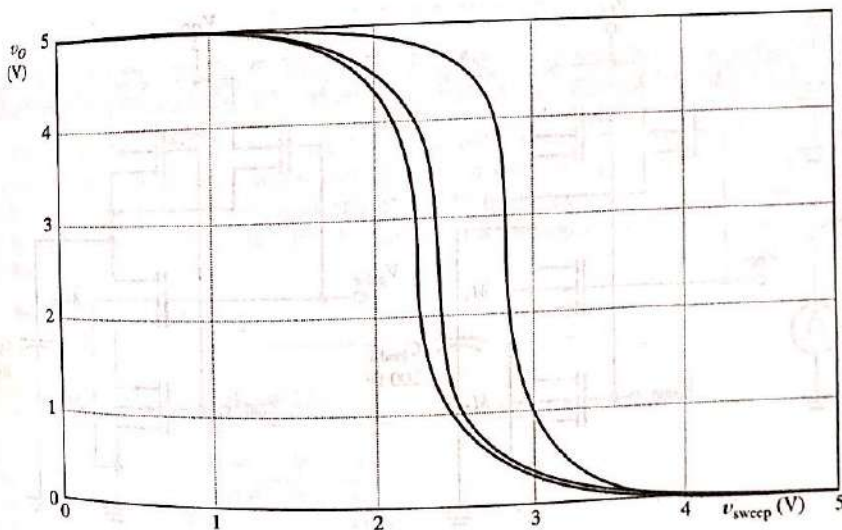


Figure 6.45 Transfer characteristics of a two-input NAND gate.

Example 6.11 Effects of Back-Gate and Channel-Length Modulation

Use SPICE to determine the propagation delays for the NAND gate designed in Example 6.9, taking back-gate and channel-length modulation effects into account.

SOLUTION Here again, because either of the inputs may switch while the other is high or both may switch simultaneously, we need to plot three switching transients:

v_O versus time for v_B high and v_A switching;

v_O versus time for v_A high and v_B switching;

v_O versus time for both v_A and v_B switching.

We have used PSpice to set up three versions of the circuit, two of which are illustrated in Figure 6.46. We set up the pulse source to produce a 5-V pulse with a duration of 1000 ps. Then we set up the transient analysis to simulate the circuit for a period of 1500 ps. The resulting input and output waveforms are shown in Figure 6.47. Using the cursor in Probe, we find that for all three output waveforms,

$$t_{PHL} = 192 \text{ ps}$$

It turns out that the output waveforms are the same for both cases in which only one input switches; the propagation delay is then

$$t_{PLH} = 151 \text{ ps}$$

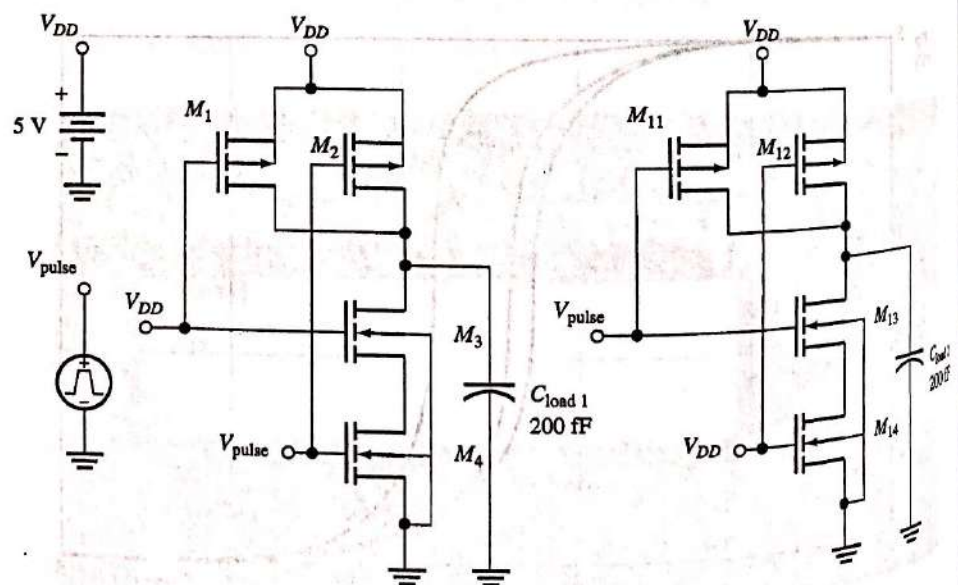


Figure 6.46 Circuits used to determine the propagation delays of the two-input NAND gate.

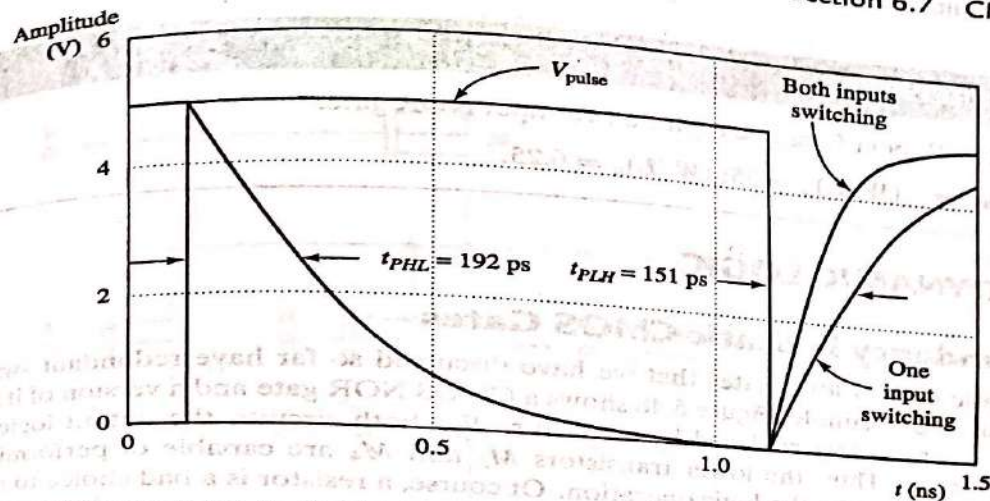


Figure 6.47 Switching transients of the two-input NAND gate.

On the other hand, when both inputs switch, we find that

$$t_{PLH} = 76 \text{ ps}$$

Of course, t_{PHL} is smaller when both inputs switch, because the load capacitance is charged through two PMOS transistors in parallel. (When only one input switches, the load capacitance charges through a single PMOS transistor.)

EXERCISE

6.20 For the circuit of Figure 6.39b, prepare a table showing all possible combinations of inputs (each input can be high or low), the corresponding state of each transistor, and the corresponding output. Indicate the state of each transistor either as *on* for operation in the triode and saturation regions or as *off* for operation in cutoff.

Answer See Table 6.3.

Table 6.3. Answer to Exercise 6.20.

A	B	M_1	M_2	M_3	M_4	X
Low	Low	On	On	Off	Off	High
Low	High	On	Off	Off	On	High
High	Low	Off	On	On	Off	High
High	High	Off	Off	On	On	Low

EXERCISE

6.21 Repeat Example 6.9 for a two-input NOR gate.

Answer $(W/L)_p = 25$; $(W/L)_n = 6.25$.

6.8 DYNAMIC LOGIC

Redundancy in Static CMOS Gates

The static CMOS logic gates that we have discussed so far have redundant switching functions. For example, Figure 6.48 shows a CMOS NOR gate and a version of it having the upper transistors replaced by a resistor. For both circuits, the output logic levels are the same. Thus, the lower transistors M_3 and M_4 are capable of performing the switching needed for the logic operation. Of course, a resistor is a bad choice to replace the transistors M_1 and M_2 , because resistors consume much more chip area than transistors do. Furthermore, using resistors results in static power dissipation when any of the inputs to the gate are high.

Dynamic NOR Gate

Figure 6.49 shows an M -input NOR gate based on a technology known as dynamic logic. Here, a clock signal ϕ controls the operation of the gate. The desired output is available only when the clock signal is high.

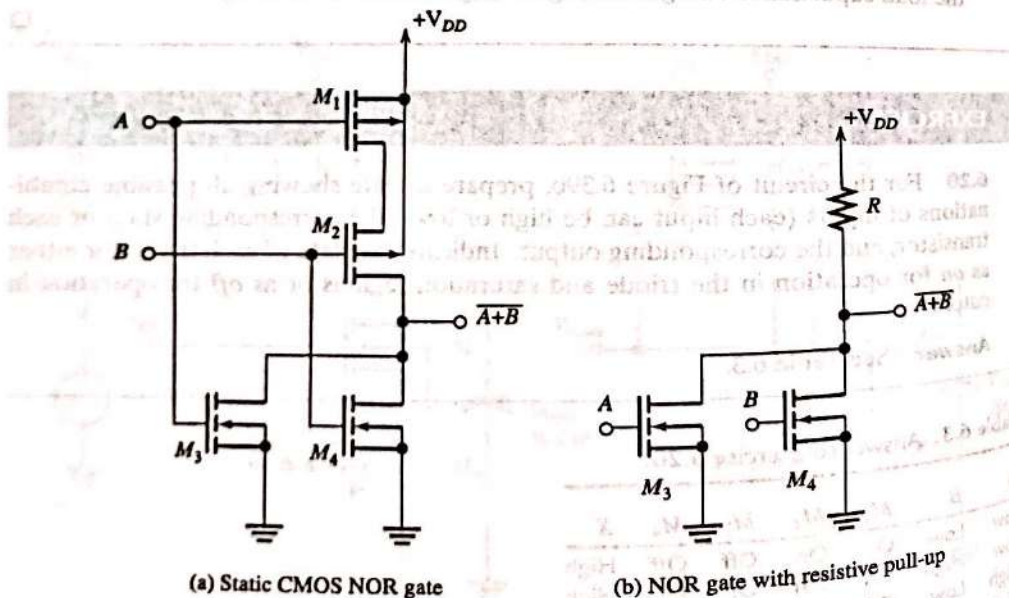


Figure 6.48 Static CMOS gates contain redundant switching functions.

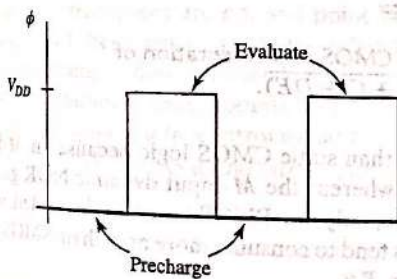
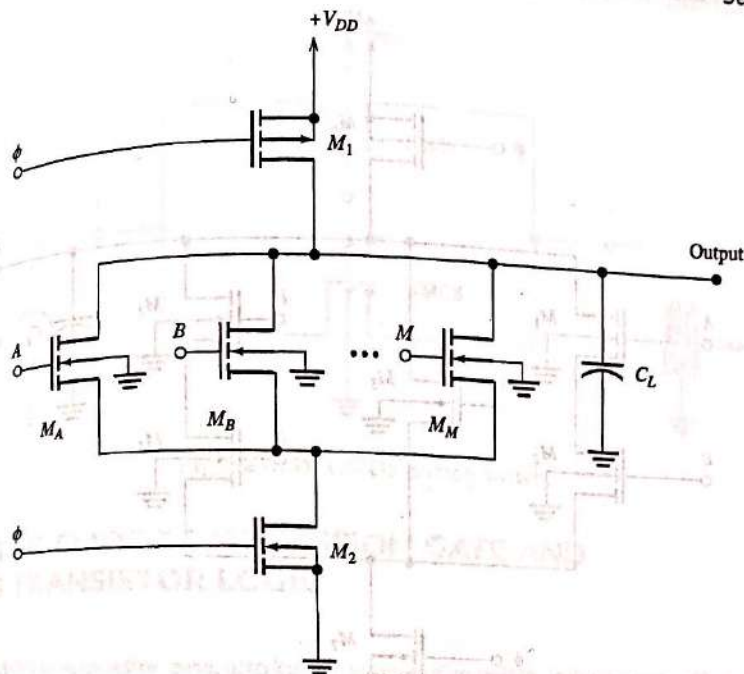


Figure 6.49 Dynamic logic NOR gate.

Let us consider the operation of the circuit. When ϕ is low, M_1 is on and M_2 is off. Hence, the load capacitance C_L is charged to V_{DD} independently of the input logic signals $A, B, \dots$, and M .

When ϕ is high, M_1 is off and M_2 is on. If all of the inputs are low, the transistors $M_A, M_B, \dots, M_M$ are off. Then the output remains high because there is no discharge path for C_L . On the other hand, if any of the inputs are high, C_L is discharged through the series path consisting of M_A and M_2 . Therefore, the output during the time that the clock is high is the NOR combination of the inputs.

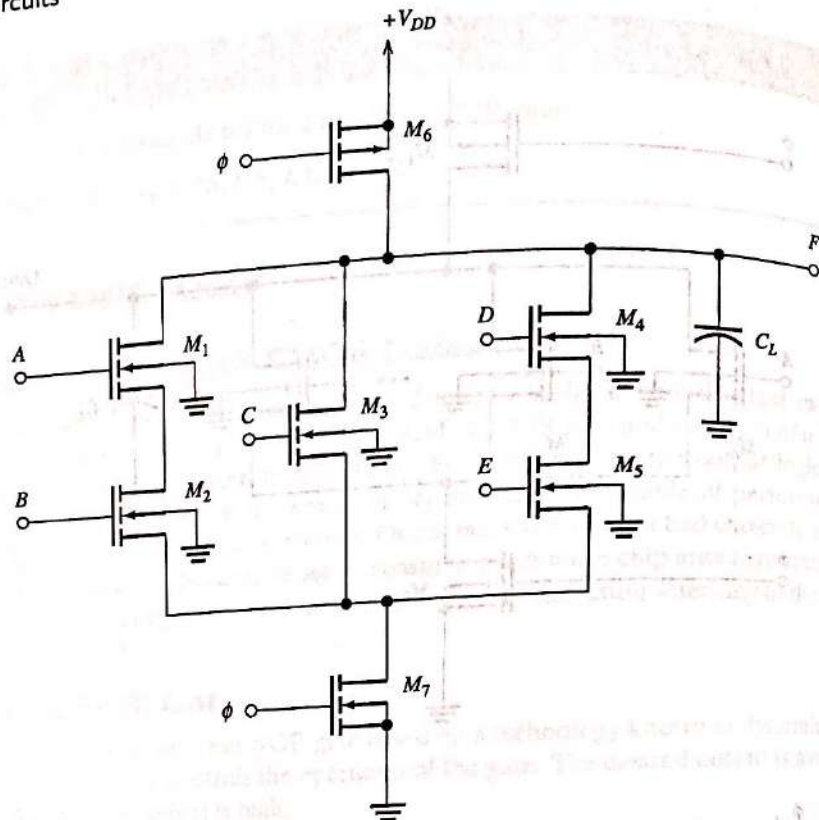


Figure 6.50 Dynamic CMOS implementation of $F = (AB + C + DE)$.

Dynamic logic requires less chip area than static CMOS logic...

Dynamic logic circuits are controlled by clock signals. First, the load capacitance is precharged to V_{DD} through a PMOS switch, then the capacitance is discharged through a network of NMOS switches that are controlled by the input logic variables. The chief advantage of dynamic logic is that it saves chip area.

Dynamic logic requires less chip area than static CMOS logic because an M -input static NOR gate requires $2M$ transistors, whereas the M -input dynamic NOR gate requires only $M + 2$ transistors. Furthermore, only one PMOS transistor is needed, which is advantageous because PMOS transistors tend to consume more area than NMOS transistors, due to the fact that KP_p is less than KP_n .

Complex logic functions can be implemented in dynamic CMOS logic by connecting the NMOS transistors in series and/or parallel. For example, the circuit displayed in Figure 6.50 implements the logic function $F = (AB + C + DE)$. Complex logic functions can be compactly implemented using dynamic logic.

EXERCISE

6.22 Draw the circuit diagram of an M -input dynamic NAND gate.

Answer The circuit is the same as the NOR gate shown in Figure 6.49, except that the transistors $M_A, M_B, \dots, M_M$ must be connected in series rather than parallel.

6.9 1 PASS

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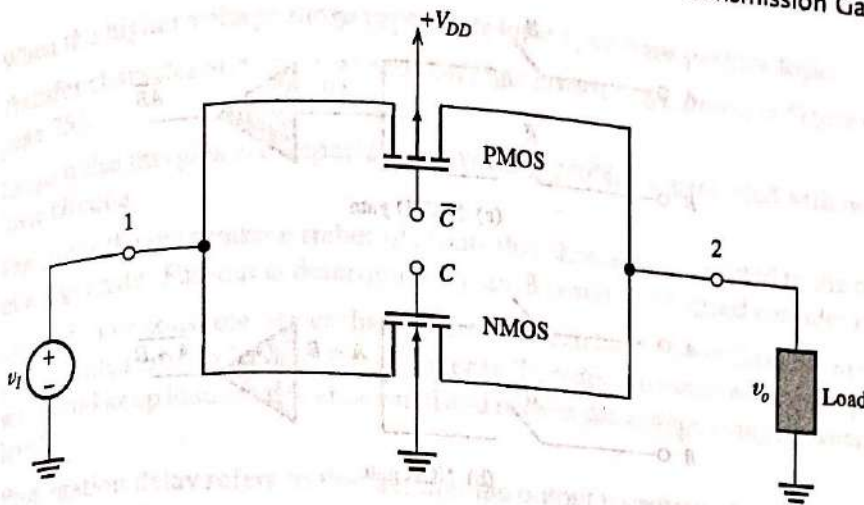


Figure 6.51 CMOS analog switch.

6.9 THE CMOS TRANSMISSION GATE AND PASS TRANSISTOR LOGIC

The **CMOS transmission gate**, also known as an **analog switch**, is illustrated in Figure 6.51. The circuit consists of an NMOS and a PMOS transistor in parallel. The gates of the transistors are connected to a logic control signal C and its complement $\bar{C}$. When C is high, the transistors are on, and point 1 is connected to point 2 through the low on resistance of the transistors. On the other hand, when C is low, the transistors are off, so current cannot flow between points 1 and 2. Thus, the circuit acts as an electronic switch that either connects points 1 and 2 through a low resistance or disconnects them, depending on the digital control signal C .

The equivalent circuit and circuit symbol for the transmission gate are displayed in Figure 6.52.

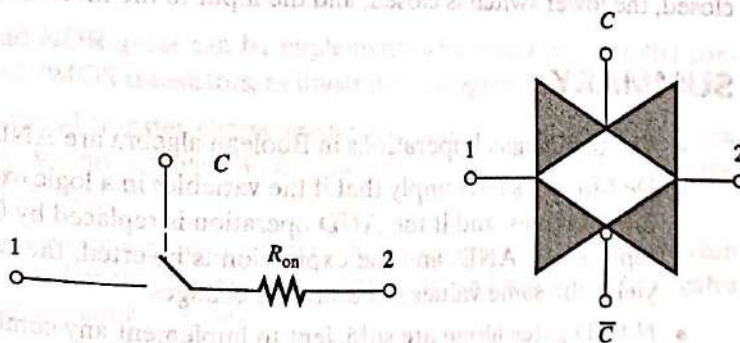
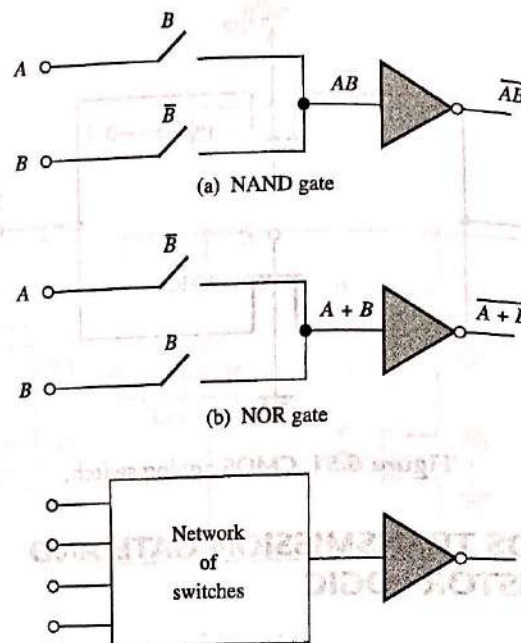


Figure 6.52

Equivalent circuit and symbol for the CMOS transmission gate.

(a) Equivalent circuit in which the switch is closed if C is high and open if C is low (the on resistance R_{on} is nonlinear)

(b) Circuit symbol



(c) Complex logic operations can be compactly implemented with a network of switches

Figure 6.53 Pass transistor logic.

Pass Transistor Logic

An analog switch can be implemented by placing an NMOS and a PMOS transistor in parallel. Pass transistor logic is implemented with this type of switch.

CMOS transmission gates are useful in implementing **pass transistor logic** functions, as shown in Figure 6.53. The logic operations are formed by the switch network. The inverter is needed mainly to provide a low-impedance output. For example, for the NAND gate, if A and B are both low, the upper switch is open, the lower switch is closed, and the input to the inverter is low. Similarly when both A and B are high, the upper switch is closed, the lower switch is closed, and the input to the inverter is high.

SUMMARY

- The basic logical operations in Boolean algebra are AND, OR, and NOT.
- De Morgan's laws imply that if the variables in a logic expression are replaced by their inverses, and if the AND operation is replaced by OR, the OR operation is replaced by AND, and the expression is inverted, the resulting logic expression yields the same values as before the changes.
- NAND gates alone are sufficient to implement any combinatorial logic function. The same is true of NOR gates.
- For a given logic family, one range of output voltages represents logic 1, and another range of voltages represents logic 0. For proper operation, a logic circuit only needs to produce a voltage somewhere in the correct range.

- When the higher voltage range represents logic 1, we have positive logic.
- Transfer characteristics of ideal and real logic inverters are shown in Figure 6.9 on page 355.
- Large noise margins are important in avoiding problems associated with noise in logic circuits.
- Fan-out is the maximum number of inputs that should be connected to the output of a logic gate. Fan-out is determined by drive current and speed considerations.
- Logic circuits consume power that is converted into heat. Power dissipation can be divided into static and dynamic components. To reduce dynamic power dissipation, we should keep load capacitance small and restrict the voltage swing between logic levels.
- Propagation delay refers to the fact that the output transition of a gate is delayed compared with the transition(s) of the input(s).
- The resistor-pull-up NMOS inverter is a good circuit for illustrating many of the important concepts of logic gate design. However, it is not practical because of the large chip area needed for the resistors, high static power dissipation, and low speed.
- Improved versions of the MOS inverter substitute MOS transistors for the load resistor, as shown in Figure 6.25 on page 377.
- An important advantage of CMOS logic is zero static power dissipation.
- Because PMOS devices have a KP_p value that is about half of KP_n , we need to choose $(W/L)_p = 2(W/L)_n$ to achieve a symmetrical transfer characteristic for a CMOS inverter.
- For fast switching of a CMOS inverter, the load capacitance C_L should be small, W/L should be large for both transistors, and KP should be large for both transistors [which in turn implies high surface mobilities (μ_n and μ_p), as well as a thin gate oxide layer].
- Smaller devices and lower supply voltages lead to higher performance digital CMOS ICs.
- CMOS NAND and NOR gates can be implemented by series and parallel connecting NMOS and PMOS transistors, as illustrated in Figure 6.39 on page 392.
- To attain a symmetrical transfer characteristic and $t_{PHL} = t_{PLH}$ for an M -input CMOS NOR gate, we must have $(W/L)_p = 2M(W/L)_n$. For a NAND gate, $(W/L)_p = (2/M)(W/L)_n$.
- In general, to attain symmetrical characteristics, NAND gates require less chip area than NOR gates. For this reason, most CMOS logic is based on NAND gates (and inverters) rather than NOR gates.
- Approximate expressions for the propagation delays of CMOS NAND and NOR gates are given in Equations (6.33) through (6.36) on pages 393–394.
- Dynamic logic circuits are controlled by clock signals. First, the load capacitance is precharged to V_{DD} through a PMOS switch. Then the capacitance is discharged

through a network of NMOS switches that are controlled by the input logic variables. The chief advantage of dynamic logic is that it saves chip area.

- An analog switch can be implemented by placing an NMOS and a PMOS transistor in parallel. Pass transistor logic is implemented with this type of switch.

PROBLEMS

Section 6.1: Basic Concepts

- 6.1. What is a truth table?
- 6.2. State De Morgan's laws in equation form.
- 6.3. Give the circuit symbol and truth table for an AND gate, an OR gate, an inverter, a NAND gate, a NOR gate, and an XOR gate. Assume two inputs for each gate (except the inverter).
- 6.4. Describe a method for proving the validity of a Boolean algebra equation.
- 6.5. List the truth table for each of these Boolean expressions:
 - (a) $D = ABC + \overline{A}\overline{B}$;
 - (b) $E = AB + \overline{A}\overline{B}C + \overline{C}D$;
 - (c) $Z = WX + (W + Y)$.
- 6.6. Write a Boolean expression for the output of each of the logic circuits illustrated in Figure P6.6.

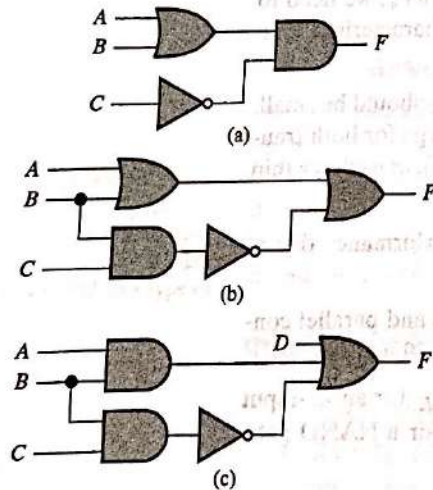


Figure P6.6

- 6.7. Use a truth table to prove that

$$(A + B)(\overline{A} + \overline{B}) = \overline{A}B + A\overline{B}$$
- 6.8. Use a truth table to prove that

$$(A + B)(A + C) = A + BC$$

- 6.9. Use a truth table to prove that

$$A + \overline{A}B = A + B$$

- 6.10. Draw a circuit to realize each of the following expressions using AND gates, OR gates, and inverters:
 - (a) $F = A + \overline{B}C$;
 - (b) $F = A\overline{B}C + AB\overline{C} + \overline{A}BC$;
 - (c) $F = (\overline{A} + \overline{B} + C)(A + B + \overline{C})(A + \overline{B} + C)$.

- 6.11. Apply De Morgan's laws to each of these expressions:
 - (a) $F = AB + (\overline{C} + A)\overline{D}$;
 - (b) $F = A(\overline{B} + C) + D$;
 - (c) $F = A\overline{B}C + A(B + C)$.

Section 6.2: Electrical Specifications for Logic Gates

- 6.12. Define V_{IL} , V_{IH} , V_{OL} , V_{OH} , NM_L , NM_H , I_{IL} , I_{IH} , I_{OL} , and I_{OH} .
- 6.13. If the output of a logic inverter is sourcing current, what is the direction of current flow?
- 6.14. Define the term *fan-out*.
- 6.15. Define the terms *static power dissipation* and *dynamic power dissipation* of a logic inverter.
- 6.16. A 100-fF load capacitance is driven by an inverter with a switching frequency of 400 Hz and an amplitude of $V_{DD} = 3V$. Determine the dynamic power dissipated.
- 6.17. Sketch a pulse input to a logic inverter and the corresponding output versus time. Label the rise time and fall time of the output pulse. Also, label the propagation delays t_{PLH} and t_{PLH} .
- 6.18. Define the term *speed-power product* for a logic inverter.
- 6.19. An ideal logic inverter operates from a power-supply voltage of 5 V. Sketch its transfer characteristic to scale.
- 6.20. A certain logic family has $V_{OL} = 1V$, $V_{OH} = 4.5V$, $V_{IL} = 1.5V$, and $V_{IH} = 3V$. Determine the noise margins.
- 6.21. Draw a logic circuit that produces a *glitch*. Sketch typical waveforms and identify the glitch.
- 6.22. The transfer characteristic of a certain logic inverter is shown in Figure P6.22. If the output is connected to the input, what output voltage results?

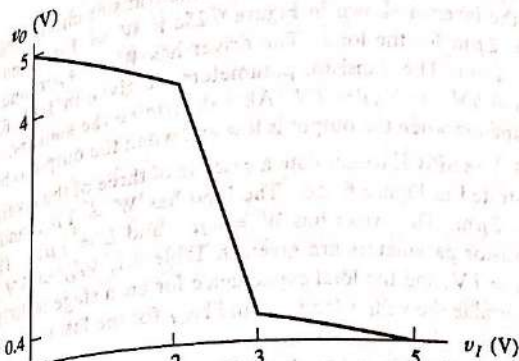


Figure P6.22

6.23. The circuit diagram of a certain logic inverter is shown in Figure P6.23. The electronic switch is closed if v_I is greater than 3.5 V and open if v_I is less than 2 V. For v_I between 2 V and 3.5 V, the state of the switch is indeterminate. Specifications for the gate give $I_{OH} = -0.5$ mA (i.e., the output can source 0.5 mA in the high state) and $I_{OL} = 1$ mA (i.e., the output can sink 1 mA in the low state). Find V_{IL} , V_{IH} , V_{OL} , and V_{OH} . Also, find the noise margins.

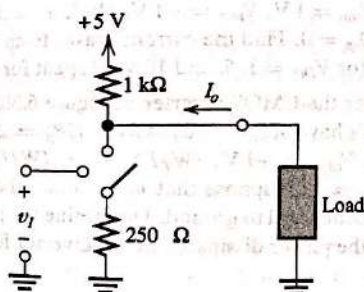


Figure P6.23

6.24. The power dissipation of a certain digital circuit is 1.5 W for a clock frequency of 10 MHz. If the clock frequency is raised to 20 MHz, the power dissipation becomes 2.5 W. Find the static power dissipation. Also, find the dynamic power dissipation for each clock frequency.

6.25. The logic inverter of Figure 6.14 has $V_{DD} = 5$ V and switches at a frequency of 25 MHz. The output levels are 0 V and 5 V. The load capacitance is 20 pF. Find the dynamic power dissipation.

6.26. Figure P6.26 shows the simplified circuit diagram of a logic inverter.

(a) Assuming an open-circuit load, find V_{OH} and V_{OL} .

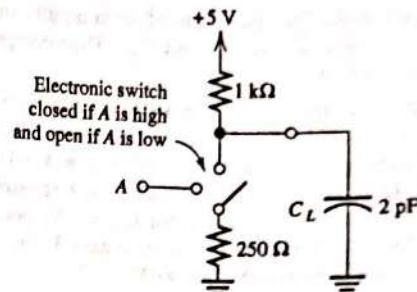


Figure P6.26

(b) Find the values of t_{PHL} , t_{PLH} , and t_{PD} . Assume an input pulse that switches abruptly between logic levels.

(c) Find the static power dissipation if the output is high. Repeat for a low output.

6.27. A certain logic family has $I_{OH} = -3$ mA, $I_{OL} = 2$ mA, $I_{IH} = 0.5$ mA, and $I_{IL} = -0.5$ mA. Determine the maximum fan-out allowed for this family.

Section 6.3: The Resistor-Pull-Up NMOS Inverter

6.28. Draw the circuit diagram of a resistor-pull-up NMOS inverter. Of a two-input NOR gate.

6.29. Explain why we need to design the resistor-pull-up NMOS inverter so that $R_D \gg R_{on}$.

6.30. If we wish to decrease the static power dissipation (in the low output state) of a resistor-pull-up inverter, should we increase or decrease (a) R_D ? (b) W ? (c) L ? (d) V_{DD} ?

6.31. List the advantages and disadvantages of increasing the value of R_D for a resistor-pull-up NMOS inverter.

D6.32. Resistor-pull-up MOS inverter design. Design a resistor-pull-up MOS inverter to meet the following objectives:

Static power consumption in low output state = 0.10 mW;

$$V_{OL} = 0.5 \text{ V};$$

$$V_{OH} = V_{DD} = 5 \text{ V};$$

Transistor: $V_{to} = 1$ V, $K_P = 50 \mu\text{A/V}^2$, $\lambda = 0$. Look at Example 6.1 on page 367.

6.33. Use SPICE to plot the drain characteristics for the transistor of Problem 6.32. Then perform a load-line analysis of the inverter to verify that the desired values for V_{OL} and V_{OH} have been achieved for the inverter designed in Problem 6.32.

6.34. Use SPICE to obtain the transfer characteristic of the inverter that we designed in Problem 6.32. Assume that the load

capacitance is zero. Use the results of the computer simulation to determine the values of V_{IL} and V_{IH} . Then compute the noise margins for this inverter.

6.35. Suppose we are designing an ASIC with NMOS transistors that have $V_{to} = 1\text{ V}$, $V_{DD} = 5\text{ V}$, and $KP = 50\text{ }\mu\text{A/V}^2$. A transistor having an on resistance (with $v_{GS} = V_{DD}$) of $2\text{ k}\Omega$ is needed. Determine the W/L ratio for the transistor. Then use SPICE to plot i_D against v_{DS} for $v_{GS} = 5\text{ V}$. Next, plot i against v for a $2\text{-k}\Omega$ resistor on the same axes. For what values of v do the two plots match fairly well?

6.36. A certain resistor-pull-up NMOS inverter has $W/L = 4$, $R_D = 50\text{ k}\Omega$, $V_{DD} = 5\text{ V}$, $V_{to} = 1\text{ V}$, $KP = 50\text{ }\mu\text{A/V}^2$, and $\lambda = 0.05$. Determine the noise margins for this inverter.

Section 6.4: Dynamic Response of the Resistor-Pull-Up NMOS Inverter

6.37. Why is the analysis of t_{PHL} more difficult than the analysis of t_{PLH} for a resistor-pull-up inverter?

6.38. If we wish to improve the switching speed of a resistor-pull-up inverter, should we increase or decrease (a) R_D (b) W (c) L (d) V_{DD} ?

6.39. Compute the rise time and t_{PLH} for a resistor-pull-up inverter that has $R_D = 100\text{ k}\Omega$, $W/L = 1$, $V_{to} = 1\text{ V}$, $V_{DD} = 5\text{ V}$, $KP = 50\text{ }\mu\text{A/V}^2$, and a load capacitance of 200 fF . Then use SPICE to determine t_{PHL} . Neglect short-channel effects (i.e., assume that $\lambda = 0$).

6.40. Consider the inverter shown in Figure P6.40. When the input v_I is high, the switch is closed, and when the input is low, the switch is open. Derive an expression for t_{PHL} in terms of the resistances and the load capacitance.

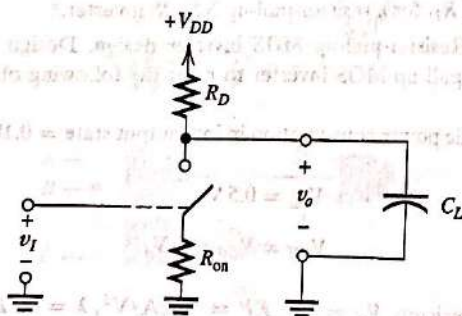


Figure P6.40

6.41. Use SPICE to simulate a cascade of three resistor-pull-up inverters, each of which has $R_D = 100\text{ k}\Omega$, $W/L = 1$, $V_{to} = 1\text{ V}$, $V_{DD} = 5\text{ V}$, $KP = 50\text{ }\mu\text{A/V}^2$, $\lambda = 0.1$, and a load capacitance of 200 fF . Determine the values for t_{PHL} and t_{PLH} for the last inverter in the chain.

6.42. Use SPICE to obtain a plot of the transfer characteristic for the inverter shown in Figure 6.25c if $W = 1\text{ }\mu\text{m}$ and $L = 2\text{ }\mu\text{m}$ for the load. The driver has $W = 4\text{ }\mu\text{m}$ and $L = 1\text{ }\mu\text{m}$. The transistor parameters are given in Table 6.1, $V_{DD} = 5\text{ V}$ and $V_{GG} = 7\text{ V}$. Also, determine the static power dissipation when the output is low and when the output is high.

6.43. Use SPICE to simulate a cascade of three of the inverters illustrated in Figure 6.25c. The load has $W = 1\text{ }\mu\text{m}$ and $L = 2\text{ }\mu\text{m}$. The driver has $W = 4\text{ }\mu\text{m}$ and $L = 1\text{ }\mu\text{m}$. The transistor parameters are given in Table 6.1, $V_{DD} = 5\text{ V}$, $V_{GG} = 7\text{ V}$, and the load capacitance for each stage is 200 fF . Determine the values for t_{PHL} and t_{PLH} for the last inverter in the chain.

6.44. Plot the threshold voltage V_{ton} against v_{BS} for an NMOS transistor having the parameters listed in Table 6.1. Allow v_{BS} to range from 0 to -5 V .

Section 6.5: The CMOS Inverter

6.45. Draw the circuit diagram of a CMOS inverter.

6.46. Of what does the input impedance of a CMOS inverter consist?

6.47. What is the static power consumption of a CMOS inverter?

6.48. Consider the CMOS inverter shown in Figure 6.30a. Assume that the FETs have $KP_n = 50\text{ }\mu\text{A/V}^2$, $KP_p = 25\text{ }\mu\text{A/V}^2$, $V_{ton} = 1\text{ V}$, $V_{top} = -1\text{ V}$, $(W/L)_n = 3$, $(W/L)_p = 6$, and $\lambda_n = \lambda_p = 0$. Find the current drawn from the source if $v_I = V_{DD}/2$ for $V_{DD} = 3, 5$, and 10 V . Repeat for $v_I = 0$.

6.49. Consider the CMOS inverter of Figure 6.30a. Assume that the FETs have $KP_n = 50\text{ }\mu\text{A/V}^2$, $KP_p = 25\text{ }\mu\text{A/V}^2$, $V_{ton} = 1\text{ V}$, $V_{top} = -1\text{ V}$, $(W/L)_n = 3$, $(W/L)_p = 6$, and $\lambda_n = \lambda_p = 0$. Suppose that $v_I = 0$ and the output is accidentally connected to ground. Determine the power-supply current and the power dissipated in the inverter for $V_{DD} = 3, 5$, and 10 V .

6.50. Consider the CMOS inverter of Figure 6.30a with $V_{DD} = 5\text{ V}$. Assume that the FETs have $KP_n = 50\text{ }\mu\text{A/V}^2$, $KP_p = 25\text{ }\mu\text{A/V}^2$, $V_{ton} = 1\text{ V}$, $V_{top} = -1\text{ V}$, $(W/L)_n = 3$, $(W/L)_p = 6$, and $\lambda_n = \lambda_p = 0$. If the input is high, how much current does the output sink when $v_O = 0.5\text{ V}$? If the input is low, how much current does the output source for $v_O = 4.5\text{ V}$?

D6.51. **TTL/CMOS interface design.** Suppose that we want to drive a CMOS inverter with the output of a TTL circuit. Both circuits are powered from a common 5-V supply. The logic levels for the TTL circuit are $V_{OH} = 2.4\text{ V}$ and $V_{OL} = 0.8\text{ V}$. Clearly, these input levels are not compatible with a symmetrical CMOS inverter having a transfer characteristic like that shown in Figure 6.32. Therefore, we need to design an asymmetrical CMOS inverter that makes its most rapid transition for an input

voltage of $\frac{1}{2}(2.4 + 0.8) = 1.6$ V. Assume that the MOSFETs have $KP_n = 50 \mu\text{A}/\text{V}^2$, $KP_p = 25 \mu\text{A}/\text{V}^2$, $V_{\text{ton}} = 1$ V, $V_{\text{top}} = -1$ V, and $\lambda_n = \lambda_p = 0$. If $(W/L)_p = 2$, use trial and error with SPICE to determine the value required for $(W/L)_n$. Use SPICE to plot the transfer characteristic of the inverter. If we design an inverter with $(W/L)_p = 2(W/L)_n$, the most rapid transition of the output occurs for $v_i = V_{\text{DD}}/2$. Think about which transistor must be made wider for the rapid transition to occur at a lower value of v_i . Then pick values for the (W/L) ratios, simulate the circuit and display the transfer characteristic. Adjust the ratios by trial and error until the desired performance is obtained.

6.52. Sometimes, conserving chip area is more important than noise margins and propagation delays. If so, we might design all of the transistors to have minimal length and width. Use SPICE to obtain a plot of the transfer characteristics of a CMOS inverter with $(W/L)_n = (W/L)_p = 1 \mu\text{m}/1 \mu\text{m}$ for $V_{\text{DD}} = 5$ V. Use the transistor parameters given in Table 6.1.

D6.53. CMOS/TTL interface design. Suppose that we need to design a CMOS inverter to drive the input of a TTL circuit. In the low-output case, the CMOS inverter must sink at least 1.5 mA while maintaining an output voltage of at most 0.8 V. In the high output case, the CMOS inverter must source at least 60 μA while maintaining an output voltage of at least 2.4 V. The supply voltage is $V_{\text{DD}} = 5$ V. Assume that the MOSFETs have $KP_n = 50 \mu\text{A}/\text{V}^2$, $KP_p = 25 \mu\text{A}/\text{V}^2$, $V_{\text{ton}} = 1$ V, $V_{\text{top}} = -1$ V, and $\lambda_n = \lambda_p = 0$. Determine the required values for $(W/L)_n$ and $(W/L)_p$. First determine the (W/L) ratio required for the NMOS so it can sink the desired current in the low state. Then determine the (W/L) ratio required for the PMOS so it can source the desired current in the high state. Finally, think about adjusting the ratios to reduce the chip space required.

6.54. Let us investigate the effect of W/L on noise margins for CMOS inverters. As in Example 6.3, we can define V_{IH} and V_{IL} to be the input voltages for which the transfer characteristic has a slope of -1 . Use the transistor parameters of Table 6.1 and SPICE to determine noise margins for inverters with

- $(W/L)_n = 3 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 6 \mu\text{m}/1 \mu\text{m}$;
- $(W/L)_n = 3 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 60 \mu\text{m}/1 \mu\text{m}$;
- $(W/L)_n = 30 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 6 \mu\text{m}/1 \mu\text{m}$.

6.55. Consider the transfer characteristic of the CMOS inverter shown in Figure 6.32. Because we assumed that $\lambda_n = \lambda_p = 0$, the section of the transfer characteristic is vertical between points C and D. Now let us assume that $\lambda_n = \lambda_p = \lambda$ is not zero, that $-V_{\text{top}} = V_{\text{ton}} = V_{\text{to}}$ and that $K_n = K_p$. Derive an expression for the slope of the transfer characteristic while both transistors are in the saturation region in terms of V_{to} , λ , and V_{DD} . (Hints: dv_o/dv_i

is the small-signal voltage gain of the circuit at the bias point $v_i = v_o = V_{\text{DD}}/2$. Thus draw the small-signal equivalent circuit and derive an expression for the voltage gain in terms of g_m and r_d . Finally, determine g_m and r_d in terms of the circuit parameters and substitute into the gain expression.)

Section 6.6: Propagation Delay of the CMOS Inverter

6.56. List the assumptions that were used in deriving Equation (6.29).

6.57. Suppose that a certain inverter in a digital CMOS IC is found to have switching speeds (t_{PHL} and t_{PLH}) that are 25% too high. What parameter(s) should the circuit designer change to correct this problem? By how much?

6.58. Let us investigate the effect of W/L on switching speeds for CMOS inverters having $V_{\text{DD}} = 5$ V and load capacitances of 2 pF. Assume that the MOSFETs have $KP_n = 50 \mu\text{A}/\text{V}^2$, $KP_p = 25 \mu\text{A}/\text{V}^2$, $V_{\text{ton}} = 1$ V, $V_{\text{top}} = -1$ V, and $\lambda_n = \lambda_p = 0$. Compute t_{PHL} and t_{PLH} for inverters with

- $(W/L)_n = 3 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 6 \mu\text{m}/1 \mu\text{m}$;
- $(W/L)_n = 3 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 60 \mu\text{m}/1 \mu\text{m}$;
- $(W/L)_n = 30 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_p = 6 \mu\text{m}/1 \mu\text{m}$.

6.59. Consider a CMOS inverter with $V_{\text{DD}} = 5$ V and zero load capacitance. The MOSFETs have $(W/L)_n = 5$, $(W/L)_p = 10$, $KP_n = 50 \mu\text{A}/\text{V}^2$, $KP_p = 25 \mu\text{A}/\text{V}^2$, $V_{\text{ton}} = 1$ V, $V_{\text{top}} = -1$ V, and $\lambda_n = \lambda_p = 0$. Determine the maximum power supply current as the input voltage switches slowly from 0 to V_{DD} .

6.60. Suppose that a CMOS inverter having $V_{\text{DD}} = 5$ V and $C_L = 1$ pF is driven by a 50-MHz pulse train. Determine the average current taken from the power supply and the average power dissipated.

D6.61. CMOS inverter design. Design a CMOS inverter to drive a 2-pF load with $t_{\text{PHL}} = t_{\text{PLH}} = 500$ ps. The supply voltage is $V_{\text{DD}} = 5$ V. Assume that the MOSFETs have $KP_n = 50 \mu\text{A}/\text{V}^2$, $KP_p = 25 \mu\text{A}/\text{V}^2$, $V_{\text{ton}} = 1$ V, $V_{\text{top}} = -1$ V, and $\lambda_n = \lambda_p = 0$. Specify the W/L ratio for each transistor. Use Equations (6.29) and (6.30) to determine the (W/L) ratios needed.

Section 6.7: CMOS NOR and NAND Gates

6.62. Draw the circuit diagram of a three-input CMOS NAND gate.

6.63. Why are NAND gates preferred to NOR gates in CMOS logic?

6.64. Suppose that, to achieve the desired output-current sourcing capability for a two-input CMOS NAND gate, the PMOS transistors must have $(W/L)_p = 4$. The channel lengths of all devices are to be $1\ \mu\text{m}$. Assume that $KP_n = 2KP_p$. Determine W for all of the transistors to achieve symmetrical operation. Also, compute the area consumed by the gate (i.e., the sum of $W \times L$ for all transistors).

6.65. Suppose that, to achieve the desired output-current sinking capability for a two-input CMOS NOR gate, the NMOS transistors must have $(W/L)_n = 2$. The channel lengths of all devices are to be $1\ \mu\text{m}$. Determine W for all of the transistors to achieve symmetrical operation. Also, compute the area consumed by the gate (i.e., the sum of $W \times L$ for all transistors).

6.66. Repeat Example 6.9 for three-input NOR gates.

6.67. Repeat Example 6.10 for two-input NOR gates having $(W/L)_p = (26\ \mu\text{m})/(1\ \mu\text{m})$ and $(W/L)_n = (6.5\ \mu\text{m})/(1\ \mu\text{m})$.

6.68. Use SPICE to determine the propagation delays for the NOR gate of Problem 6.67, taking back-gate and channel-length modulation effects into account for a load capacitance of $2\ \text{pF}$.

6.69. By using alternative series/parallel connections of transistors, various logic functions can be implemented in CMOS. For example, consider the circuit illustrated in Figure P6.69. Find the Boolean expression for F in terms of A , B , and C .

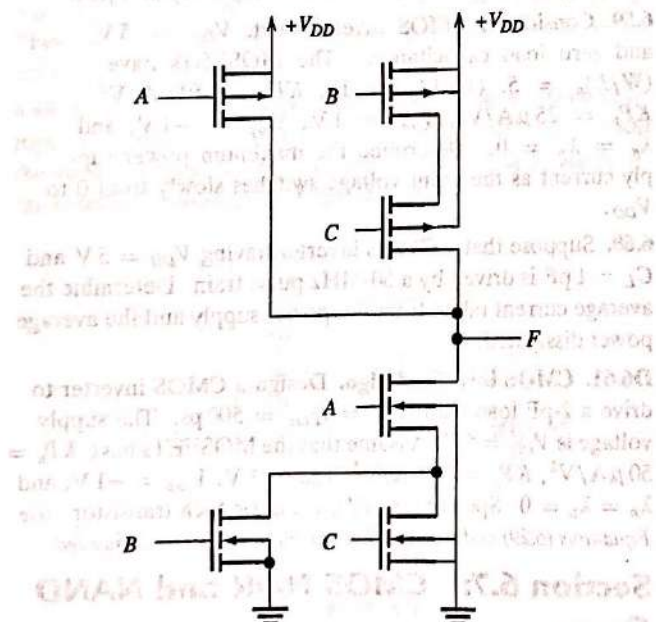


Figure P6.69

6.70. Using the idea illustrated in Problem 6.69, draw a CMOS gate that implements the exclusive-OR logic function $F = A \oplus B = \overline{A}B + A\overline{B}$. Assume that A , $\overline{A}$, B , and $\overline{B}$ are available as inputs.

Section 6.8: Dynamic Logic

6.71. Consider the dynamic logic circuit shown in Figure 6.50. Suppose that A , B , D , and E are low and C is high. When the clock is high, which transistors are on? Which are off? What is the output level? What is the steady-state supply current? Repeat when the clock is low.

6.72. Draw the circuit diagram of a dynamic CMOS gate that realizes the logic function $F = \overline{A + B + CD}$.

6.73. Draw the circuit diagram of a dynamic CMOS gate that realizes the logic function $F = \overline{(AB + CD)E}$.

6.74. Consider the dynamic logic circuit shown in Figure 6.50. The supply voltage is $V_{DD} = 5\ \text{V}$. The MOSFETs have $KP_n = 50\ \mu\text{A}/\text{V}^2$, $KP_p = 25\ \mu\text{A}/\text{V}^2$, $V_{ton} = 1\ \text{V}$, $V_{top} = -1\ \text{V}$, and $\lambda_n = \lambda_p = 0$. Suppose that $C_L = 500\ \text{fF}$. Neglect back-gate effects. Suppose further that, prior to each clock transition, the output voltage is either $+V_{DD}$ or 0. Estimate the minimum (W/L) ratio needed for each transistor so that the output transitions are 50% complete 500 ps after each clock transition, regardless of the logic input levels.

6.75. Repeat Problem 6.74 for a two-input NOR gate.

6.76. Repeat Problem 6.74 for a two-input NAND gate.

6.77. Use SPICE to simulate a two-input dynamic NOR gate like Figure 6.49, for A high and B low. Use the transistor parameters from Table 6.1 and $(W/L) = (20\ \mu\text{m}/1\ \mu\text{m})$ for all transistors. The clock is a 100-MHz square wave and $C_L = 500\ \text{fF}$. Before running the simulation, sketch to approximate scale the output voltage waveform and the current waveforms through each of the transistors.

Section 6.9: The CMOS Transmission Gate and Pass Transistor Logic

6.78. Draw the circuit diagram of an analog switch implemented with MOS transistors.

6.79. Use SPICE to simulate the circuit shown in Figure 6.51, with C high and a resistive load of $10\ \text{k}\Omega$. Use the transistor parameters given in Table 6.1 with $(W/L)_n = 20\ \mu\text{m}/1\ \mu\text{m}$ and $(W/L)_p = 40\ \mu\text{m}/1\ \mu\text{m}$. Sweep v_I from 0 to 5 V and obtain a plot of v_O versus v_I . Repeat for C low.

6.80. Draw a circuit diagram (similar to Figure 6.53a or Figure 6.53b), showing how to implement the logic function $F = AB + C$ with pass transistor logic.

Differential and Multistage IC Amplifiers

In Chapters 4 and 5, we met some basic amplifier circuits, such as the common-emitter amplifier, the emitter follower, the common-source amplifier, and the source follower. In this chapter, we discuss additional circuits that are particularly suitable for designing IC amplifiers.

We start by considering the design rules that are appropriate for integrated circuits compared with those for discrete circuits. The components available—and therefore the most suitable circuits—depend heavily on the methods used for implementation. Then we discuss the biasing techniques used in ICs. Finally, we discuss several types of differential amplifiers.

7

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7.1 DESIGN RULES FOR DISCRETE AND INTEGRATED CIRCUITS

A **discrete circuit** is constructed of components that are manufactured separately. Later, these components are connected together, usually by the conductors of a **printed circuit board**. On the other hand, in an **integrated circuit**, the components and their interconnections are manufactured concurrently by a sequence of processing steps, such as photolithography, doping, and diffusion. The types of components that are available and their practical values depend heavily on the approach taken for implementation. Table 7.1 contrasts the components available for discrete circuits with those for a typical bipolar IC process.

The types of components that are available and their practical values depend heavily on the approach taken for implementation.

Process Complexity

Many different **processes** (combinations of steps) are used in manufacturing ICs. It is desirable to limit the number of steps in a process, because failures occur during each step. Not only does each step incur costs, but the failures reduce the final **yield** (i.e., the percentage of acceptable units at the end of the process).

Table 7.1. Components and Practical Values for Discrete Circuits Compared with Those for ICs.

Discrete Circuits	Integrated Circuits
Resistors	
1 Ω to 20 M Ω	1 Ω to 100 k Ω
Tolerances ± 1 or $\pm 5\%$	Tolerances $\pm 30\%$ with $\pm 2\%$ or better between resistors on a given chip
High-power and low-temperature-coefficient types available	Special types not available
Capacitors	
1 pF to 0.1 F	1 to 100 pF
Tolerances ± 1 to $\pm 20\%$	Tolerances $\pm 25\%$
Low-temperature-coefficient types available	Special types not available
Inductors	
10 nH to 1 H	Almost totally impractical
Tolerances ± 1 to $\pm 20\%$	
BJTs, FETs, and Diodes	
Wide variety of types available	Restricted types available depending on process details
Large unit-to-unit parameter variations	Matched devices available

Depending on the process in use, various limitations exist on the types of components that are available and their characteristics. For example, in a relatively simple bipolar process, we might be restricted to *nnp* transistors, diodes, low-quality *pnp* transistors, resistors, and a few small capacitors. Adding more processing steps increases cost, but can make high-quality *pnp* transistors, JFETs, MOSFETs, and Zener diodes available.

Chip Area

An important consideration in IC design is to keep the surface area of the chip small. Defects are scattered at random on the surface of a semiconductor wafer. Therefore, larger chips have higher probabilities of containing defects that result in circuit failure.

Resistors and capacitors—particularly those of large value—consume large amounts of chip area compared with BJTs, FETs, and diodes. This is the reason that large-value capacitors and resistors are not practical in ICs. For example, it is not unusual for a 30-pF compensation capacitor to consume half of the chip area for an op amp. (The need for the compensation capacitor will be discussed in Chapter 9.)

While each process sets different restrictions, we see that ICs must be designed by using active devices of a few types. A small number of resistors and one or two small-value capacitors can be included if absolutely necessary.

Matching of Device Parameters

One very important advantage that ICs have is that close matching of active device characteristics results because the devices are fabricated concurrently. For example, the β s of BJTs typically match within 10% for transistors on a given chip. On the other hand, for discrete BJTs, β displays unit-to-unit variations of 3 to 1, even for devices having the same type number. The design of IC amplifiers heavily exploits device matching.

Because of the wider variety of devices available, design is often easier in discrete form. As technology advances, ICs replace discrete circuits in given applications. However, the capability of discrete circuits also improves, opening new applications. Furthermore, if a relatively small number of special circuits are to be manufactured, discrete circuits can be more economical than ICs. Thus, applications for discrete circuits are likely to persist, but the bulk of electronic systems are based on ICs.

FETs Versus BJTs

Let us consider some of the advantages and disadvantages of FET circuits compared with BJT circuits. In general, it is possible to design virtually any amplifier (or other electronic function) either with BJTs or FETs. However, some designs that are easily accomplished with one type of device are very difficult with the other.

In discrete circuits, we are not limited in the types of devices that can be employed. However, the majority of the active devices found in discrete electronics (and in pure analog ICs) are BJTs. JFETs are found in the (relatively infrequent) applications for which they offer an advantage compared with BJTs. For example, we might choose a JFET for the input stage of an amplifier if high input impedance is required. In discrete circuits, MOSFETs are quite rare, although they are often used as the input stage of radio receivers to achieve low third-order distortion (which is a rather specialized topic that we will not pursue).

An important consideration in IC design is to keep the surface area of the chip small.

Resistors and capacitors—particularly those of large value—consume large amounts of chip area compared with BJTs, FETs, and diodes.

ICs must be designed using active devices of a few types. A small number of resistors and one or two small-value capacitors can be included if absolutely necessary.

The design of IC amplifiers heavily exploits device matching.

In complex digital ICs, MOSFETs have several important advantages, including the fact that they consume less chip area than BJTs and static power dissipation is very small for CMOS circuits. Thus, by using MOSFETs, it is possible to design complex digital ICs that would be impossible to fabricate using BJTs.

Increasingly, we encounter applications in which it is desirable to mix analog functions with digital functions. For a long time, it was impractical to mix BJTs and MOS devices on the same chip, because a complex process containing numerous steps is necessary to manufacture both types of devices. Until the reliability of each processing step became sufficiently high, mixing BJTs and MOS devices on the same chip led to poor yield. Thus, engineers have expended much effort on designing high-performance analog MOSFET circuits such as op amps.

A relatively recent development is BiCMOS technology, which mixes bipolar devices with complementary MOS. Hence, it has become possible to use a wider variety of active devices in mixed-mode (analog and digital) ICs. We will see that BJTs provide differential-amplifier input stages with low offset voltage and output stages with high current drive capability. The MOS devices provide the capability of handling complex digital functions.

Section summary: The variety of devices available to the IC designer is limited by the complexity of the fabrication process and the need to minimize chip area. Active device characteristics are tailored to a given application by the selection of device dimensions. Resistors and capacitors are avoided if possible. Inductors are not practical in integrated circuits.

In integrated circuits, we cannot use coupling and bypass capacitors, so direct coupling of the stages is employed.

7.2 IC BIASING WITH BJTS

We discussed discrete BJT bias circuits in Section 4.5 and discrete FET bias circuits in Section 5.3. In this section, we consider biasing techniques suitable for ICs. The difference in approaches stems from the relative "cost" of resistors and capacitors. In discrete circuits, resistors are relatively cheap and large capacitors are readily available. In ICs, both of these types of components are "expensive" in terms of chip area. Thus, discrete bias circuits use a network of resistors to bias each transistor, and capacitors are used for coupling and to bypass certain resistors. In integrated circuits, we cannot use coupling and bypass capacitors, so direct coupling of the stages is employed. Also, in ICs, we try to replace resistors with transistors wherever possible.

Factors that Determine the Desired Q -point

The transistors in amplifier circuits must be biased in the active region. (An exception is power amplifiers, for which the devices can be biased near cutoff. We consider power amplifiers in a later chapter.) Many factors are important in determining the best Q -point. Next, we give a brief qualitative discussion of some of these factors.

The desired output signal swing of the amplifier often sets limits on suitable bias-point values. For example, if V_{CEQ} is too small, the BJT can reach saturation—resulting in clipping—before the desired peak signal swing is achieved. If I_{CQ} is too small, cut-off can occur before the desired signal swing is achieved. Therefore, we must make sure that V_{CEQ} and I_{CQ} are large enough so that clipping does not occur.

Device limits must be considered in selecting the Q -point. If V_{CEQ} and I_{CEQ} are too large, the power dissipation limits of the device can be exceeded or collector breakdown can occur.

Lower current levels lead to high-impedance circuits. Hence, a requirement for high input impedance calls for a low value for I_{CQ} for the input stage.

The desired frequency response of the circuit can also be a factor in selecting the nominal Q -point. For example, the collector-junction capacitance becomes smaller with higher values of V_{CEQ} , resulting in wider bandwidth. A measure of the high-frequency performance of BJTs is the transition frequency f_t . (The high-frequency response of amplifiers, device capacitances, and f_t are treated in Chapter 8.) Higher values of f_t imply better operating characteristics at high frequency. The transition frequency of a given BJT reaches a maximum for a particular collector current. For extended high-frequency response, we would select the bias point to achieve the maximum f_t .

Usually, considerations such as these establish a range of values for I_{CQ} and V_{CEQ} that are suitable for a particular circuit. (For an example of these considerations in discrete amplifier design, see Anatomy of a Circuit Design: A Discrete Multistage Amplifier, starting on page 343.)

In biasing, we must make sure that V_{CEQ} and I_{CQ} are large enough so that clipping does not occur due to saturation and cutoff, respectively. Device limits, desired impedance levels, and frequency response are also factors in selecting the Q -point.

The Current Mirror

Next, we show how matched transistors, combined with a few resistors, can act as current sources that are useful in biasing IC amplifiers. Figure 7.1a shows a simple two-transistor current source. Notice that the collector of Q_1 is connected to its base. Thus, $V_{CE1} = V_{BE1} \approx 0.6$ V, and Q_1 is (barely) in the active region. If V_{CE2} is larger than about 0.2 V, Q_2 is also in the active region. We assume that the transistors are matched (i.e., identical). Because the base-to-emitter voltages of the two transistors are equal, we have

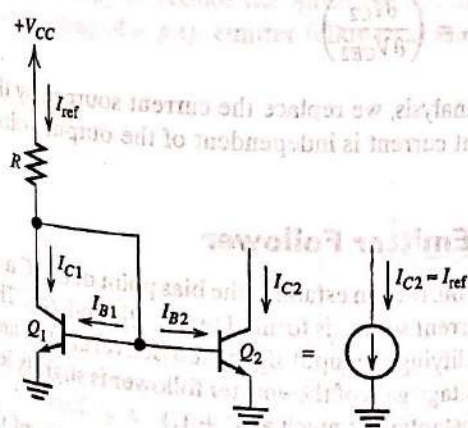
$$I_{B1} = I_{B2} \quad (7.1)$$

and

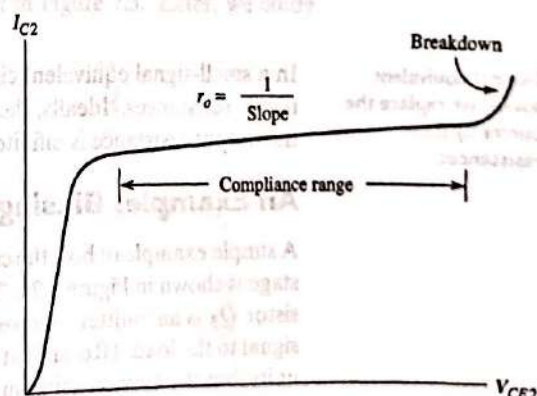
$$I_{C1} = I_{C2} = \beta I_{B1} \quad (7.2)$$

Applying Kirchhoff's current law to Figure 7.1a, we get

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \quad (7.3)$$



(a) Circuit diagram



(b) Output characteristic

Figure 7.1 The current mirror.

Using Equations (7.1), (7.2), and (7.3) to solve for I_{C1} and I_{C2} , we obtain

$$I_{C1} = I_{C2} = \frac{I_{\text{ref}}}{1 + 2/\beta} \quad (7.4)$$

Usually, β is much larger than unity, and we have

$$I_{C1} = I_{C2} \cong I_{\text{ref}} \quad (7.5)$$

Because $I_{C1} = I_{C2}$, this circuit is called a **current mirror**. The current I_{ref} is called the **reference current** and is given by

$$I_{\text{ref}} = \frac{V_{CC} - V_{BE}}{R} \quad (7.6)$$

IC amplifiers are invariably direct coupled. Current sources composed of one or two resistors and active devices are used for biasing.

As usual, $V_{BE} \cong 0.6 \text{ V}$ for silicon devices at room temperature and for currents on the order of 1 mA.

Compliance Range and Dynamic Output Resistance

The output characteristic (current versus voltage) of the current mirror is displayed in Figure 7.1b. To a first approximation, the base current of Q_2 is independent of the output voltage V_{CE2} . Therefore, the output characteristic is almost identical to one of the collector characteristic curves for Q_2 .

An important specification of a current source is the range of output voltage for which the output current is approximately constant. This is called the **compliance range** and is illustrated in Figure 7.1b.

Another important specification of a current source is its **dynamic output resistance**, which is the ratio of the incremental output voltage divided by the incremental output current. Thus, the dynamic output resistance is the inverse of the slope of the output characteristic, as shown in Figure 7.1b. In equation form, the output resistance is given by

$$r_o = \left(\frac{\partial I_{C2}}{\partial V_{CE2}} \right)^{-1} \quad (7.7)$$

The most important parameters of a current source are its dynamic resistance and compliance range.

In a small-signal equivalent circuit analysis, we replace the current sources by their dynamic resistances.

In a small-signal equivalent circuit analysis, we replace the current sources by their dynamic resistances. Ideally, the output current is independent of the output voltage and the output resistance is infinite.

An Example: Biasing an Emitter Follower

A simple example of how the current mirror can establish the bias point of an IC amplifier stage is shown in Figure 7.2a. The current source is formed by R , Q_1 , and Q_2 . The transistor Q_3 is an emitter follower, amplifying the input signal and delivering the amplified signal to the load. (Recall that the voltage gain of the emitter follower is slightly less than unity, but the current gain can be substantial—as much as $\beta + 1$.)

Often, in drawing the circuit diagram of an IC, we simplify the diagram of the bias circuits as illustrated in Figure 7.2b.

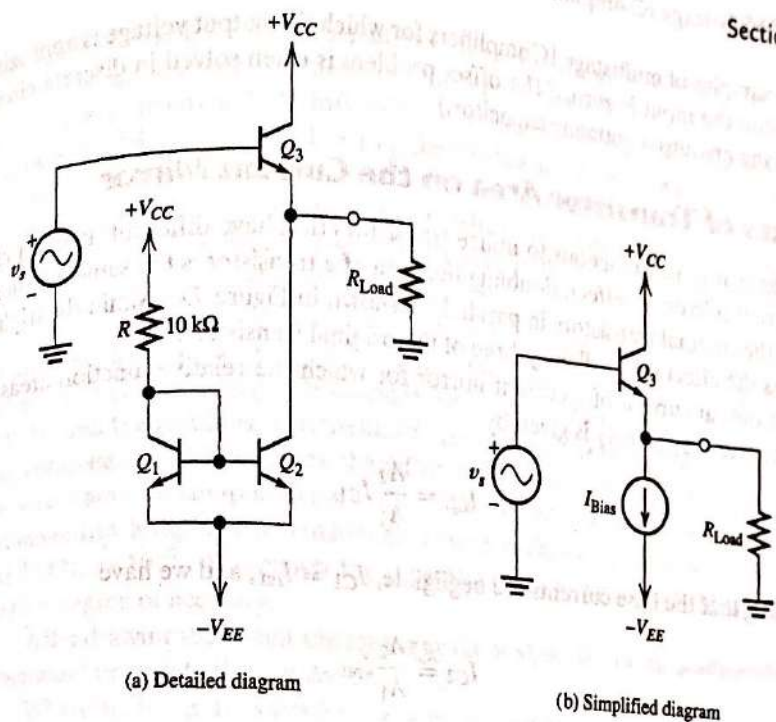


Figure 7.2 Emitter follower with bias current source.

Notice in Figure 7.2 that the amplifier is directly connected to the source and to the load. (That is, no coupling capacitors are used.) The dc base current of Q_3 flows through the signal source. The input circuits of IC amplifiers are almost always direct coupled. (This is the reason for the input bias current of IC op amps.)

Another aspect of the amplifier shown in Figure 7.2 is that the output voltage is approximately -0.7 V for an input voltage of zero. This is due to the V_{BE} drop of Q_3 . We say that the circuit displays a dc offset. Often, this is not a very desirable characteristic for an amplifier to have.

A simple way to reduce the offset for this follower would be to cascade a second stage consisting of a *pnp* emitter follower as illustrated in Figure 7.3. Later, we study

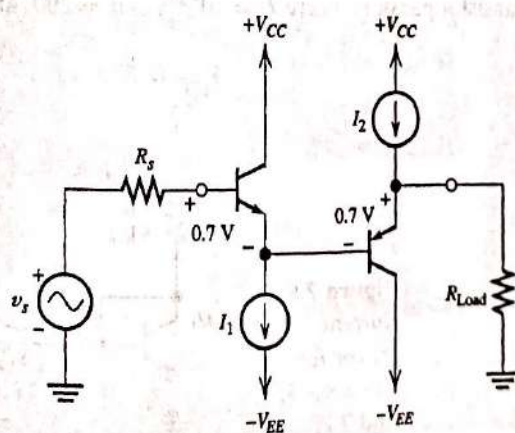


Figure 7.3
The offset voltage can be reduced by cascading a complementary (*pnp*) emitter follower.

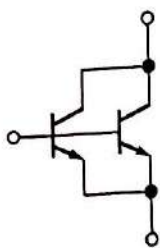


Figure 7.4 Doubling the junction area of a BJT is equivalent to connecting two of the original BJTs in parallel.

other examples of multistage IC amplifiers for which the output voltage is approximately zero when the input is zero. (The offset problem is often solved in discrete circuits by employing an output coupling capacitor.)

Effects of Transistor Area on the Current Mirror

Sometimes it is advantageous to utilize transistors that have different junction areas in the current mirror. In effect, doubling the area of a transistor is the same as connecting two of the original transistors in parallel, as shown in Figure 7.4. Similarly, tripling the area has the effect of paralleling three of the original transistors.

The output current of a current mirror for which the relative junction areas of the transistors are A_1 and A_2 is given by

$$I_{C2} = \frac{A_2}{A_1} I_{C1} \quad (7.8)$$

Assuming that the base currents are negligible, $I_{C1} = I_{ref}$, and we have

$$I_{C2} \cong \frac{A_2}{A_1} I_{ref} \quad (7.9)$$

Sometimes, we need a small-valued current source. A large value of R could be used; however, large resistances consume excessive chip area. An alternative is to employ a smaller transistor for Q_2 than for Q_1 .

Nevertheless, when extremely small currents are required, even this approach makes poor use of chip area, because a given process has a fixed minimum feature size. Thus, to achieve a large ratio, a large transistor is needed.

Example 7.1 Current-Source Output Characteristic Using SPICE

Use PSpice to plot I_{C2} against V_O for the circuit of Figure 7.5. Also, obtain a plot of the dynamic resistance against V_O . Assume that $V_{CC} = 15\text{ V}$, $R = 5\text{ k}\Omega$, and the relative areas for Q_1 and Q_2 are $A_1 = 2$ and $A_2 = 1$, respectively. The transistor parameters are $I_s = 10^{-15}\text{ A}$, $\beta = 200$, and $V_A = 100\text{ V}$.

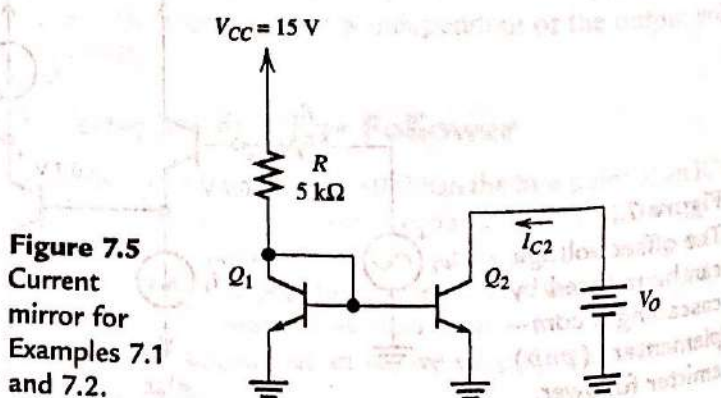


Figure 7.5 Current mirror for Examples 7.1 and 7.2.

SOLUTION First we use Schematics to draw the circuit. Then we use the **analysis/setup/dc sweep** command to bring up the window in which we set up a sweep of V_{CE2} from 0 to 15 V, in 0.01-V increments. We then use the **edit/model/edit instance model** command to bring up the window in which we specify the model name and model parameters for the transistors. Next, we double click on each transistor icon to bring up the window in which we specify the relative area for each transistor. The circuit schematic is stored in the file named Fig7.5. If you open this file, you can examine these windows.

Because we want a plot of the dynamic resistance of the source, which is approximated in Probe by $\Delta V_O / \Delta I_{C2}$, the currents and voltages must be computed very accurately. For example, we have specified increments for ΔV_O of 0.01 V, and the resulting increments of ΔI_{C2} are very small. Unless the currents are computed to high accuracy, the difference between two successive values will be due mainly to computational error. Thus, we use the **analysis/setup/options** command to bring up the window illustrated in Figure 7.6, in which we enter $RELTOL = 10^{-7}$. This causes the currents and voltages to be computed with a higher degree of accuracy.

After drawing the circuit and setting up the analysis, we use the **analysis/simulate** command to initiate the simulation.

When the program is finished running, we use Probe to generate the plot of I_{C2} versus V_{CE2} shown in Figure 7.7. Notice that as long as V_{CE2} is greater than a few tenths of a volt, the current is nearly constant, as expected.

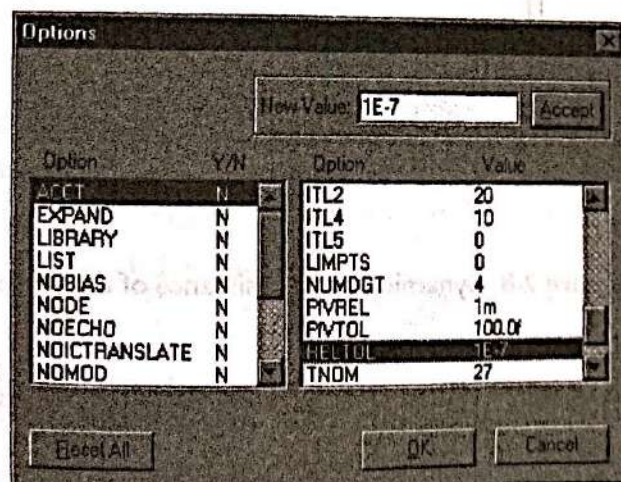
The small-signal (dynamic) output resistance of the source is

$$r_o = \left(\frac{\partial I_{C2}}{\partial V_{CE2}} \right)^{-1}$$

A plot of r_o can be obtained by requesting Probe to plot $1/D(IC(Q2))$. The result is shown in Figure 7.8. In the intended range of operation (i.e., $V_{CE2} > 0.5$ V), the output resistance of the current source is approximately 70 k Ω .

□

Figure 7.6
The **analysis/setup/options** command brings up this window.



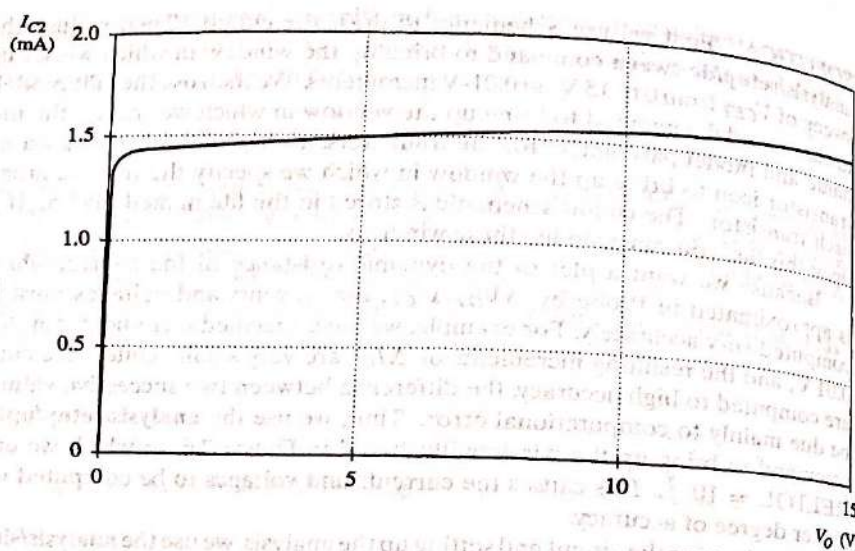


Figure 7.7 Output characteristic for the current mirror of Figure 7.5.

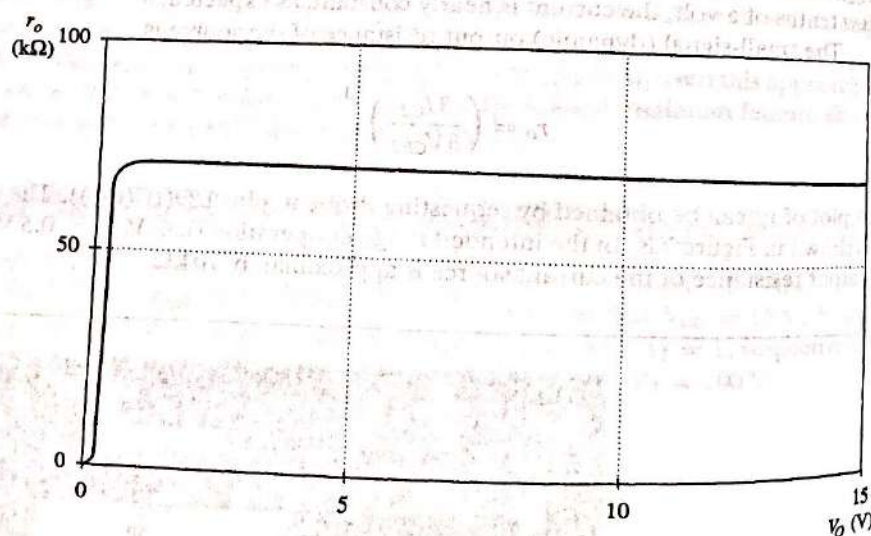


Figure 7.8 Dynamic output resistance of the current mirror of Figure 7.5.

Example 7.2 Manual Analysis of a Current Source

Use manual analysis to check the results found in Example 7.1.

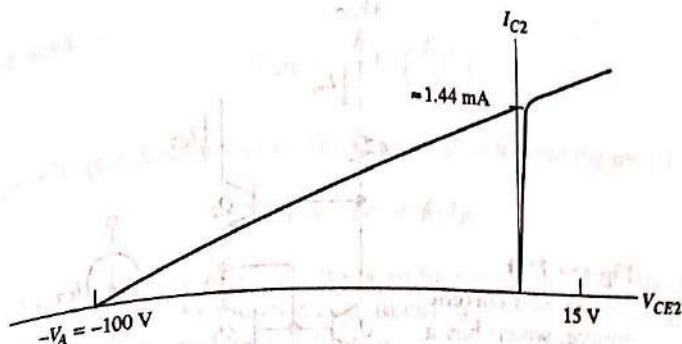


Figure 7.9 Collector characteristic of Q_2 , illustrating the Early voltage.

SOLUTION Refer to the circuit diagram illustrated in Figure 7.5. First, we use Equation (7.6) to compute

$$I_{\text{ref}} = \frac{V_{CC} - V_{BE}}{R} \approx \frac{15 - 0.6}{5 \text{ k}\Omega} = 2.88 \text{ mA}$$

Then we use Equation (7.9) to find

$$I_{C2} \approx \frac{A_2}{A_1} I_{\text{ref}} = \frac{1}{2} \times 2.88 \text{ mA} = 1.44 \text{ mA}$$

which agrees very well with the SPICE result.

The forward Early voltage of the transistor is $V_A = V_{AF} = 100 \text{ V}$. The plot of I_{C2} versus V_{CE2} for the current mirror is approximately the same as one of the collector characteristics of Q_2 . (For the collector characteristics, I_{B2} is constant, which is only approximately true in the current mirror.) A plot of the collector characteristic showing the Early voltage appears in Figure 7.9. From this plot, we can see that

$$r_o = \left(\frac{\partial I_{C2}}{\partial V_{CE2}} \right)^{-1} \approx \left(\frac{I_{C2}}{V_A} \right)^{-1} \approx \left(\frac{1.44 \text{ mA}}{100 \text{ V}} \right)^{-1} = 69.4 \text{ k}\Omega$$

which agrees closely with the SPICE result. $\square$

The Wilson Current Source

An improved circuit, called the **Wilson current source**, with higher output impedance than the current mirror is illustrated in Figure 7.10. For this circuit, we have

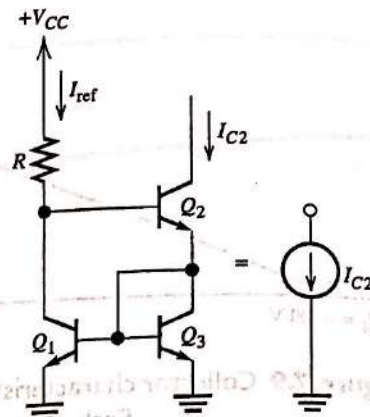
$$I_{\text{ref}} = \frac{V_{CC} - V_{BE2} - V_{BE3}}{R} \quad (7.10)$$

and

$$I_{C2} \approx \frac{A_3}{A_1} I_{\text{ref}} \quad (7.11)$$

in which A_1 and A_3 are the relative junction areas of Q_1 and Q_3 , respectively.

Figure 7.10
The Wilson current source, which has a high output resistance.



Later, we will see that high-impedance current sources such as the Wilson circuit are useful in the design of differential amplifiers that have good common-mode rejection. (Common-mode rejection is defined in Section 1.11.)

The Widlar Current Source

As we have seen, the basic current mirror is not economical in terms of chip area for small-value current sources. The **Widlar current source** shown in Figure 7.11 is much better in this respect.

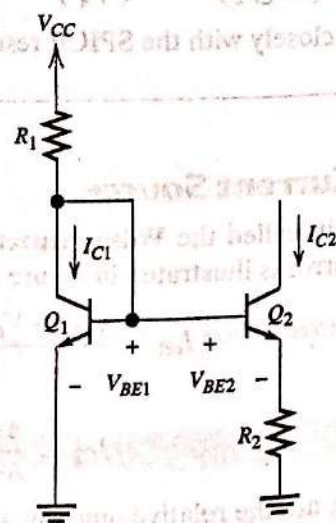
In analyzing the Widlar circuit, we assume that the transistors are identical and that V_{CE2} is high enough to allow Q_2 to operate in the active region. Then the collector current of Q_2 is given by

$$I_{C2} = I_s \exp\left(\frac{V_{BE2}}{V_T}\right) \quad (7.12)$$

Solving for V_{BE2} , we get

$$V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_s}\right) \quad (7.13)$$

Figure 7.11
The Widlar current source, which is useful for small currents.



Similarly, we have

$$V_{BE1} = V_T \ln \left(\frac{I_{C1}}{I_s} \right) \quad (7.14)$$

Writing a voltage equation around the base-emitter loop of Figure 7.11, we obtain

$$V_{BE1} = V_{BE2} + R_2 I_{E2} \quad (7.15)$$

We assume that β is large compared to unity, so we can replace I_{E2} with I_{C2} . We make this change in Equation (7.15), then use Equations (7.13) and (7.14) to substitute for V_{BE1} and V_{BE2} , and finally solve for R_2 , resulting in

$$R_2 \cong \frac{V_T}{I_{C2}} \ln \left(\frac{I_{C1}}{I_{C2}} \right) \quad (7.16)$$

Neglecting the base currents, we have

$$I_{C1} \cong I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1} \quad (7.17)$$

Example 7.3 Widlar-Current-Source Design

Design a $10\text{-}\mu\text{A}$ Widlar current source, given that $V_{CC} = 15\text{ V}$. Assume identical transistors. Also, design a $10\text{-}\mu\text{A}$ current mirror, and compare the total resistance required in the two circuits.

SOLUTION First, we design the Widlar source. We arbitrarily select a reference current of 1 mA . Then Equation (7.17) yields

$$R_1 = \frac{V_{CC} - V_{BE1}}{I_{ref}} \cong \frac{15\text{ V} - 0.6\text{ V}}{1\text{ mA}} = 14.4\text{ k}\Omega$$

If we selected a larger value of I_{ref} , R_1 would be smaller in value and (possibly) take less chip area. However, the demand on the power supply and the chip dissipation would be larger. Thus, we must use good judgment to make the trade-off. (Of course, what constitutes good judgment depends on the application.) The value we have selected would be a good choice in many situations.

Next, we use Equation (7.16) to compute the value of R_2 :

$$R_2 \cong \frac{V_T}{I_{C2}} \ln \left(\frac{I_{C1}}{I_{C2}} \right) = \left(\frac{0.026}{10\text{ }\mu\text{A}} \right) \ln \left(\frac{1\text{ mA}}{10\text{ }\mu\text{A}} \right) \cong 12\text{ k}\Omega$$

Now we design the current mirror. (The circuit diagram is shown in Figure 7.1.) The resistance can be found from Equation (7.6) as

$$R = \frac{V_{CC} - V_{BE}}{I_{ref}} = \frac{15\text{ V} - 0.5\text{ V}}{10\text{ }\mu\text{A}} = 1.45\text{ M}\Omega$$

The simplest BJT current source is the current mirror. The Wilson current source is used when a higher dynamic resistance is needed, and the Widlar source is best when the application calls for very small currents.

(Notice that we have used a smaller estimate for V_{BE} in this case, because the current is $10\ \mu\text{A}$, whereas for the Widlar source, we used $V_{BE1} = 0.6$, because the current in Q_1 was $1\ \text{mA}$.)

Comparing the two approaches, we see that the Widlar circuit requires a total resistance of $R_1 + R_2 = 26.4\ \text{k}\Omega$, whereas the current mirror needs $1.45\ \text{M}\Omega$. Consequently, the Widlar circuit consumes a much smaller chip area.

Combined Current Sources

Often, in an IC amplifier, several current sources use the same reference current. An example is given in Figure 7.12. The current through R_1 is the reference current for all four current sources. Transistors Q_1 and Q_2 form a current mirror. Transistors Q_1 and Q_3 form a Widlar source. The *pnp* transistor circuits are similar—differing only in current direction and voltage polarity.

Sometimes engineers refer to *nnp* transistors, which remove current from the circuit to which they are connected, as **current sinks**. By contrast, *pnp* transistors deliver current and are called **current sources**. Notice that current flows into a *sink* and out of a *source*. At other times, the term *current source* is used to refer to both sources and sinks.

EXERCISE

7.1 Use SPICE to verify the design of the $10\text{-}\mu\text{A}$ current mirror and the Widlar source of Example 7.3. Determine the compliance ranges of the circuits, and obtain plots of their incremental output resistances versus V_O , for V_O ranging from 0 to 15 V. The transistor parameters are $I_s = I_{S1} = 10^{-15}\ \text{A}$, $\beta = \beta_F = 200$, and $V_A = V_{AF} = 100\ \text{V}$.

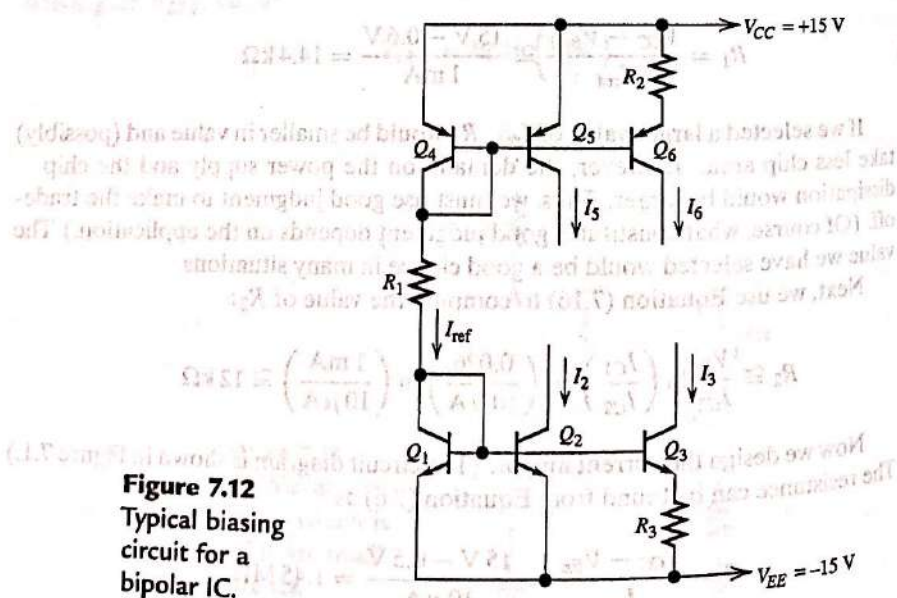


Figure 7.12
Typical biasing
circuit for a
bipolar IC.

Answer The schematic is stored in the file named Exer7.1. The simulation shows that both circuits yield output currents of approximately $10\ \mu\text{A}$. For the Widlar source, the compliance range extends from 0.5 to 15 V, and the output resistance is approximately $60\ \text{M}\Omega$ in the compliance range. For the current mirror, the compliance range extends from 0.35 to 15 V, and the output resistance is approximately $10\ \text{M}\Omega$ in the compliance range.

EXERCISE

7.2 Assuming identical *npn* transistors having equal areas, design a 1-mA current mirror. The supply voltage is $V_{CC} = 15\ \text{V}$. Also, design a 1-mA Wilson sink. Use SPICE to plot the current versus voltage characteristics of both circuits. Also, obtain plots of the output resistance versus voltage. The transistor parameters are $I_s = I_{S0} = 10^{-15}\ \text{A}$, $\beta = \text{BF} = 200$, and $V_A = \text{VAF} = 100\ \text{V}$.

Answer The circuits are illustrated in Figure 7.13. The schematic is stored in file Fig7.13. The simulation results show that the mirror has an output resistance of approximately $100\ \text{k}\Omega$ in the compliance range, whereas the Wilson sink has an output resistance ranging from $8\ \text{M}\Omega$ to $10\ \text{M}\Omega$. [Hint: To obtain a plot of the output resistance of the Wilson source, use the **analysis/setup/options** command, and change the parameter **RELTOL** to 10^{-9} ; then, after the simulation, request a plot of $1/D(\text{IC}(Q4))$.]

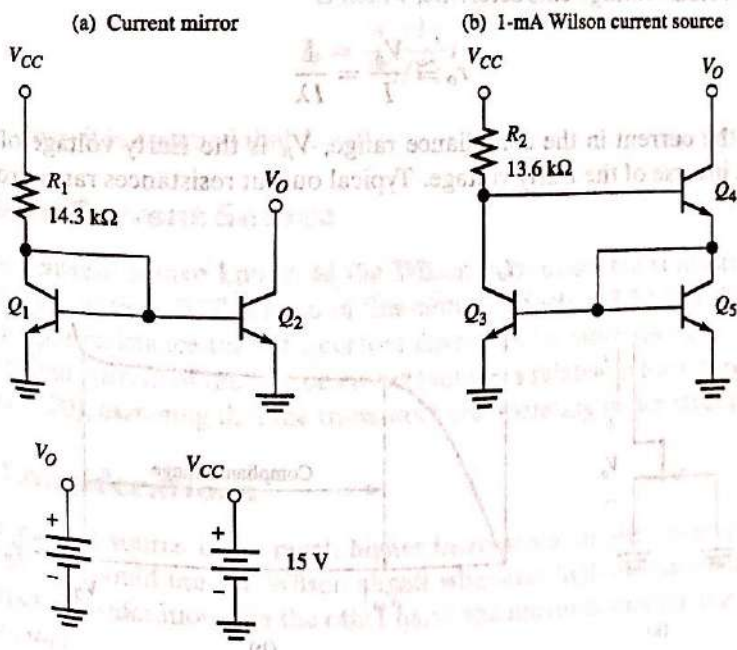


Figure 7.13 Answer for Exercise 7.2.

EXERCISE

7.3 Consider the circuit shown in Figure 7.12. The relative transistor areas are $A_1 = A_2 = A_3 = A_4 = A_6 = 1$. Assume that β is very high for all transistors, so the base currents can be neglected. We wish to design the circuit so that $I_2 = 1 \text{ mA}$, $I_3 = 50 \mu\text{A}$, $I_5 = 3 \text{ mA}$, and $I_6 = 100 \mu\text{A}$. Find the resistor values and the relative area of Q_5 . Assume that $v_{BE} \cong 0.7 \text{ V}$ for all transistors.

Answer $R_1 = 28.6 \text{ k}\Omega$, $R_2 = 599 \Omega$, $R_3 = 1.56 \text{ k}\Omega$, and $A_5 = 3$.

7.3 IC BIASING WITH FETS

The BJT current sources that we discussed in the previous section have counterparts constructed with FETs. The simplest FET current source consists of a depletion-mode MOSFET or a JFET with its gate connected to its source as shown in Figure 7.14. The current-versus-voltage characteristic of this current source is the drain characteristic of the FET. (The circuit is not suitable for enhancement MOSFETs, because the current is zero for $v_{GS} = 0$.)

As in the case of BJT current sources, the most important specifications for FET current sources are the compliance range and the small-signal output impedance. For the circuit of Figure 7.14, the compliance range extends from $V_o = |V_{to}|$ to the breakdown voltage of the device.

The output resistance of the simple FET current source is the inverse of the slope of the current-versus-voltage characteristic, which is

$$r_o \cong \frac{V_A}{I} = \frac{1}{I\lambda} \quad (7.18)$$

where I is the current in the compliance range, V_A is the Early voltage of the device, and λ is the inverse of the Early voltage. Typical output resistances range from $10 \text{ k}\Omega$ to $1 \text{ M}\Omega$.

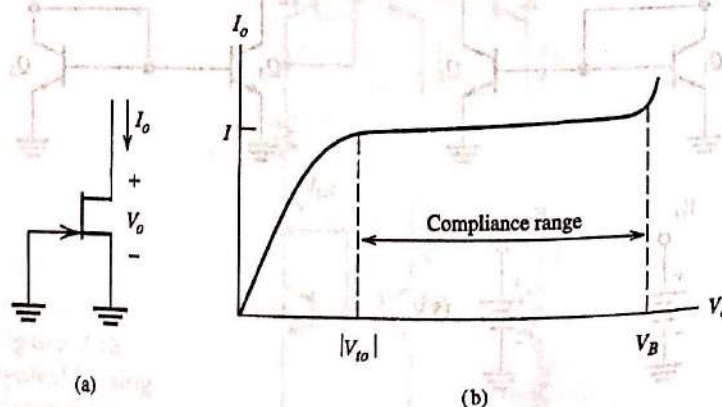
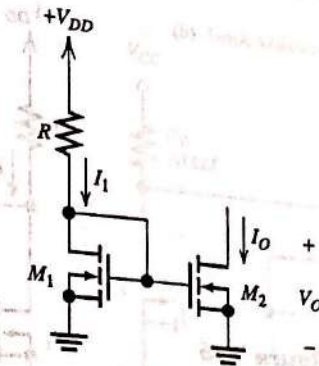


Figure 7.14 JFET as a current source.

Figure 7.15
NMOS current mirror.



The FET Current Mirror

A current-mirror circuit using enhancement-mode MOSFETs is shown in Figure 7.15. This circuit is similar to the BJT current mirror considered in Section 7.2. Because the drain-to-gate voltage of M_1 is zero, it is operating in saturation (provided that V_{DD} is greater than V_{to}). Assuming that the MOSFETs are identical and that the output voltage V_o is large enough so that M_2 is in saturation, the currents are nearly equal:

$$I_o = I_1 \quad (7.19)$$

By using devices with different width-to-length ratios, circuits having I_o equal to a predetermined constant times I_1 can be designed. In terms of the width-to-length ratios of the devices, the currents are approximately related by

$$I_o = \frac{W_2/L_2}{W_1/L_1} I_1 \quad (7.20)$$

In this expression, it is assumed that $\lambda = 0$.

The Wilson Current Source

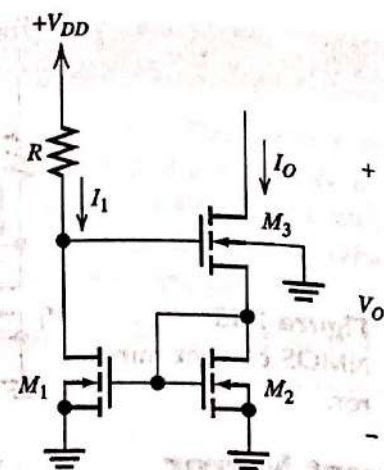
An improved current source known as the Wilson current source is illustrated in Figure 7.16. (We discussed a BJT version of this circuit in Section 7.2.) The Wilson circuit has higher output resistance than the current mirror, but a more restricted compliance range. The output current of the Wilson current source is related to the reference current by Equation (7.20), assuming that the transistors are operating in the saturation region.

Design Considerations

The Wilson current source has a much higher incremental output resistance than the mirror. Thus, we should use the Wilson circuit whenever high output resistance is the most important consideration. On the other hand, the mirror is simpler and has a larger compliance range. We can design for a given current value by our selection of the resistor values and the width-to-length ratios of the transistors.

The Wilson current source has a much higher incremental output resistance than the mirror. Thus, we should use the Wilson circuit whenever high output resistance is the most important consideration. On the other hand, the mirror is simpler and has a larger compliance range.

Figure 7.16
NMOS Wilson current source.



Referring to the mirror circuit shown in Figure 7.15, we see that the voltage at the gate of M_1 must be higher than the threshold voltage of the transistors. (Otherwise the transistors do not conduct.) Hence, we can estimate the reference current as

$$I_1 \cong \frac{V_{DD} - V_{to}}{R} \quad (7.21)$$

Then the output current can be found by using Equation (7.20).

In the case of the Wilson source shown in Figure 7.16, the voltage at the gate of M_3 must be at least $2 \times V_{to}$. (Otherwise either M_3 or M_2 is in cutoff.) Therefore, we can estimate the reference current as

$$I_1 \cong \frac{V_{DD} - 2V_{to}}{R} \quad (7.22)$$

For both circuits, the compliance range increases as the widths of the transistors are increased.

EXERCISE

7.4 Use SPICE to plot output currents versus V_O for the current mirror and for the Wilson current sink shown in Figure 7.17. The model parameters for the NMOS transistors are $K_P = 50 \mu\text{A}/\text{V}^2$, $\lambda = \text{LAMBDA} = 0.01$, and $V_{to} = \text{VTO} = 1\text{V}$. All of the transistors have a channel length of $10 \mu\text{m}$ and a width of $100 \mu\text{m}$. Also obtain plots of the small-signal output resistance versus V_O .

Answer The schematic is stored in the file named Fig7_17. The plots are displayed in Figures 7.18 and 7.19.

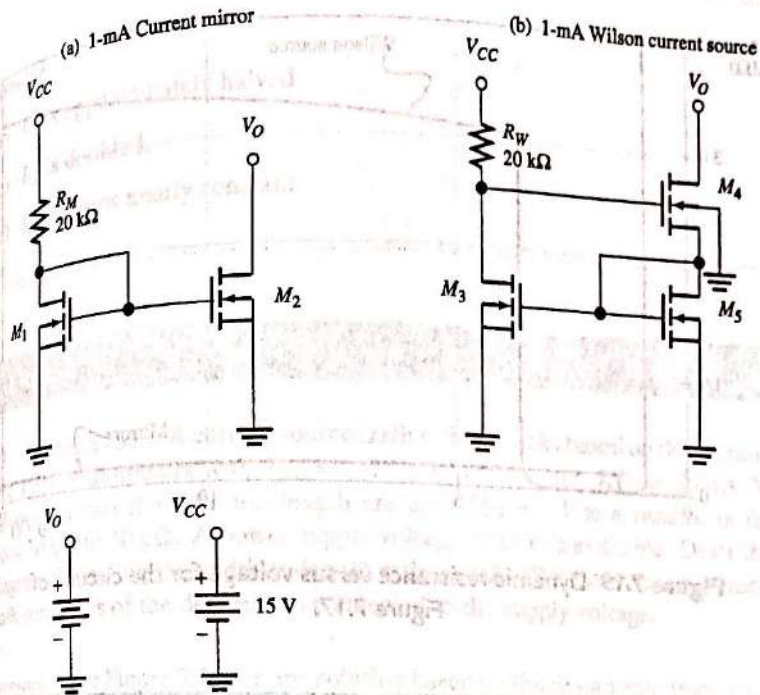


Figure 7.17 Circuits for Exercise 7.4.

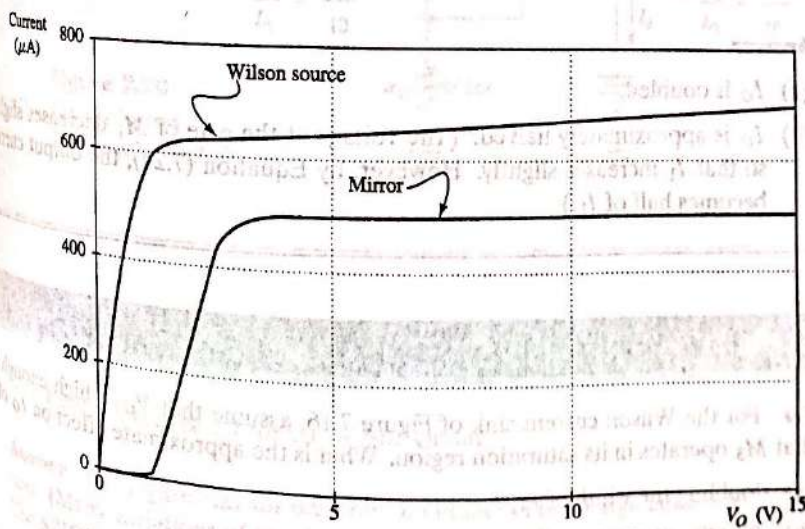


Figure 7.18 Current versus voltage for the circuits of Figure 7.17.

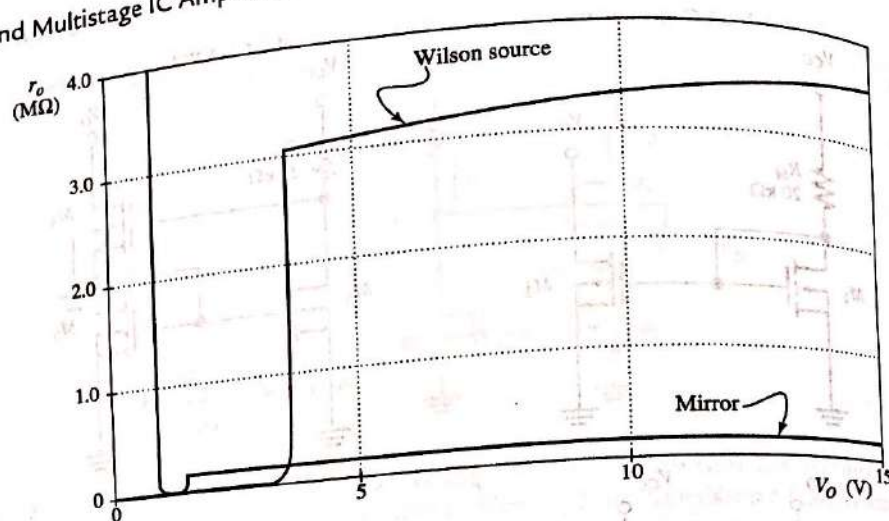


Figure 7.19 Dynamic resistance versus voltage for the circuits of Figure 7.17.

EXERCISE

7.5 For the current mirror of Figure 7.15, assume that V_O is large enough so that M_2 operates in its saturation region. Approximately what is the effect on I_O of

- (a) doubling the width of M_2 ?
- (b) doubling the width of M_1 ?

Answer

- (a) I_O is doubled.
- (b) I_O is approximately halved. (The voltage at the gate of M_1 decreases slightly so that I_1 increases slightly. However, by Equation (7.20), the output current becomes half of I_1 .)

EXERCISE

7.6 For the Wilson current sink of Figure 7.16, assume that V_O is high enough so that M_3 operates in its saturation region. What is the approximate effect on I_O of

- (a) doubling the width of M_1 ?
- (b) doubling the width of M_2 ?
- (c) doubling the width of M_3 ?

Answer

- (a) I_O is approximately halved.
- (b) I_O is doubled.
- (c) I_O remains nearly constant.

EXERCISE

7.7 Design a $200\text{-}\mu\text{A}$ current source (rather than a sink) based on the current mirror. Use PMOS transistors with $V_{to} = -1\text{ V}$, $\lambda = 0.01$, and $K_P = 25\text{ }\mu\text{A/V}^2$. The minimum channel width and length are each $10\text{ }\mu\text{m}$. Use a resistor in the range from $10\text{ k}\Omega$ to $50\text{ k}\Omega$. A power-supply voltage of 15 V is available. Draw the circuit diagram, including the width-to-length ratio of each PMOS device. Assume that the bulk terminals of the devices are connected to the supply voltage.

Answer See Figure 7.20 for one solution based on the design equations given in this section. Many other combinations of device dimensions and resistance values will work. You can use SPICE to check your solution and to refine the design.

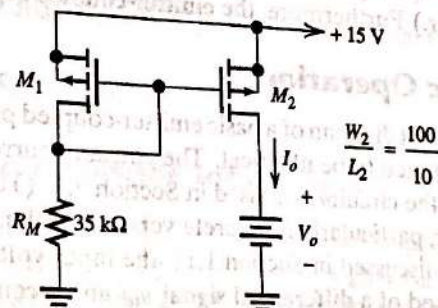


Figure 7.20
One solution
for Exercise 7.7.

EXERCISE

7.8 Repeat Exercise 7.7 for the Wilson circuit.

Answer See Figure 7.21 for one solution based on the design equations in this section. (Many variations of resistance and transistor dimensions are equally correct.) Use SPICE to check your answer and to refine your design.

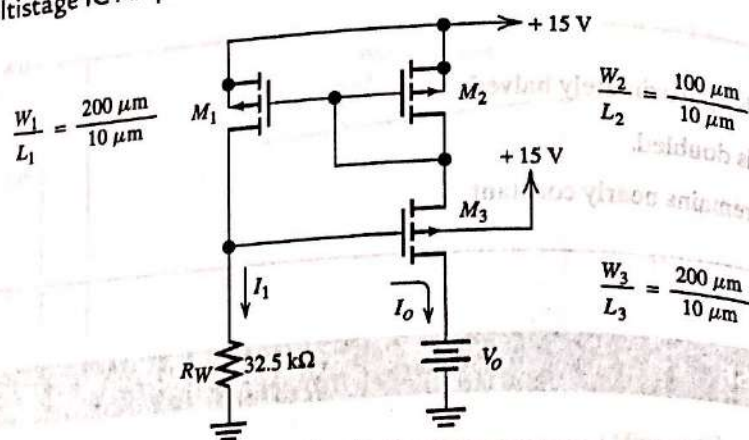


Figure 7.21 One solution for Exercise 7.8.

7.4 LARGE-SIGNAL ANALYSIS OF THE EMITTER-COUPLED DIFFERENTIAL PAIR

In Section 1.11, we introduced differential amplifiers without considering their internal operation. In this section, we discuss a very important circuit called the **BJT differential amplifier**, also known as the **emitter-coupled pair**. This circuit is common in bipolar analog ICs. For example, it forms the input stage of many op amps and comparators. (Some op amps use FETs in a similar circuit configuration that we consider in later in the chapter.) Furthermore, the **emitter-coupled logic (ECL)** family is based on this circuit.

Basic Operation

The circuit diagram of a basic emitter-coupled pair is shown in Figure 7.22. The transistors are assumed to be identical. The constant current source I_{EE} is usually implemented as one of the circuits discussed in Section 7.2. (The current source may be replaced with a resistor, particularly in discrete versions of the circuit.)

As discussed in Section 1.11, the input voltages v_{i1} and v_{i2} can be considered to be composed of a **differential signal** v_{id} and a **common-mode signal** v_{icm} . These are given by

$$v_{id} = v_{i1} - v_{i2}$$

and

$$v_{icm} = \frac{1}{2}(v_{i1} + v_{i2})$$

Ideally, a differential amplifier produces an amplified version of v_{id} and ignores v_{icm} .

Referring to Figure 7.22, we can see that the output voltages are given by

$$v_{o1} = V_{CC} - R_C i_{C1} \quad (7.23)$$

and

$$v_{o2} = V_{CC} - R_C i_{C2} \quad (7.24)$$

Ideally, a differential amplifier produces an amplified version of v_{id} and ignores v_{icm} .

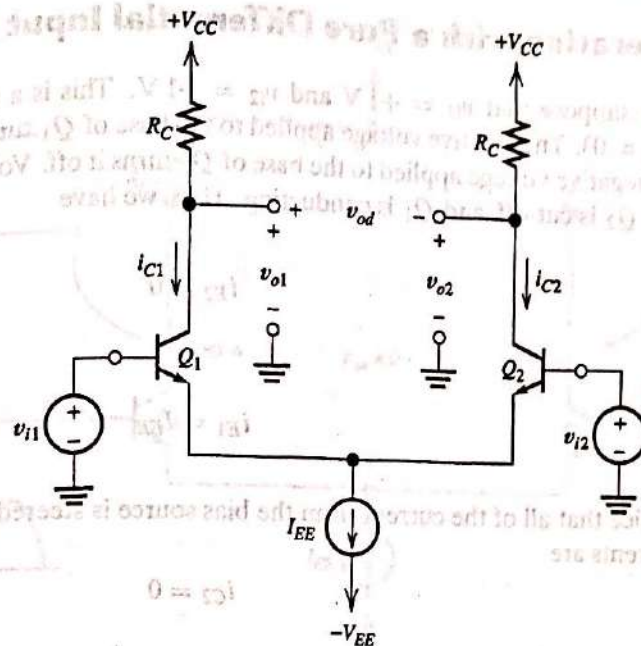


Figure 7.22
Basic BJT differential amplifier.

The differential output voltage is

$$v_{od} = v_{o1} - v_{o2} \quad (7.25)$$

Using Equations (7.23) and (7.24) to substitute into Equation (7.25), we have

$$v_{od} = R_C(i_{C2} - i_{C1}) \quad (7.26)$$

Operation with a Pure Common-Mode Input Signal

Let us consider the basic operation of the circuit of Figure 7.22. To start, suppose that the input voltages v_{i1} and v_{i2} are equal. Then the differential input signal v_{id} is zero, and we have a pure common-mode input signal. Because of the symmetry of the circuit, the bias current I_{EE} splits equally between Q_1 and Q_2 . Thus, we have

$$i_{E1} = i_{E2} = I_{EE}/2 \quad (7.27)$$

We assume that both transistors are operating in the active region, so that the collector current is α times the emitter current for each transistor. Therefore,

$$i_{C1} = i_{C2} = \alpha I_{EE}/2 \quad (7.28)$$

Notice that these currents are independent of the input voltages. Consequently, the output voltages are unaffected by a pure common-mode input signal. The circuit does not respond to the common-mode component of the input.

Operation with a Pure Differential Input Signal

Now suppose that $v_{i1} = +1$ V and $v_{i2} = -1$ V. This is a pure differential input (i.e., $v_{icm} = 0$). The positive voltage applied to the base of Q_1 turns it on even more, whereas the negative voltage applied to the base of Q_2 turns it off. Voltages of ± 1 V are sufficient that Q_2 is cut-off, and Q_1 is conducting. Thus, we have

$$i_{E2} = 0 \quad (7.29)$$

and

$$i_{E1} = I_{EE} \quad (7.30)$$

Notice that all of the current from the bias source is steered through Q_1 . The collector currents are

$$i_{C2} = 0 \quad (7.31)$$

and

$$i_{C1} = \alpha I_{EE} \quad (7.32)$$

The differential output voltage can be found by using Equations (7.31) and (7.32) to substitute for the currents in Equation (7.26):

$$v_{od} = -R_C \alpha I_{EE} \quad (7.33)$$

Now consider the opposite condition, for which $v_{i1} = -1$ and $v_{i2} = 1$ V. In this case, Q_1 is cutoff, and Q_2 is conducting. The bias current I_{EE} is then steered through Q_2 . Thus, we have

$$i_{C1} = 0$$

$$i_{C2} = \alpha I_{EE}$$

$$v_{od} = +R_C \alpha I_{EE}$$

Notice that the polarity of v_{od} has reversed.

To summarize, the circuit rejects the common-mode input component and responds to the differential input. When a pure common-mode input is applied, the current I_{EE} continues to split equally, and the output voltages do not change. On the other hand, a differential input signal steers I_{EE} toward one side or the other, resulting in a differential output voltage.

In amplifier applications, we apply a small signal, and both transistors remain in linear operation—only a fraction of the current is deflected. Figure 7.23 shows waveforms for a common-mode input signal and for a differential input signal.

When a pure common-mode input is applied, the current I_{EE} continues to split equally, and the output voltages do not change. On the other hand, a differential input signal steers I_{EE} toward one side or the other, resulting in a differential output voltage.

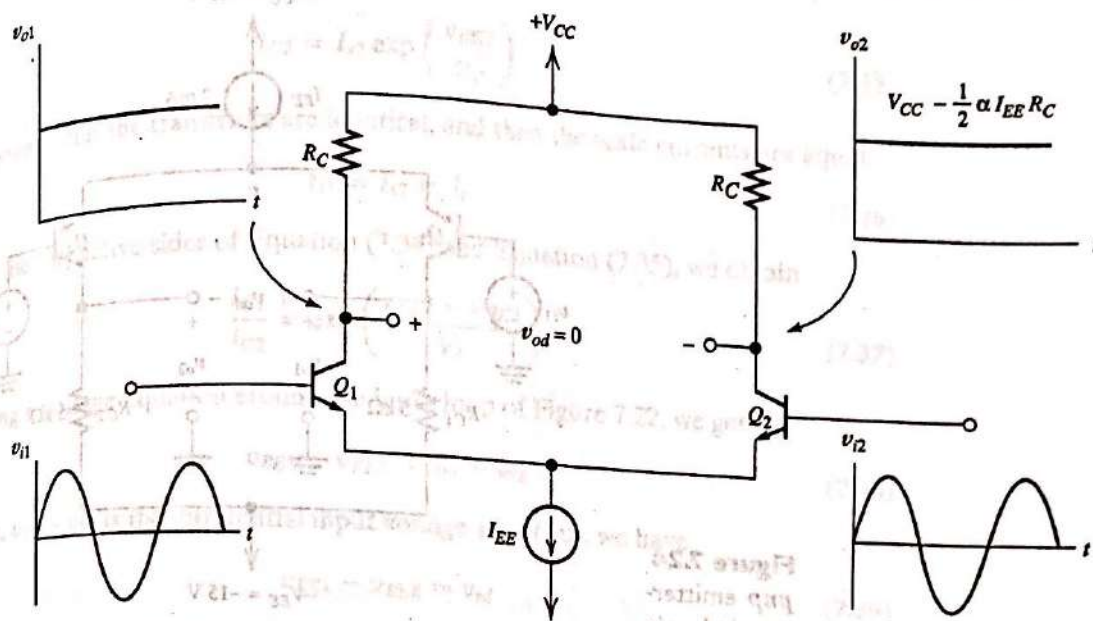
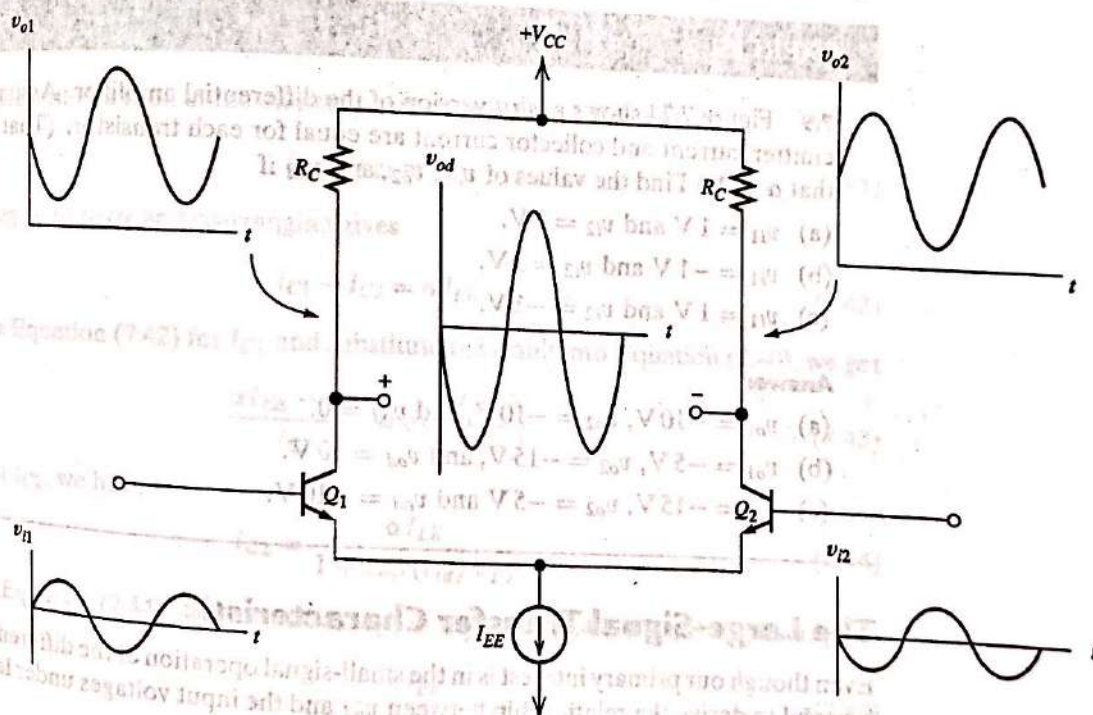

(a) Common-mode input signal ($v_{i1} = v_{i2}$)

(b) Differential input signal ($v_{i2} = -v_{i1}$)

Figure 7.23 Basic BJT differential amplifier with waveforms.

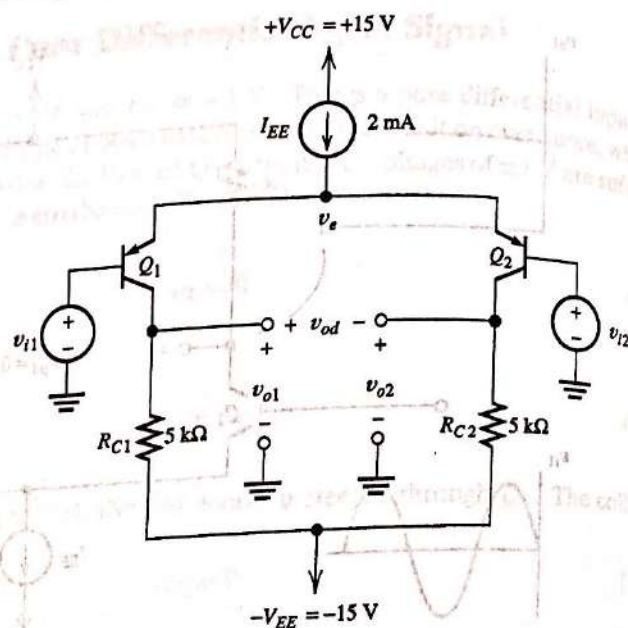


Figure 7.24
pnp emitter-coupled pair.

EXERCISE

7.9 Figure 7.24 shows a pnp version of the differential amplifier. Assume that the emitter current and collector current are equal for each transistor. (That is, assume that $\alpha \cong 1$.) Find the values of v_{o1} , v_{o2} , and v_{od} if

- (a) $v_{i1} = 1 \text{ V}$ and $v_{i2} = 1 \text{ V}$.
- (b) $v_{i1} = -1 \text{ V}$ and $v_{i2} = 1 \text{ V}$.
- (c) $v_{i1} = 1 \text{ V}$ and $v_{i2} = -1 \text{ V}$.

Answer

- (a) $v_{o1} = -10 \text{ V}$, $v_{o2} = -10 \text{ V}$, and $v_{od} = 0$.
- (b) $v_{o1} = -5 \text{ V}$, $v_{o2} = -15 \text{ V}$, and $v_{od} = 10 \text{ V}$.
- (c) $v_{o1} = -15 \text{ V}$, $v_{o2} = -5 \text{ V}$ and $v_{od} = -10 \text{ V}$.

The Large-Signal Transfer Characteristic

Even though our primary interest is in the small-signal operation of the differential pair, it is useful to derive the relationship between v_{od} and the input voltages under large-signal conditions.

Assuming that the transistors are operating in the active region, the collector currents are given by

$$i_{C1} = I_{S1} \exp\left(\frac{v_{BE1}}{V_T}\right) \quad (7.34)$$

$$i_{C2} = I_{S2} \exp\left(\frac{v_{BE2}}{V_T}\right) \quad (7.35)$$

We assume that the transistors are identical, and then the scale currents are equal:

$$I_{S1} = I_{S2} = I_S \quad (7.36)$$

Dividing the respective sides of Equation (7.34) and Equation (7.35), we obtain

$$\frac{i_{C1}}{i_{C2}} = \exp\left(\frac{v_{BE1} - v_{BE2}}{V_T}\right) \quad (7.37)$$

Writing a voltage equation around the input loop of Figure 7.22, we get

$$v_{BE1} - v_{BE2} = v_{i1} - v_{i2} \quad (7.38)$$

However, $v_{i1} - v_{i2}$ is the differential input voltage v_{id} . Thus, we have

$$v_{BE1} - v_{BE2} = v_{id} \quad (7.39)$$

Using Equation (7.39) to substitute for $v_{BE1} - v_{BE2}$ in Equation (7.37), we obtain

$$\frac{i_{C1}}{i_{C2}} = \exp\left(\frac{v_{id}}{V_T}\right) \quad (7.40)$$

Writing a current equation at the emitter junction in Figure 7.22 results in

$$i_{E1} + i_{E2} = I_{EE} \quad (7.41)$$

Substituting $i_E = i_C/\alpha$ and rearranging gives

$$i_{C1} + i_{C2} = \alpha I_{EE} \quad (7.42)$$

If we solve Equation (7.42) for i_{C1} and substitute the result into Equation (7.40), we get

$$\frac{\alpha I_{EE} - i_{C2}}{i_{C2}} = \exp\left(\frac{v_{id}}{V_T}\right) \quad (7.43)$$

Solving for i_{C2} , we have

$$i_{C2} = \frac{\alpha I_{EE}}{1 + \exp(v_{id}/V_T)} \quad (7.44)$$

Using Equation (7.44) to substitute for i_{C2} in Equation (7.40) and solving for i_{C1} , we obtain

$$i_{C1} = \frac{\alpha I_{EE}}{1 + \exp(-v_{id}/V_T)} \quad (7.45)$$

Plots of Equations (7.44) and (7.45) are shown in Figure 7.25. Notice that, for $v_{id} = 0$, we have $i_{C1} = i_{C2}$, as expected. For $v_{id} > 5V_T$, the current is steered almost entirely through Q_1 , and $i_{C2} \approx 0$. On the other hand, for $v_{id} < -5V_T$, the current flows almost entirely through Q_2 .

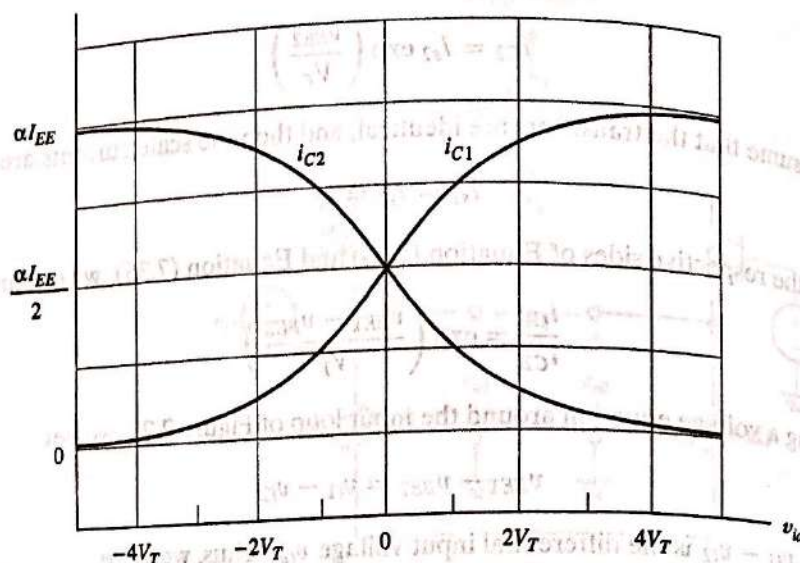


Figure 7.25 Collector currents versus differential input voltage.

If we use Equations (7.44) and (7.45) to substitute for the currents in Equation (7.26), we can eventually reduce the result to

$$v_{od} = \alpha I_{EE} R_C \tanh\left(\frac{-v_{id}}{2V_T}\right) \quad (7.46)$$

in which $\tanh$ is the **hyperbolic tangent** function. By definition, the hyperbolic tangent is

$$\tanh(x) = \frac{\exp(x) - \exp(-x)}{\exp(x) + \exp(-x)} \quad (7.47)$$

A plot of the transfer characteristic given by Equation (7.46) is illustrated in Figure 7.26. The curvature of the transfer characteristic shows that the differential amplifier can distort a signal if the amplitude is too large. For $|v_{id}| < V_T$, the characteristic is fairly straight, and the distortion is not excessive. Notice that if the magnitude of the input voltage exceeds $4V_T \cong 100 \text{ mV}$, the output will be severely clipped. (Sometimes we use the circuit as a waveshaper to convert a sinusoidal input into a square wave. It is quite effective for this purpose if the peak input is one volt or more.)

Emitter Degeneration

Sometimes it is advantageous to add emitter degeneration resistors R_{EF} to the circuit, as shown in Figure 7.27. (*Degeneration* is the term for negative feedback, which we consider in detail in Chapter 9.) We will see that these resistors have the disadvantage of reducing the differential voltage gain of the circuit. However, two reasons for including the resistors are to increase input impedance and to reduce distortion due to the nonlinearity of the BJTs. (These are also the reasons for using an unbypassed emitter resistor in a common-emitter amplifier.)

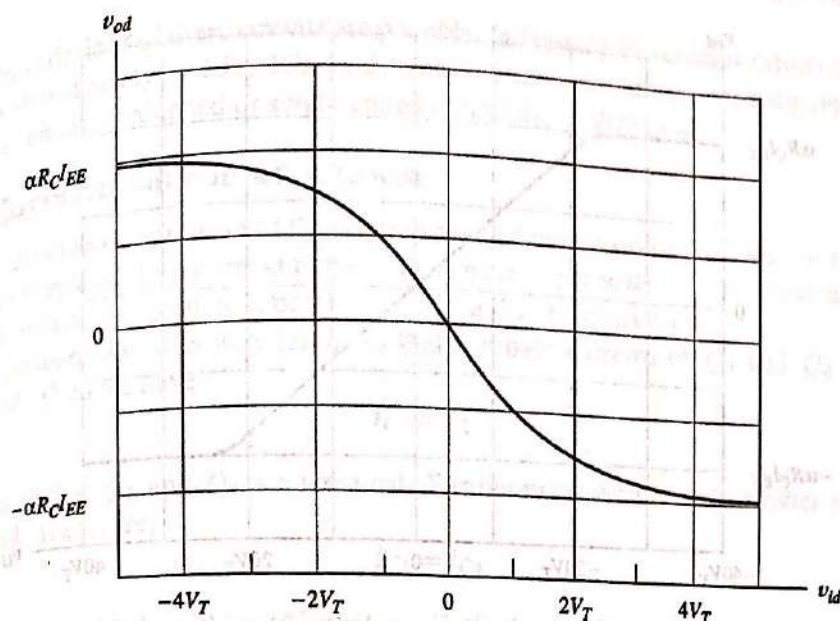


Figure 7.26 Voltage transfer characteristic of the BJT differential amplifier.

Figure 7.28 shows the transfer characteristic of the differential amplifier, including emitter degeneration resistors having the value $R_{EF} = 40V_T/I_{EE}$. (Of course, this choice is an example, and other values can be used for R_{EF} .) Compare Figure 7.28 with Figure 7.26. Notice that the characteristic with the emitter resistors is (approximately) straight for a wider range. Should we reduce the gain to improve the distortion performance or increase the input impedance? The answer depends on the application.

The BJT differential amplifier large-signal transfer characteristic becomes linear over a greater range if resistances are added in series with the emitters.

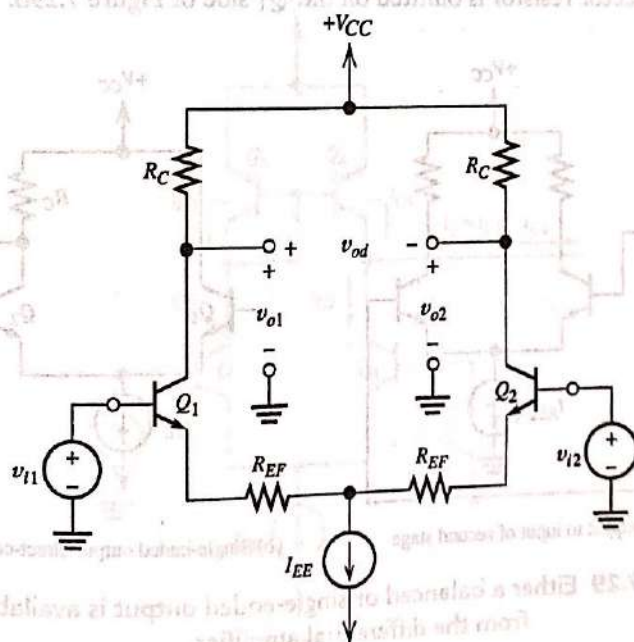


Figure 7.27 Differential amplifier with emitter degeneration resistors.

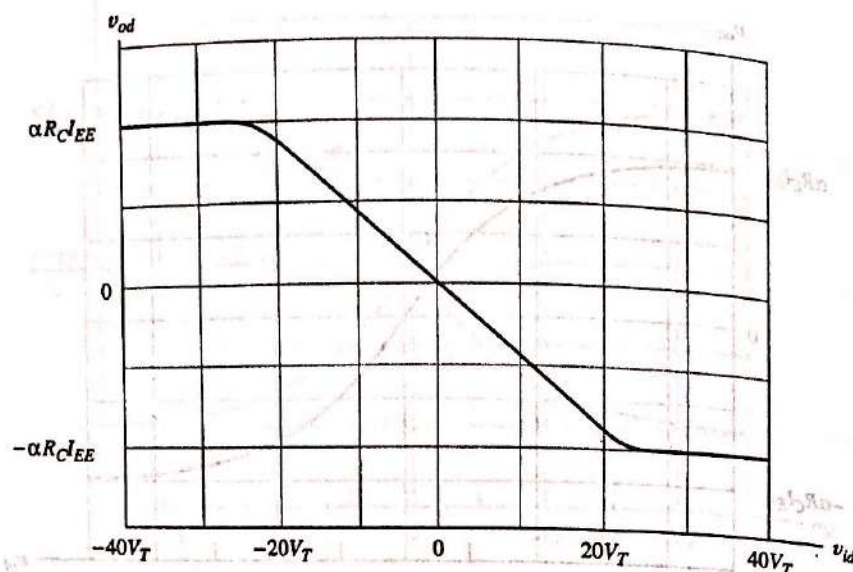


Figure 7.28 Voltage transfer characteristic with emitter degeneration resistors. $R_{EF} = 40(V_T/I_{EE})$.

Balanced Versus Single-Ended Outputs

The output of the emitter-coupled pair can be **balanced** as illustrated in Figure 7.29a. In this case, the output voltages from both collectors are connected to the inputs of another differential amplifier.

On the other hand, the output can be taken from one collector as shown in Figure 7.29b. In that case, we say that the output is **single ended**. If a single-ended output is desired, there is no need for a resistor in the collector of the other transistor. Thus, the collector resistor is omitted on the Q_1 side of Figure 7.29b.

Either a single-ended or a differential output can be taken from the differential pair, as shown in Figure 7.29.

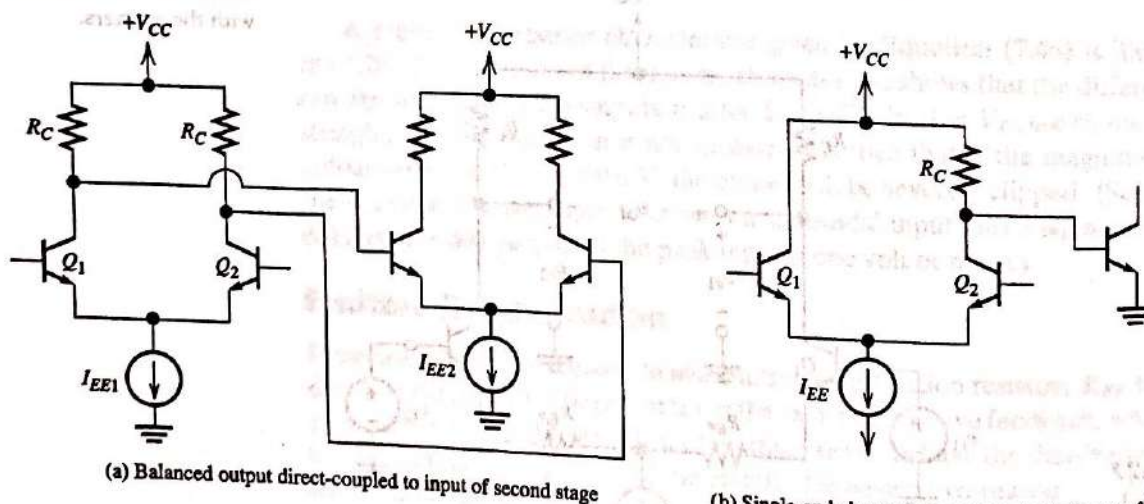


Figure 7.29 Either a balanced or single-ended output is available from the differential amplifier.

Many variations of these circuits are possible. In Figure 7.29, we show direct coupling, which is almost always used in ICs. In discrete circuits, we could use coupling capacitors to deliver either a balanced or single-ended output signal to the load.

The Current Mirror as a Load

Figure 7.30 shows a variation of the emitter-coupled pair in which the collector resistors have been replaced by a current mirror. This circuit is particularly advantageous in ICs, because transistors consume much less chip area than resistors do.

We assume that β is very large, so that the base currents of Q_3 and Q_4 can be neglected. Then we have

$$i_{C3} = i_{C1} \quad (7.48)$$

We assume that Q_3 and Q_4 are identical. Furthermore, their base-to-emitter voltages are equal. Therefore,

$$i_{C3} = i_{C4} \quad (7.49)$$

Equating the right-hand sides of Equations (7.48) and (7.49), we have

$$i_{C4} = i_{C1} \quad (7.50)$$

Writing a current equation at the collector of Q_2 , we obtain

$$i_o = i_{C4} - i_{C2} \quad (7.51)$$

Using Equation (7.50) to substitute for i_{C4} in Equation (7.51) yields

$$i_o = i_{C1} - i_{C2} \quad (7.52)$$

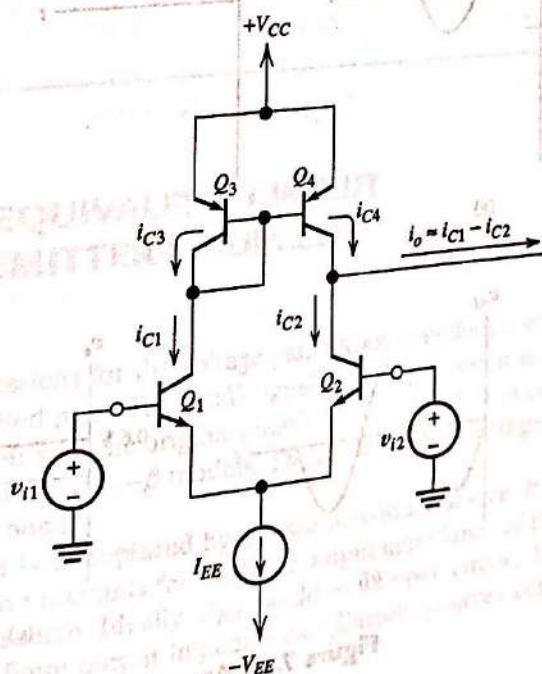


Figure 7.30
Emitter-coupled
pair with current-
mirror load.

Using Equations (7.44) and (7.45) to substitute for i_{C1} and i_{C2} in Equation (7.52) eventually results in

$$i_o = \alpha I_{EE} \tanh\left(\frac{v_{id}}{2V_T}\right) \quad (7.53)$$

For $|v_{id}| < V_T$, i_o is approximately proportional to v_{id} . Thus, for small signals, the circuit produces an output current that is proportional to the differential input voltage. Furthermore, the common-mode input component does not affect the output current.

The current mirror is a more practical load than resistors are for differential pairs in integrated circuits.

EXERCISE

7.10 Consider the circuit of Figure 7.24. Suppose that $v_{i1} = 10 \sin(20\pi t)$ mV and $v_{i2} = -10 \sin(20\pi t)$ mV. Sketch the following voltages against time:

- $v_{id}(t)$ to scale.
- $v_{icm}(t)$ to scale.
- $v_{o1}(t)$ (need not be to scale).
- $v_{od}(t)$ (need not be to scale).
- $v_e(t)$ to scale.

Answer See Figure 7.31. (You can also check your answers by using SPICE. However, you learn best by first trying to sketch the waveforms on your own.)

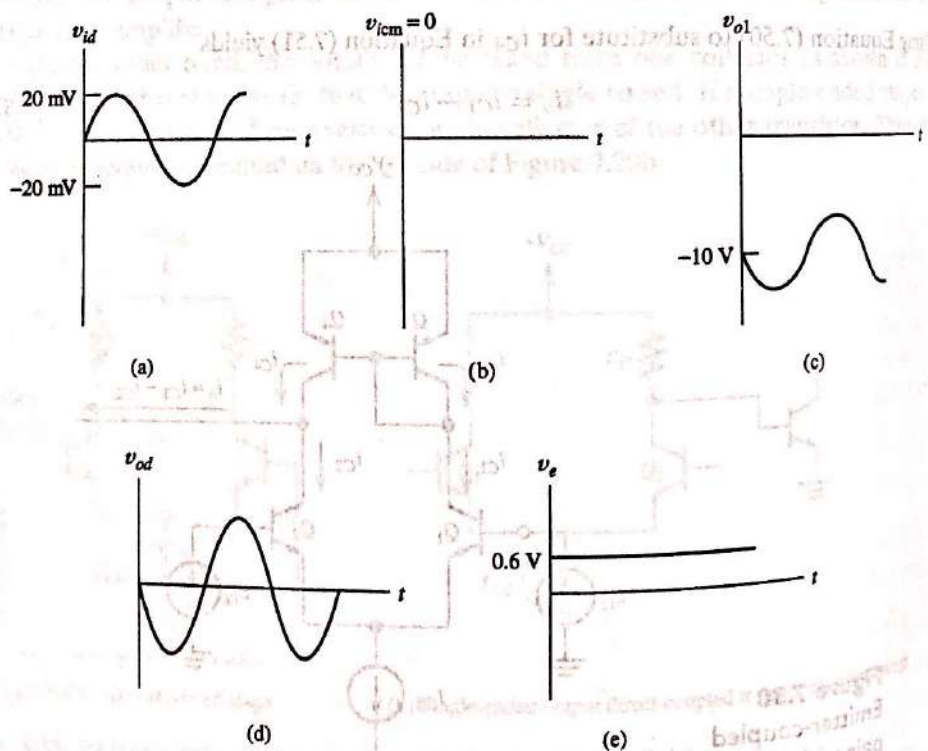


Figure 7.31 Answers for Exercise 7.10.

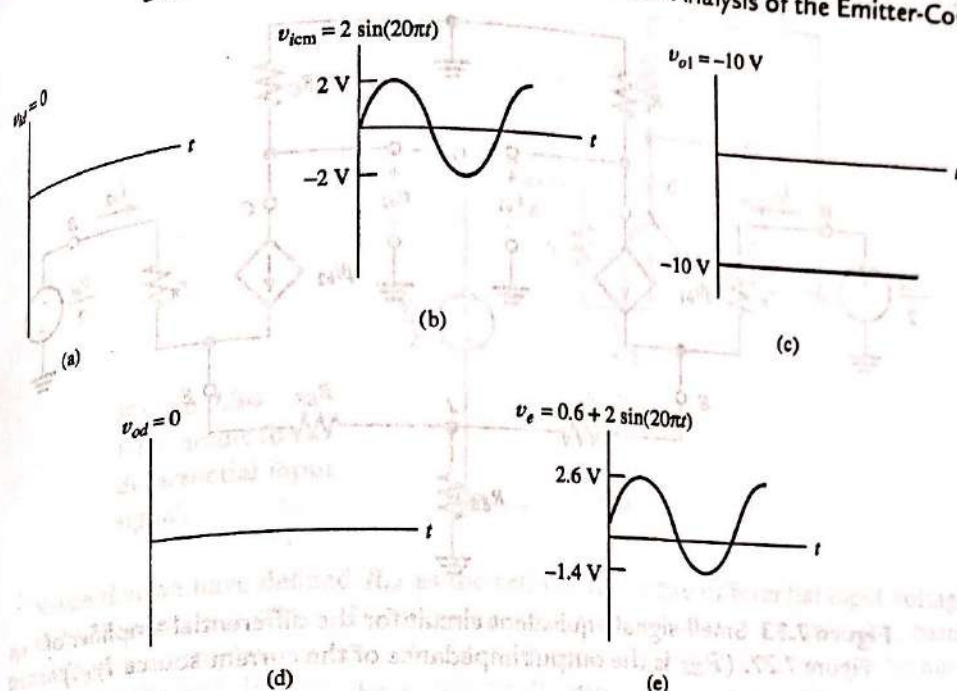


Figure 7.32 Answers for Exercise 7.11.

EXERCISE

7.11 Repeat Exercise 7.10 for $v_{i1} = v_{i2} = 2 \sin(20\pi t)$ V.

Answer See Figure 7.32.

7.5 SMALL-SIGNAL EQUIVALENT-CIRCUIT ANALYSIS OF THE EMITTER-COUPLED DIFFERENTIAL PAIR

In this section, we derive expressions for the voltage gain, input impedance, and output impedance of the emitter-coupled pair. The small-signal equivalent circuit is shown in Figure 7.33. Compare this circuit with the original circuit in Figure 7.27. Notice that the transistors have been replaced by their $r_{\pi}-\beta$ models. The power-supply voltage has been replaced by a short circuit to ground.

The I_{EE} current source has been replaced by a resistor with resistance R_{EE} in the equivalent circuit. This resistance accounts for the finite output impedance of the circuit used to implement the current source. Ideally, R_{EE} would be an open circuit. However, practical current sources have finite output impedances. (Current sources suitable for biasing in ICs are discussed in Sections 7.2 and 7.3.)

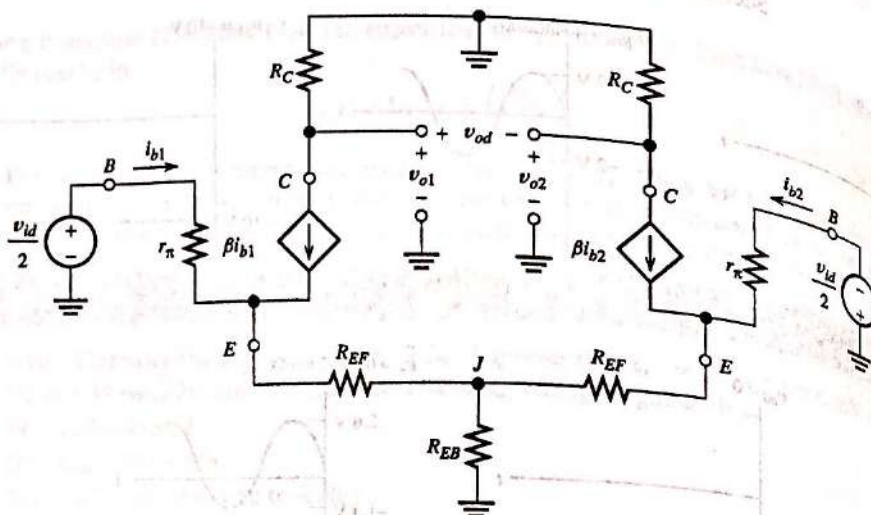


Figure 7.33 Small-signal equivalent circuit for the differential amplifier of Figure 7.27. (R_{EB} is the output impedance of the current source I_{EE} .)

Analysis for the Differential Input Signal

First, we analyze the circuit for a pure differential input signal. Thus, the input voltages are $v_{i1} = -v_{i2} = v_d/2$. [Notice that the differential voltage between the input (i.e., base) terminals is v_d .]

The analysis can be simplified by observing that the equivalent circuit (Figure 7.33) is symmetrical. The left half is the mirror image of the right half, except for the polarity of the input voltage. The input voltage is $+v_d/2$ on the left-hand side and $-v_d/2$ on the right-hand side. Because of this symmetry and the opposite polarity of the independent sources, the voltage at point J (see Figure 7.33) is zero. Thus, the circuit behavior would be unchanged by shorting point J to ground. (Keep in mind that this is true only for a pure differential input signal.)

Shorting point J to ground results in two identical (except for source polarity) and independent circuits, one on the left and one on the right. The half circuit for the left-hand side is illustrated in Figure 7.34. We need to analyze only this half circuit, because the voltages in the right half are identical, except for having reversed polarity.

From the differential half circuit of Figure 7.34, we can write the following equations:

$$\frac{v_{id}}{2} = r_{\pi} i_{b1} + (\beta + 1) i_{b1} R_{EF} \quad (7.54)$$

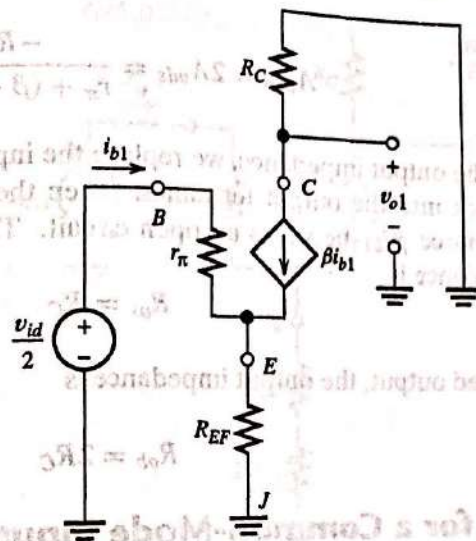
and

$$v_{o1} = -R_C \beta i_{b1} \quad (7.55)$$

From these equations, we can find the input impedance and voltage gain. For example, the input impedance seen looking into the input terminals can be found from Equation (7.54):

$$R_{id} = \frac{v_{id}}{i_{b1}} = 2[r_{\pi} + (\beta + 1)R_{EF}] \quad (7.56)$$

Figure 7.34
Half-circuit for a
differential input
signal.



Notice that we have defined R_{id} as the ratio of the entire differential input voltage v_{id} to the input current. Thus, R_{id} is the input impedance between the input (i.e., base) terminals of the complete circuit. (A potential point of confusion arises here because we have used the half circuit to derive this result. However, R_{id} is the differential input impedance for the complete circuit because it is defined as the ratio of the total differential input voltage divided by the input current.)

From Equations (7.54) and (7.55), we can find the voltage gain as

$$A_{vds} = \frac{v_{o1}}{v_{id}} = \frac{-R_C \beta}{2[r_{\pi} + (\beta + 1)R_{EF}]} \quad (7.57)$$

where A_{vds} is the voltage gain for a differential input and single-ended output. (In the subscript of vds , v stands for voltage gain, d denotes a differential input signal, and s symbolizes single-ended output.)

Sometimes the circuit drives a balanced load, and then the differential output voltage is $v_{od} = v_{o1} - v_{o2}$. By symmetry, the output voltage for the right half circuit is $v_{o2} = -v_{o1}$. Thus, the differential output voltage is

$$v_{od} = v_{o1} - v_{o2} = 2v_{o1} \quad (7.58)$$

We define the gain for a balanced output as

$$A_{vdb} = \frac{v_{od}}{v_{id}} \quad (7.59)$$

(Here, the subscript v designates the voltage gain, d indicates a differential input signal, and b signifies a balanced load.) Using Equation (7.58) to substitute for v_{od} , we find that

$$A_{vdb} = \frac{2v_{o1}}{v_{id}} \quad (7.60)$$

Thus, we have

$$A_{vdb} = 2A_{vds} = \frac{-R_C \beta}{r_\pi + (\beta + 1)R_{EF}} \quad (7.61)$$

To find the output impedance, we replace the input voltage sources by short circuits and look back into the output terminals. Then the input current i_{b1} is zero, and the controlled source βi_{b1} becomes an open circuit. Thus, for a single-ended output, the output impedance is

$$R_{os} = R_C \quad (7.62)$$

For a balanced output, the output impedance is

$$R_{ob} = 2R_C \quad (7.63)$$

Analysis for a Common-Mode Input Signal

Now we turn our attention to the behavior of the circuit for a pure common-mode input signal. Thus, the input voltages are

$$v_{i1} = v_{i2} = v_{icm} \quad (7.64)$$

The equivalent circuit is depicted in Figure 7.35. Here, we have shown the output impedance of the I_{EE} current source as the parallel combination of two resistors each with resistance $2R_{EB}$. Of course, this combination is equivalent to a single resistance R_{EB} .

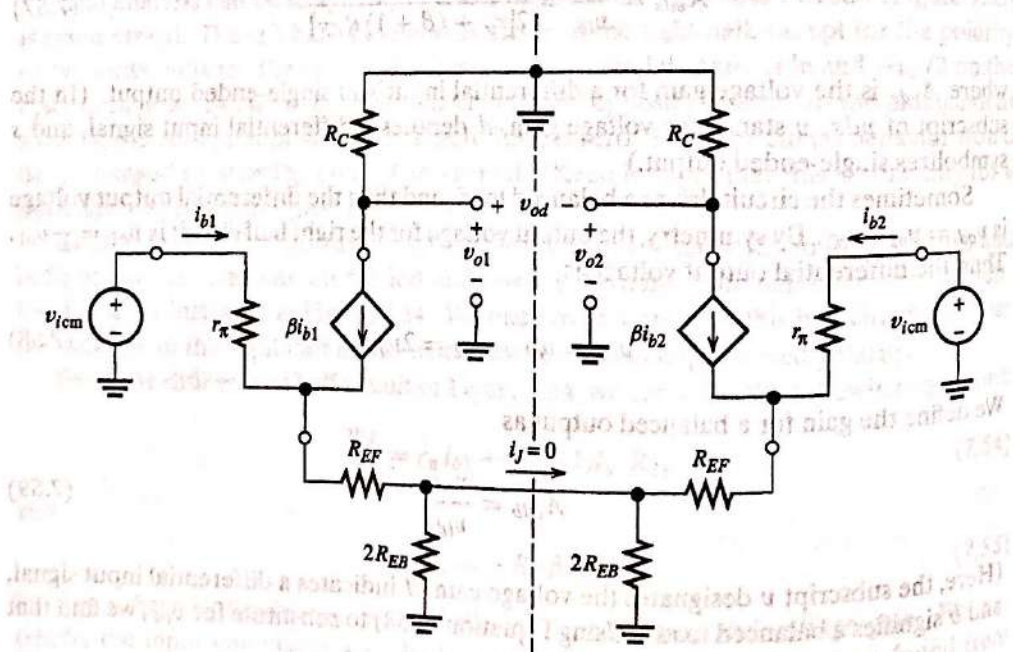
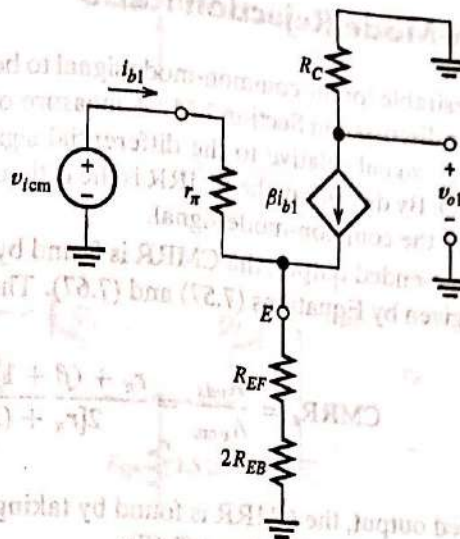


Figure 7.35 Small-signal equivalent circuit with a pure common-mode input signal.

Figure 7.36
Half-circuit for
a pure common-
mode input signal.



The equivalent circuit is symmetrical with respect to the dashed line shown in Figure 7.35, including the polarities of the signal sources. Therefore, we conclude that the current i_J must be zero. Because i_J is zero, we can open the connection between the two halves of the circuit, and no change occurs in any of the currents or voltages. Once again, we can consider the left-hand and the right-hand halves of the circuit separately.

The equivalent circuit for the left half of the circuit is shown in Figure 7.36. From this equivalent circuit, we can derive the desired results. For example, we can show that

$$R_{i\text{ cm}} = \frac{v_{i\text{ cm}}}{i_{b1} + i_{b2}} = \frac{r_{\pi} + (\beta + 1)R_{EF}}{2} + (\beta + 1)R_{EB} \quad (7.65)$$

We have defined the common-mode input impedance to be the voltage divided by the total current that the source must deliver to both input terminals. In other words, this is the impedance “seen” by the source if both input terminals are tied together and driven by a single source.

Notice that because of symmetry, $v_{o1} = v_{o2}$. Thus, a pure common-mode input gives rise to a pure common-mode output. Of course, if any components are mismatched, a differential output component could arise from a pure common-mode input.

The voltage gain for a common-mode input and a single-ended load is

$$A_{v\text{ cm}} = \frac{v_{o1}}{v_{i\text{ cm}}} = \frac{-R_C\beta}{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})} \quad (7.66)$$

Because $v_{o1} = v_{o2} = v_{o\text{ cm}}$, this is also the gain for the common-mode output voltage applied to a balanced load. Thus, we can also write

$$A_{v\text{ cm}} = \frac{v_{o\text{ cm}}}{v_{i\text{ cm}}} = \frac{-R_C\beta}{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})} \quad (7.67)$$

The output impedances are given by Equations (7.62) and (7.63), regardless of whether the input signal is differential or common mode. (In either case, we set the input sources to zero when finding the output impedance.)

... if any components are mismatched, a differential output component could arise from a pure common-mode input.

Common-Mode Rejection Ratio

Often, it is desirable for the common-mode signal to be rejected in favor of the differential signal. This is discussed in Section 1.11. A measure of how well the amplifier rejects the common-mode signal relative to the differential signal is the **common-mode rejection ratio (CMRR)**. By definition, the CMRR is the ratio of the gain for the differential signal to the gain for the common-mode signal.

For a single-ended output, the CMRR is found by taking the ratio of the magnitudes of the gains given by Equations (7.57) and (7.67). The result is

$$\text{CMRR}_s = \frac{A_{vds}}{A_{vcm}} = \frac{r_\pi + (\beta + 1)(R_{EF} + 2R_{EB})}{2[r_\pi + (\beta + 1)R_{EF}]} \quad (7.68)$$

For a balanced output, the CMRR is found by taking the ratio of the magnitudes of the gains given by Equations (7.61) and (7.67):

$$\text{CMRR}_b = \frac{A_{vdb}}{A_{vcm}} = \frac{r_\pi + (\beta + 1)(R_{EF} + 2R_{EB})}{r_\pi + (\beta + 1)R_{EF}} \quad (7.69)$$

Notice that the CMRR is twice as large for a balanced output as for a single-ended output.

Because r_π is proportional to β , all of the terms in the numerator and denominator of the expressions for the CMRR are approximately proportional to β (for $\beta \gg 1$). Thus, CMRR is nearly independent of β .

The primary approach that a designer can take to achieve a high CMRR is to make sure that the circuit components are well matched, to select a large value for R_{EB} , and to select a small value for R_{EF} .

The primary approach that a designer can take to achieve a high CMRR is to make sure that the circuit components are well matched, to select a large value for R_{EB} , and to select a small value for R_{EF} .

EXERCISE

7.12 Starting from the equivalent circuit of Figure 7.36, derive the expressions

- given by Equation (7.65) for the common-mode input impedance.
- given by Equation (7.66) for A_{vcm} .

EXERCISE

7.13 The circuit diagram of a discrete-component emitter-coupled pair is shown in Figure 7.37. The transistors have $\beta = 200$ and $I_s = 10^{-13}$. Assume matched transistors and a temperature of 300 K.

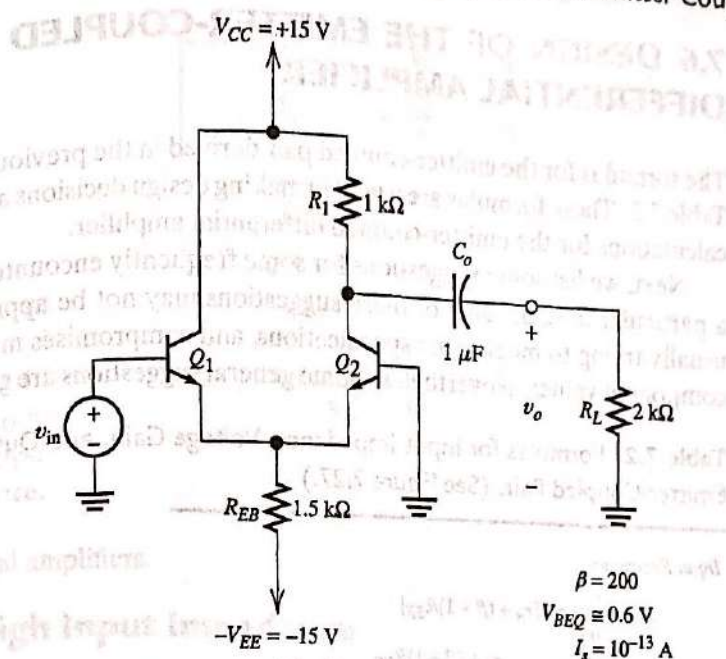


Figure 7.37
Emitter-coupled
pair of Exercise 7.13.

- Perform a dc analysis of the circuit to determine I_{CQ} and V_{CEQ} for each transistor. In the Q -point analysis, assume that $v_{in} = 0$. Calculate the value of r_{π} .
- Draw the midband small-signal equivalent circuit, and show that it is identical to the circuit illustrated in Figure 7.33 if we define $R_C = R_1 || R_L$. Assume that the output coupling capacitor is a short circuit for the ac signal. (The resistor is missing from the collector of Q_1 , but this is of no consequence because the output is taken from the collector of Q_2 . Also, we have $R_{EF} = 0$.)
- Assume that the input signal v_{in} can be treated as a pure differential signal. Use the formulas developed in this section to compute the values of $A_v = v_o/v_{in}$, the input impedance seen by v_{in} , and the output impedance of the amplifier. [Actually, the input signal has both a differential component $v_{id} = v_{i1} - v_{i2} = v_{in}$ and a common-mode component $v_{icm} = (1/2)(v_{i1} + v_{i2}) = v_{in}/2$. However, the effect of the differential signal swamps out the effect of this relatively small common-mode signal. This is because the gain for the differential signal is much higher.]
- Use a SPICE program to obtain a Bode plot for the voltage gain. Compare the midband voltage gain with the value found in part (c). Also, use the SPICE program to find the input impedance and compare it with the midband value found in part (c).

Answer

- $I_{CQ1} = I_{CQ2} \cong 4.78 \text{ mA}$, $V_{CE1} = 15.6 \text{ V}$, $V_{CE2} = 10.8 \text{ V}$, and $r_{\pi1} = r_{\pi2} = 1090 \Omega$.
- $A_v = v_o/v_{in} = 61.2$, $R_{in} = v_{in}/i_{in} = 2180 \Omega$, and $R_o = R_1 = 1 \text{ k}\Omega$.
- The schematic is stored in file Exer7.13.

7.6 DESIGN OF THE EMITTER-COUPLED DIFFERENTIAL AMPLIFIER

The formulas for the emitter-coupled pair derived in the previous section are collected in Table 7.2. These formulas are useful in making design decisions and in initial performance calculations for the emitter-coupled differential amplifier.

Next, we list some suggestions for some frequently encountered design problems. In a particular design, some of these suggestions may not be appropriate, because we are usually trying to meet many specifications, and compromises must be found in selecting component values. Nevertheless, some general suggestions are given for you to reference

Table 7.2. Formulas for Input Impedance, Voltage Gain, and Output Impedance of the Emitter-Coupled Pair. (See Figure 7.27.)

Input Resistance

$$R_{id} = \frac{v_{id}}{i_{b1}} = 2[r_{\pi} + (\beta + 1)R_{EF}]$$

$$R_{icm} = \frac{v_{icm}}{i_{b1} + i_{b2}} = \frac{r_{\pi} + (\beta + 1)R_{EF}}{2} + (\beta + 1)R_{EB}$$

Voltage Gains for Single-Ended Output

$$A_{vds} = \frac{v_{o1}}{v_{id}} = \frac{-R_c\beta}{2[r_{\pi} + (\beta + 1)R_{EF}]} \quad (\text{output taken from } Q_1)$$

or

$$A_{vds} = \frac{v_{o2}}{v_{id}} = \frac{R_c\beta}{2[r_{\pi} + (\beta + 1)R_{EF}]} \quad (\text{output taken from } Q_2)$$

$$A_{vcm} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = \frac{-R_c\beta}{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})}$$

Voltage Gains for Balanced Output

$$A_{vdb} = \frac{v_{od}}{v_{id}} = \frac{-R_c\beta}{r_{\pi} + (\beta + 1)R_{EF}}$$

$$A_{vcm} = \frac{v_{ocm}}{v_{icm}} = \frac{-R_c\beta}{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})}$$

Output Impedance for Single-Ended Output

$$R_{os} = R_c$$

Output Impedance for Balanced Output

$$R_{ob} = 2R_c$$

CMRR for Single-Ended Output

$$\text{CMRR}_s = \frac{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})}{2[r_{\pi} + (\beta + 1)R_{EF}]}$$

CMRR for Balanced Output

$$\text{CMRR}_b = \frac{r_{\pi} + (\beta + 1)(R_{EF} + 2R_{EB})}{r_{\pi} + (\beta + 1)R_{EF}}$$

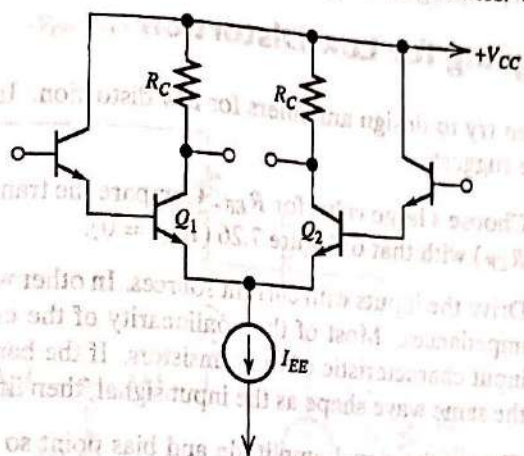


Figure 7.38
Addition of
emitter fol-
lowers to in-
crease input
impedance.

as you design differential amplifiers.

Designing for High Input Impedance

Often, we face the problem of designing a differential amplifier that has high input impedance, for both the differential signal and the common-mode signal. We offer the following design suggestions:

1. Choose a large value of R_{EF} . (Unfortunately, this also reduces gain and CMRR.)
2. Choose transistors that have high β .
3. Select a low value of bias current I_{EE} . This allows large resistances to be used and gives a large value for r_{π} . [Recall that $r_{\pi} = (\beta V_T)/I_{CQ}$.]
4. Design the I_{EE} current source to maximize its output impedance R_{EB} . (This increases the common-mode input impedance, but not the differential input impedance.)
5. Choose a modified circuit configuration, such as that of the circuit shown in Figure 7.38, which has emitter followers between the input terminals and the bases of Q_1 and Q_2 .
6. Consider changing to a FET differential amplifier, such as any of those discussed in Section 7.7.

Designing for Large CMRR

Another common design problem is to achieve a high CMRR. Some suggestions are as follows:

1. Make sure that the two sides of the circuit are as perfectly matched as is practical. (If the transistor parameters or resistor values are mismatched, the common-mode input voltage can be converted into a differential output voltage.)
2. Design the bias current source I_{EE} to have a high output impedance.
3. Cascade several stages of emitter-coupled differential amplifiers, as indicated in Figure 7.29a. The common-mode output signal of the first stage is further rejected by the second stage. Notice, however, that the second stage does not help if asymmetry of the first stage has converted a common-mode signal into a differential signal.

Designing for Low Distortion

We often try to design amplifiers for low distortion. In the case of the emitter-coupled pair, we suggest:

1. Choose a large value for R_{EF} . Compare the transfer function of Figure 7.28 (large R_{EF}) with that of Figure 7.26 ($R_{EF} = 0$).
2. Drive the inputs with current sources. In other words, choose high internal source impedances. Most of the nonlinearity of the emitter-coupled pair is due to the input characteristic of the transistors. If the base currents can be forced to have the same wave shape as the input signal, then little distortion occurs.
3. Choose the signal amplitude and bias point so that the peak signal current is a small fraction of the Q -point current.

Next, we show a design example for the differential amplifier.

Example 7.4 Emitter-Coupled-Differential-Amplifier Design

Design an emitter-coupled pair differential amplifier suitable for discrete implementation and having the following specifications:

- Direct-coupled differential input.
- Ac-coupled single-ended output.
- $R_L = 1 \text{ k}\Omega$.
- Output amplitude capability of 2 V peak.
- $A_{vds} = 10$ (nominal value).
- Half-power bandwidth from 1 Hz to at least 1 kHz.
- CMRR = 80 dB minimum from 1 Hz to at least 1 kHz.

The transistors to be used are assumed to be identical and to have the following parameters:

$$\beta = \beta_F = 200;$$

$$I_s = I_S = 10^{-14} \text{ A};$$

$$V_A = V_{AF} = 100 \text{ V (Early voltage)}.$$

The available power-supply voltages are $V_{CC} = +15 \text{ V}$ and $V_{EE} = -15 \text{ V}$.

SOLUTION First, we select a circuit configuration. It is desirable to minimize the number of components in any design. Therefore, we start with the simple circuit configuration shown in Figure 7.39.

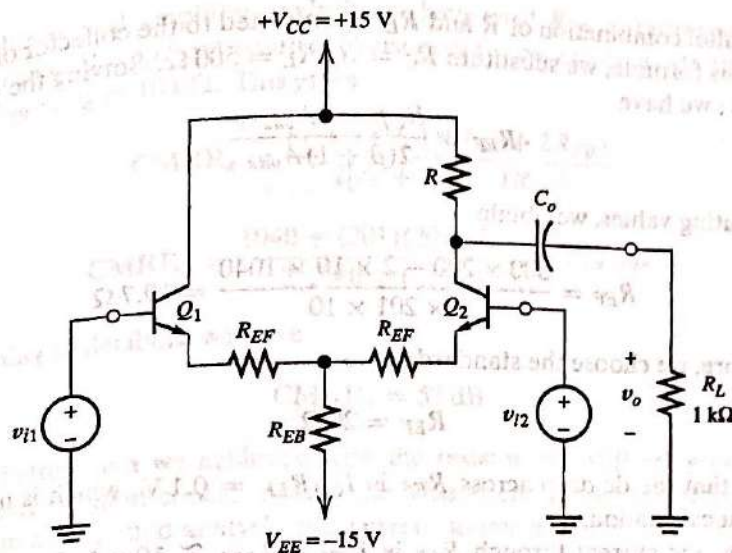


Figure 7.39 First attempt in Example 7.4.

Next, we consider how to choose the value of R and the Q -point for Q_2 . The amplifier is required to produce at least 2-V-peak ac voltage across the load without clipping. Thus, the peak load current is $(2\text{ V})/(1\text{ k}\Omega) = 2\text{ mA}$. Also, a peak ac current of $2/R$ flows through the collector bias resistor R . (We assume that R is the resistance in $\text{k}\Omega$.) Then the peak ac collector current (in mA) is $2 + (2/R)$. The Q -point collector current of Q_2 must be greater than the peak ac current, or clipping will occur due to cut-off. Hence, we require that

$$I_{CQ2} > 2 + \frac{2}{R} \quad (7.70)$$

Furthermore, the Q -point value of the collector-to-emitter voltage of Q_2 must be greater than 2.2 V, or clipping will occur due to saturation. Somewhat arbitrarily, we choose $R = 1\text{ k}\Omega$ and $I_{CQ2} = 5\text{ mA}$. These choices satisfy Equation (7.70) and result in $V_{CEQ2} = V_{CC} - I_{CQ2}R + V_{BEQ2} \cong 10.6\text{ V}$, which is large enough to ensure that clipping due to saturation does not occur. Other values could be chosen that would work just as well.

Now we can compute

$$r_{\pi} = \frac{\beta V_T}{I_{CQ}} = \frac{200 \times 26\text{ mV}}{5\text{ mA}} = 1040\ \Omega$$

Table 7.2 gives the following formula for the differential voltage gain:

$$A_{vds} = \frac{v_{o2}}{v_{id}} = \frac{R_C \beta}{2[r_{\pi} + (\beta + 1)R_{EF}]}$$

This formula was derived for the equivalent circuit of Figure 7.33, in which the only resistor connected to the collector is R_C . In the circuit at hand (Figure 7.39),

the parallel combination of R and R_L is connected to the collector of Q_2 . Thus, in using this formula, we substitute $R_C = R || R_L = 500 \Omega$. Solving the gain equation for R_{EF} , we have

$$R_{EF} = \frac{R_C \beta - 2A_{vds}r_\pi}{2(\beta + 1)A_{vds}}$$

Substituting values, we obtain

$$R_{EF} = \frac{500 \times 200 - 2 \times 10 \times 1040}{2 \times 201 \times 10} = 19.7 \Omega$$

Therefore, we choose the standard value

$$R_{EF} = 20 \Omega$$

Notice that the dc drop across R_{EF} is $I_{CQ}R_{EF} = 0.1 \text{ V}$, which is negligible in Q -point calculations.

Now, the current through R_{EB} is $I_{CQ1} + I_{CQ2} \cong 10 \text{ mA}$, because $I_{CQ1} \cong I_{CQ2} \cong 5 \text{ mA}$. Neglecting the drop across R_{EF} , the voltage across R_{EB} is $15 - V_{BEQ} \cong 14.4 \text{ V}$. Thus, we have

$$R_{EB} = \frac{14.4 \text{ V}}{10 \text{ mA}} = 1.44 \text{ k}\Omega$$

and we select the standard value $R_{EF} = 1.5 \text{ k}\Omega$.

Now the CMRR can be computed. From Table 7.2,

$$\text{CMRR}_s = \frac{r_\pi + (\beta + 1)(R_{EF} + 2R_{EB})}{2[r_\pi + (\beta + 1)R_{EF}]}$$

Substituting values, we obtain

$$\text{CMRR}_s = \frac{1040 + (201)(20 + 2 \times 1500)}{2[1040 + (201) \times 20]} \cong 60$$

Converting to decibels, yields

$$\text{CMRR}_s = 20 \log(60) = 35.6 \text{ dB}$$

Therefore, we have a problem: The circuit does not meet the desired CMRR specification. Furthermore, it is not possible to solve this problem by adjusting component values. Accordingly, we must consider a different circuit configuration.

The circuit seems to be capable of meeting all of the specifications except that for CMRR. If the value of R_{EB} could be increased, the CMRR would increase. Therefore, we propose to replace R_{EB} by one of the current sources discussed in Section 7.2. First, let us consider the simple current mirror of Figure 7.1. As in Example 7.2, the output impedance of the current mirror is

$$r_o = \left(\frac{\partial I_C}{\partial V_{CE}} \right)^{-1} \cong \left(\frac{I_C}{V_A} \right)^{-1} \cong \left(\frac{10 \text{ mA}}{100 \text{ V}} \right)^{-1} = 10 \text{ k}\Omega$$

In the differential-amplifier analysis, we have used R_{EB} to represent the output impedance of the current source. Consequently, we can compute the CMRR by using $R_{EB} = r_o = 10 \text{ k}\Omega$. This gives

$$\text{CMRR}_s = \frac{r_\pi + (\beta + 1)(R_{EF} + 2R_{EB})}{2[r_\pi + (\beta + 1)R_{EF}]}$$

$$\text{CMRR}_s = \frac{1040 + (201)(20 + 2 \times 10^4)}{2[1040 + (201) \times 20]} = 398$$

Converting to decibels, we have

$$\text{CMRR}_s = 52 \text{ dB}$$

This is better than we achieved with the resistor, but still not good enough. Therefore, we next consider using the Wilson current source of Figure 7.10. Based on a simplified analysis, this current source has infinite output impedance. However, in practice, we find that the impedance is finite. Nevertheless, the Wilson current source is much better than the simple current mirror and, hopefully, will allow our circuit to achieve the desired CMRR specification. The circuit, including the Wilson current source, is illustrated in Figure 7.40.

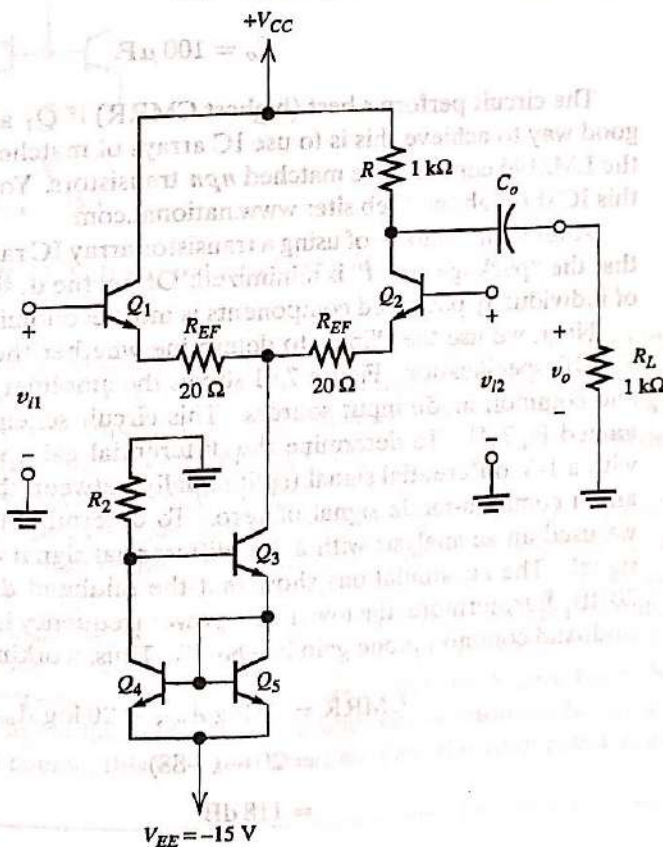


Figure 7.40
Differential
amplifier of
Example 7.4
using the Wil-
son current
source.

In this circuit, R_2 , Q_3 , Q_4 , and Q_5 form the Wilson source. The upper end of resistor R_2 could be connected either to $+V_{CC}$ or to ground. We have elected to connect R_2 to ground, because this reduces its voltage drop and power dissipation. The current through R_2 is the desired bias current, which is 10 mA. The voltage across R_2 is $15 - V_{BEQ5} - V_{BEQ3} \cong 13.8$ V. Thus, we have $R_2 = 13.8 \text{ V}/10 \text{ mA} = 1.38 \text{ k}\Omega$. We choose the standard value

$$R_2 = 1.3 \text{ k}\Omega$$

Next, we select the output coupling capacitor. The resistance in series with C_o is $R + R_L$. In Chapter 8, we will see that the break frequency is

$$f_o = \frac{1}{2\pi C_o(R + R_L)}$$

The desired specifications call for a lower 3-dB frequency of 1 Hz. Solving for C_o and substituting values, we have

$$C_o = \frac{1}{2\pi f_o(R + R_L)} = \frac{1}{2\pi(1000 + 1000)} \cong 79.6 \mu\text{F}$$

Therefore, we choose the standard value

$$C_o = 100 \mu\text{F}$$

The circuit performs best (highest CMRR) if Q_1 and Q_2 are well matched. A good way to achieve this is to use IC arrays of matched transistors. For example, the LM3146 contains five matched *nnp* transistors. You can find the data sheet for this IC through the Web site: www.national.com

Another advantage of using a transistor array IC rather than separate devices is that the "package count" is minimized. Often, the design using the fewest number of individually packaged components is most economical.

Next, we use the PSpice to determine whether the circuit meets the desired CMRR specification. Figure 7.41 shows the amplifier, as well as the differential and common-mode input sources. This circuit schematic is stored in the file named Fig7.41. To determine the differential gain, we used an ac simulation with a 1-V differential signal (split equally between the two differential sources) and a common-mode signal of zero. To determine the common-mode gain, we used an ac analysis with a 0-V differential signal and a 1-V common-mode signal. The ac simulations show that the midband differential gain is in fact 20 dB. Furthermore, the lower half-power frequency is approximately 0.8 Hz. The midband common-mode gain is -88 dB. Thus, working in decibels, we obtain

$$\begin{aligned} \text{CMRR} &= 20 \log A_{vds} - 20 \log A_{vcm} \\ &= 20 - (-88) \\ &= 118 \text{ dB} \end{aligned}$$

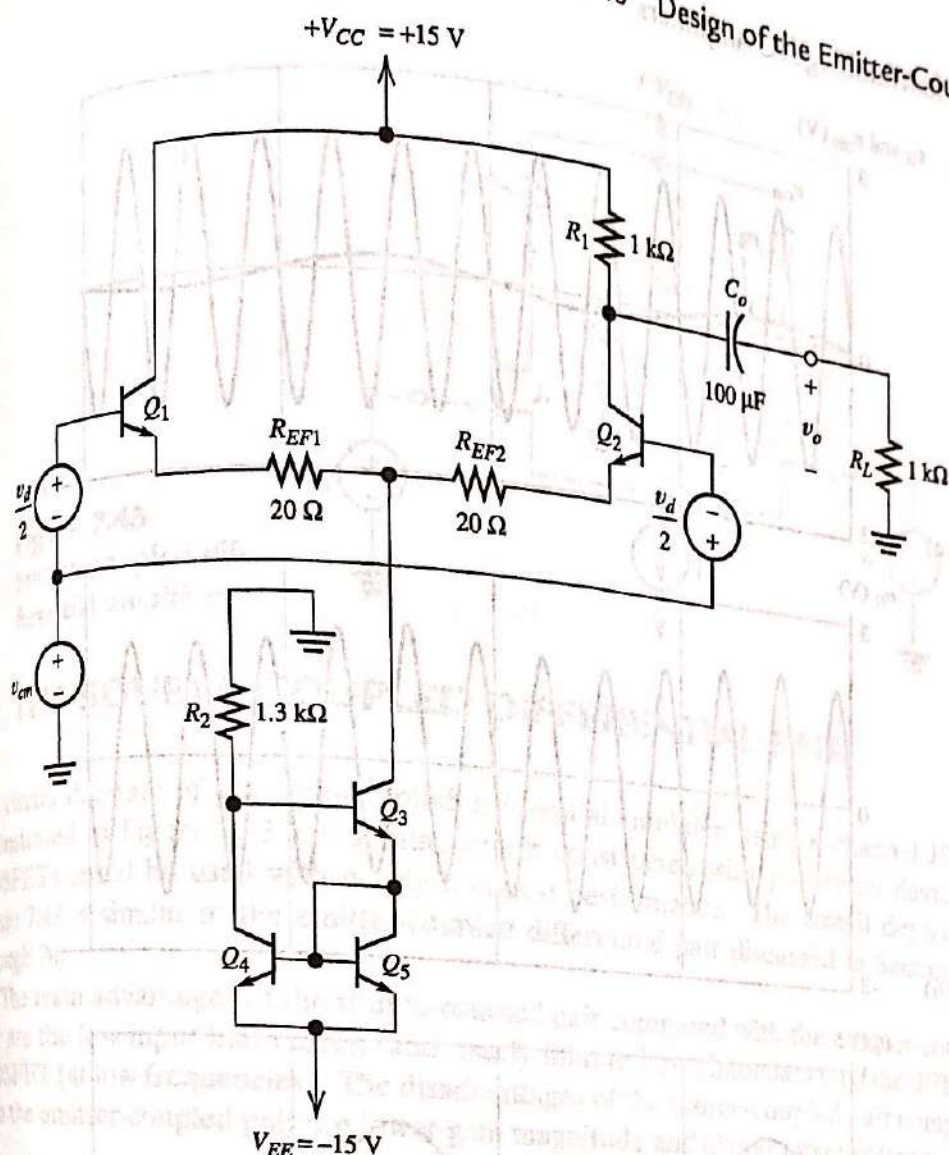


Figure 7.41 Differential amplifier of Example 7.4.

Of course, these results are for nominal-value components with a simple model for the transistors. Using a model for the transistors that includes typical device capacitances (for example, the 2N2222A model) shows that the CMRR declines rapidly above about 10 kHz, but there is no difficulty realizing the desired performance in the band of interest (i.e., 1 Hz to 1 kHz).

In the transient analysis, we selected an input signal that consists of a 0.2-V-peak 10-Hz differential signal and a 2-V-peak 60-Hz common-mode signal. These signals are shown in Figure 7.42a. The input signal at the base of Q_1 is the sum of the common-mode signal and half of the differential signal. This is illustrated in Figure 7.42b. The input voltage at the base of Q_2 is similar, except for the phase of the differential component. The output voltage is shown in Figure 7.42c. Notice that the differential signal has been amplified and the common-mode signal has been eliminated. Of course, this is exactly what we want the differential amplifier to do. $\square$

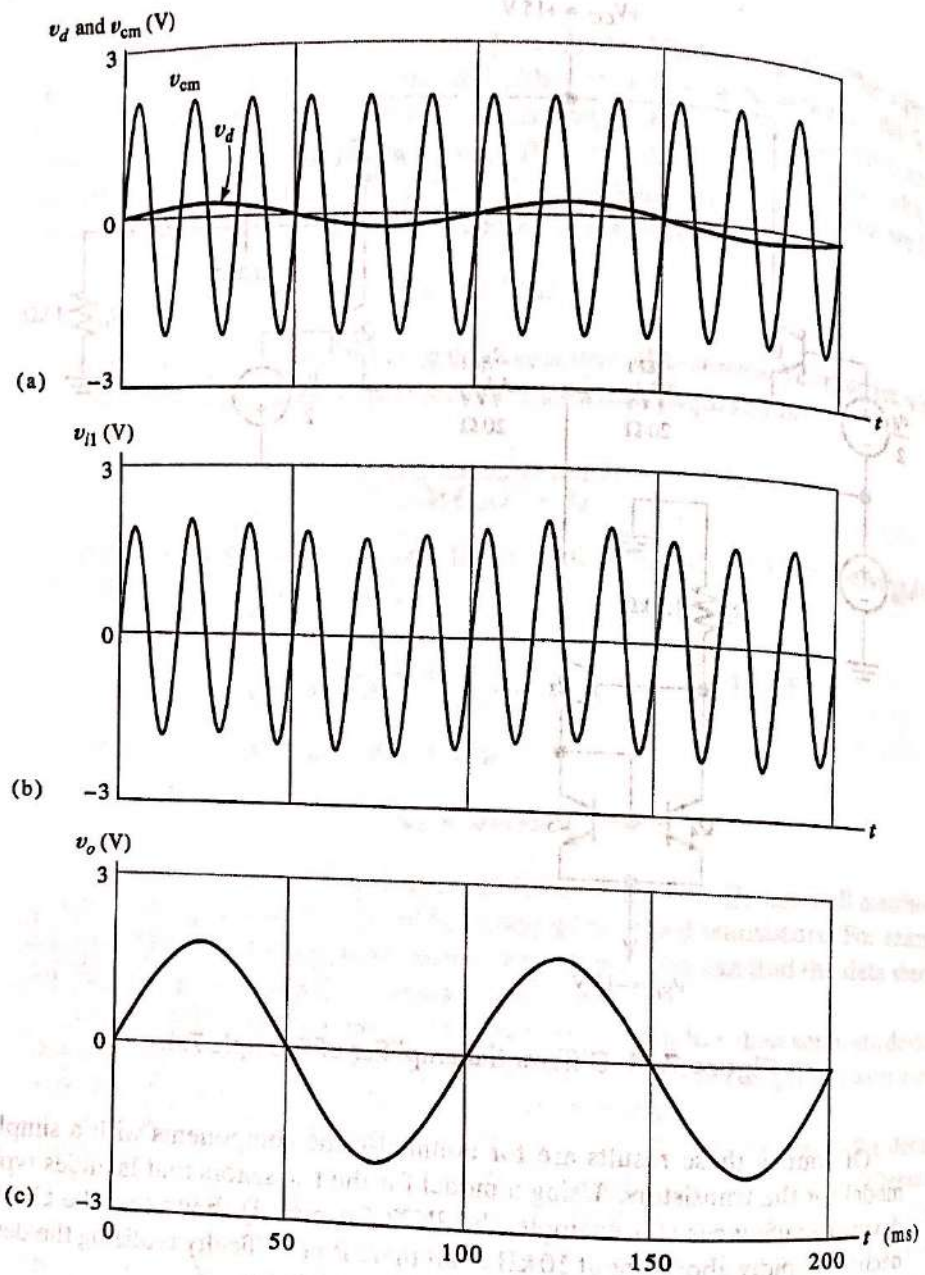


Figure 7.42 Waveforms for the differential amplifier of Example 7.4.

EXERCISE

7.14 Use SPICE to verify that the differential amplifier designed in Example 7.4 meets the desired specifications.

Answer The simulation is stored in the file named Fig7.41.

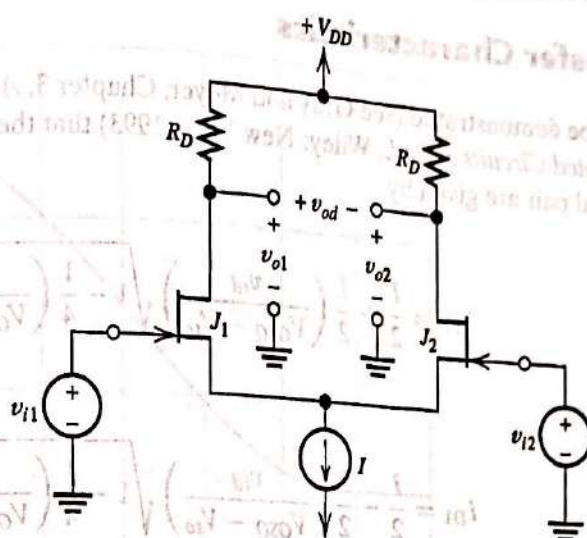


Figure 7.43
Source-coupled differential amplifier.

7.7 THE SOURCE-COUPLED DIFFERENTIAL PAIR

The circuit diagram of a source-coupled differential amplifier, using n -channel JFETs, is illustrated in Figure 7.43. A similar circuit constructed with p -channel devices or MOSFETs could be used with nearly identical performance. The circuit depicted in Figure 7.43 is similar to the emitter-coupled differential pair discussed in Sections 7.4 through 7.6.

The main advantages of the source-coupled pair compared with the emitter-coupled pair are the low input bias current and nearly infinite input impedance of the JFET or MOSFET (at low frequencies). The disadvantages of the source-coupled pair compared with the emitter-coupled pair are lower gain magnitude and higher offset voltage.

Basic Operation

Recall that the differential amplifier is intended to respond to the differential input voltage $v_{id} = v_{i1} - v_{i2}$ and to reject the common-mode input voltage $v_{i\text{cm}} = (1/2)(v_{i1} + v_{i2})$.

First, consider a pure common-mode input for which $v_{i1} = v_{i2}$. We assume that the FETs are identical. Then, due to the symmetry of the circuit (Figure 7.43), the dc bias current I splits equally between the two FETs. Thus, provided that the output impedance of the current source is infinite, so that I does not change, the currents in the FETs do not depend on the common-mode input voltage. Therefore, the output voltages are independent of the common-mode input.

The effect of a differential input voltage is to steer the majority of the bias current I through one device or the other. For example, if v_{i1} is greater than v_{i2} , a larger current flows through J_1 . For a sufficiently large differential input voltage, the entire bias current I flows through one side of the circuit.

If JFETs are used, we usually want the gate-to-channel junction to remain reverse biased for the expected range of input voltages. In order to avoid forward bias when the current is steered toward one side, we should choose $I \leq I_{DSS}$. (Recall that I_{DSS} is the drain current of a JFET in pinch-off for $v_{GS} = 0$.)

Transfer Characteristics

It can be demonstrated (see Gray and Meyer, Chapter 3, *Analysis and Design of Analog Integrated Circuits 3rd ed.*, Wiley: New York, 1993) that the drain currents in the source-coupled pair are given by

$$i_{D1} = \frac{I}{2} + \frac{I}{2} \left(\frac{v_{id}}{V_{GSQ} - V_{to}} \right) \sqrt{1 - \frac{1}{4} \left(\frac{v_{id}}{V_{GSQ} - V_{to}} \right)^2} \quad (7.71)$$

and

$$i_{D2} = \frac{I}{2} - \frac{I}{2} \left(\frac{v_{id}}{V_{GSQ} - V_{to}} \right) \sqrt{1 - \frac{1}{4} \left(\frac{v_{id}}{V_{GSQ} - V_{to}} \right)^2} \quad (7.72)$$

in which V_{GSQ} is the gate-to-source voltage at the Q -point (i.e., for $v_{id} = 0$). I is the value of the bias current, and V_{to} is the pinch-off voltage of the JFET (or the threshold voltage if MOSFETs are used). Equations (7.71) and (7.72) are valid for

$$\left| \frac{v_{id}}{V_{GSQ} - V_{to}} \right| \leq \sqrt{2}$$

Outside of this range, the currents are constant either at zero or at I . Normalized transfer characteristics are plotted in Figures 7.44 and 7.45. The corresponding transfer characteristics for the emitter-coupled circuit are displayed in

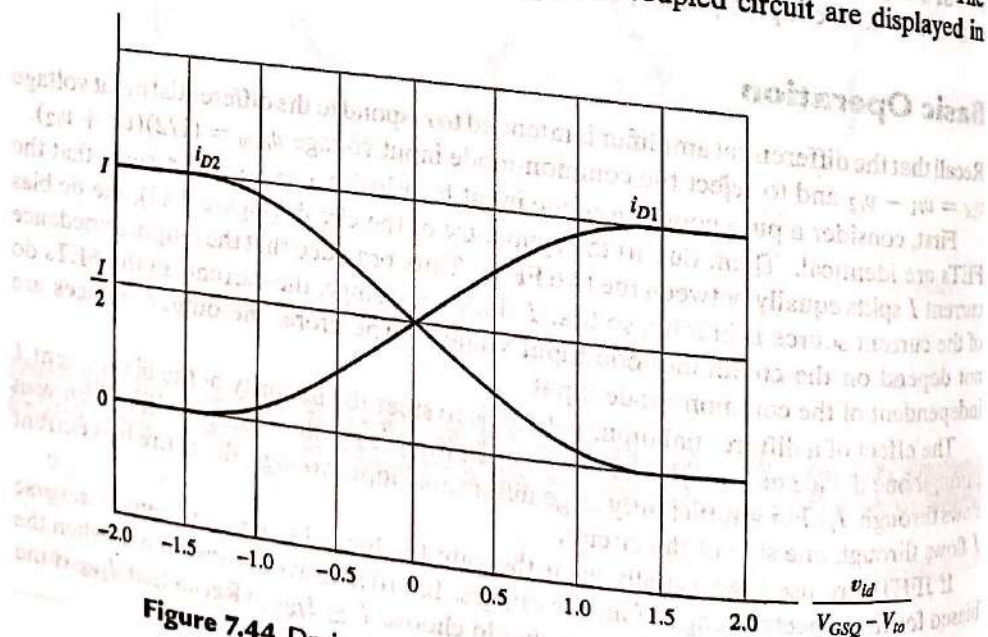


Figure 7.44 Drain currents versus normalized input voltage.

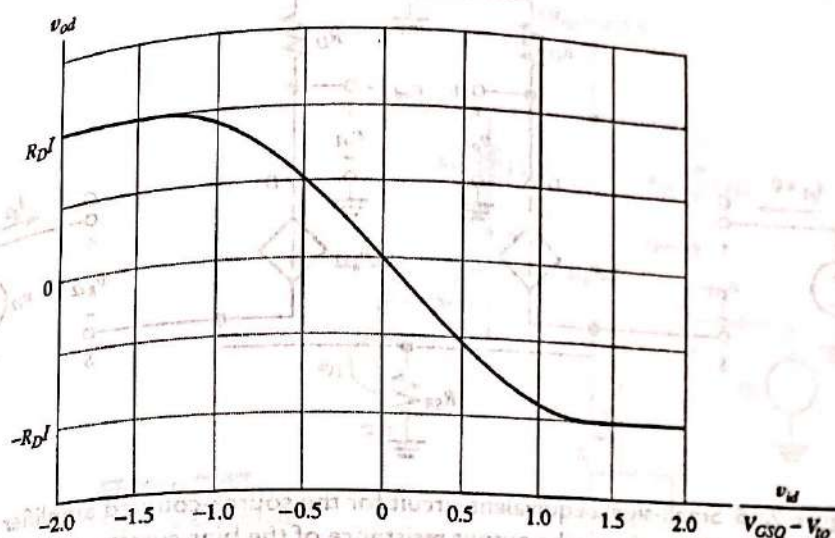


Figure 7.45 Differential output voltage versus normalized input voltage.

Figures 7.25 and 7.26. Generally, a few volts of differential input are required to completely steer the current to one side of the source-coupled pair. On the other hand, only about $4V_T \cong 100 \text{ mV}$ are required in the emitter-coupled pair.

Offset Voltage

We define the offset voltage of the differential pair to be the differential input voltage required to cause the current to split equally between the two devices. If the devices are matched, the offset voltage is zero; if the characteristics are not matched, a nonzero offset voltage occurs.

In general, the offset voltages of BJT differential amplifiers are smaller than the offset voltages of FET differential amplifiers. To attain the best matching, the devices should be fabricated on the same chip, close together. Thus, when low offset voltage is the primary concern, we should implement a differential amplifier as a BJT IC.

Small-Signal Characteristics

The small-signal equivalent circuit for the source-coupled amplifier is illustrated in Figure 7.46. Each of the FETs has been replaced by its small-signal equivalent circuit. The power-supply voltage source has been replaced by a short circuit. The resistance R_{SS} represents the output impedance of the bias current source.

The source-coupled circuit can be analyzed for differential and common-mode input signals in a manner parallel to the analysis of the emitter-coupled circuit given in Section 7.5. The results of this analysis are summarized in Table 7.3.

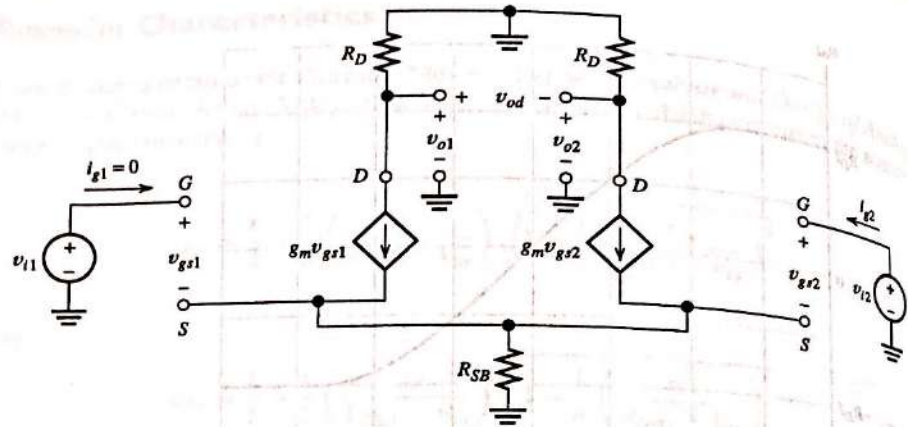


Figure 7.46 Small-signal equivalent circuit for the source-coupled amplifier of Figure 7.43. (Note: R_{SB} is the output resistance of the bias current source I .)

Table 7.3. Formulas for Input Impedance, Voltage Gain, and Output Impedance of the Source-Coupled Pair.

Input Resistance	$R_{id} = \frac{v_{id}}{i_{g1}} = \infty$ $R_{icm} = \frac{v_{icm}}{i_{g1} + i_{g2}} = \infty$
Voltage Gains for Single-Ended Output	$A_{vds} = \frac{v_{o1}}{v_{id}} = \frac{-g_m R_D}{2}$ (output taken from J_1) or $A_{vds} = \frac{v_{o2}}{v_{id}} = \frac{+g_m R_D}{2}$ (output taken from J_2) $A_{vcm} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = \frac{-g_m R_D}{1 + 2g_m R_{SB}}$
Voltage Gains for Balanced Output	$A_{vdb} = \frac{v_{od}}{v_{id}} = -g_m R_D$ $A_{vcm} = \frac{v_{ocm}}{v_{icm}} = \frac{-g_m R_D}{1 + 2g_m R_{SB}}$
Output Impedance for Single-Ended Output	$R_{os} = R_D$
Output Impedance for Balanced Output	$R_{ob} = 2R_D$
CMRR for Single-Ended Output	$CMRR_s = \left \frac{A_{vds}}{A_{vcm}} \right = \frac{1}{2} + g_m R_{SB}$
CMRR for Balanced Output	$CMRR_b = \left \frac{A_{vdb}}{A_{vcm}} \right = 1 + 2g_m R_{SB}$

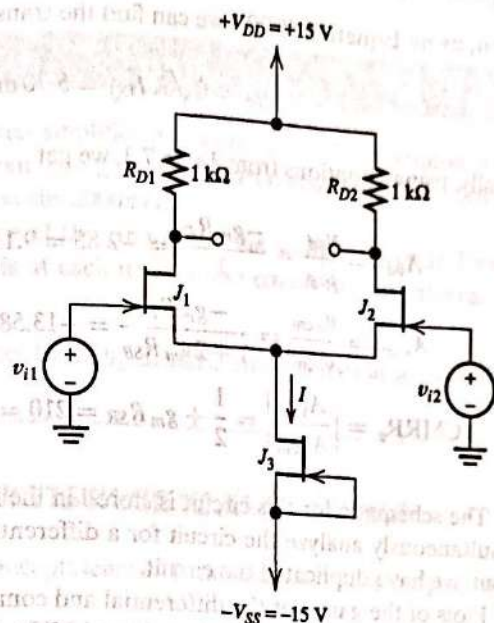


Figure 7.47
Source-coupled
differential
pair of
Example 7.5.

Example 7.5 Analysis of a Source-Coupled Differential Amplifier

Consider the source-coupled differential amplifier shown in Figure 7.47. Assume that the JFETs are identical and that they can be characterized by the model statement for the 2N3819 given in the EVAL.LIB file. This device has $I_{DSS} = 12.1 \text{ mA}$, $\lambda = 2.25 \times 10^{-3}$, and $V_{to} = -3 \text{ V}$. Use the formulas given in Table 7.3 to compute the differential gain, the common-mode gain, and the CMRR for an unbalanced output taken from the drain of J_2 . Then use PSpice to obtain plots of the gains versus frequency.

SOLUTION First, we notice that J_3 acts as a current source. It is biased at $V_{GS3} = 0$ and $I = I_{DSS} = 12.1 \text{ mA}$. The output impedance of this source is given by Equation (7.18):

$$R_{SB} = r_o \cong \frac{1}{I\lambda}$$

Substituting values, we have

$$R_{SB} = 36.73 \text{ k}\Omega$$

Notice that the Q -point values of drain current for J_1 and J_2 are $I_{DQ} = I_{DSS}/2 = 6.05 \text{ mA}$. Using Equation 5.57, we obtain

$$K = \frac{I_{DSS}}{V_{to}^2} = 1.344 \times 10^{-3}$$

Then, using Equation (5.29), we can find the transconductance of J_1 and J_2 :

$$g_m = 2\sqrt{K I_{DQ}} = 5.70 \text{ mS}$$

Finally, using equations from Table 7.3, we get

$$A_{vds} = \frac{v_{od}}{v_{id}} = \frac{-g_m R_D}{2} = -2.85 = 9.1 \text{ dB}$$

$$A_{vcm} = \frac{v_{ocm}}{v_{icm}} = \frac{-g_m R_D}{1 + 2g_m R_{SB}} = -13.58 \times 10^{-3} = -37.3 \text{ dB}$$

$$\text{CMRR}_s = \left| \frac{A_{vds}}{A_{vcm}} \right| = \frac{1}{2} + g_m R_{SB} = 210 = 46.4 \text{ dB}$$

The schematic for this circuit is stored in the file named Fig7.47. In order to simultaneously analyze the circuit for a differential input and a common-mode input, we have duplicated the circuit.

Plots of the gains for the differential and common-mode signals are shown in Figure 7.48. For frequencies below about 1 MHz, there is good agreement between the results computed using the formulas of Table 7.3 and the SPICE results. Notice, however, that the CMRR becomes drastically smaller for frequencies above 1 MHz. This drop is due to the effects of device capacitances, which we will study in Chapter 8.

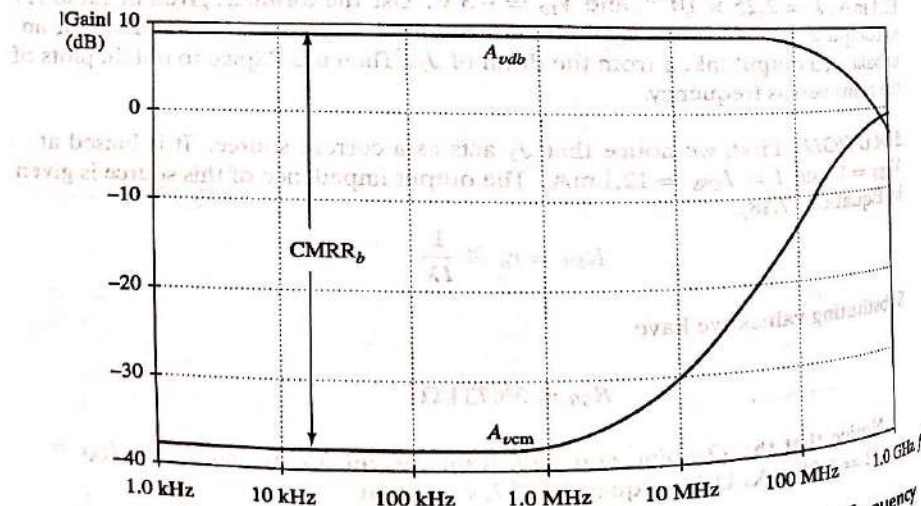


Figure 7.48 Differential and common-mode voltage gains versus frequency for the circuit of Example 7.5.

EXERCISE

7.15 Consider the differential amplifier of Example 7.5. The common-mode input signal is a 60-Hz sinusoid given by $v_{icm} = \sin(120\pi t)$, and the differential signal is a 1-kHz sinusoid given by $v_{id} = \sin(2000\pi t)$.

Based on your knowledge of the circuit and the analysis given in Example 7.5, sketch the voltage waveforms at each node in the circuit for the interval from 0 to 20 ms.

Answer Check your answers by using SPICE. The simulation is stored in the file named Exer7_15.

7.8 EXAMPLES OF MULTISTAGE IC AMPLIFIERS

Now we are ready to apply the concepts learned in this chapter to the design of integrated multistage amplifiers.

A CMOS Op Amp

As a first example, we consider the CMOS op amp shown in Figure 7.49. This op amp is intended to drive high impedance loads. Its characteristics—particularly its open-loop gain—are degraded by a low impedance load. However, for high impedance loads, it has the advantage that the output voltage can swing all the way up to the positive supply voltage V_{DD} and down to the negative supply voltage $-V_{SS}$.

Another advantage of this op amp is that it can be fabricated on the same chip as CMOS logic circuits. The channel length of the transistors in digital circuits is usually less than $1\text{ }\mu\text{m}$. However, amplifier stages with higher gain can be achieved with larger devices, because their output impedances ($r_d \cong 1/(\lambda I_{DQ})$) are larger. Also, since the op amp contains relatively few devices, larger device dimensions can be used without exceeding allowable chip-area constraints. The channel lengths of all of the devices in this example are $10\text{ }\mu\text{m}$.

The op amp contains one resistor, one capacitor, five PMOS devices, and three NMOS devices. As usual in integrated circuits, most of the elements are transistors, rather than resistors or capacitors.

The PMOS transistors M_8 , M_1 , and M_2 form a dual current mirror that supplies bias currents to the amplifier stages. The resistor R_{set} is selected to yield the desired reference current I_{set} for the current mirrors. When the circuit is operating, the source-to-drain voltage of M_8 is approximately 1.6 V. Thus, the following approximate relationship applies:

$$I_{set} \cong \frac{V_{DD} + V_{SS} - 1.6\text{ V}}{R_{set}} \quad (7.73)$$

For the values shown in Figure 7.49, this equation yields $I_{set} \cong 200\text{ }\mu\text{A}$. The currents in a MOSFET current mirror are related by Equation (7.20). Because the width of M_1 is twice the width of M_8 , the drain current of M_1 is approximately twice the value of

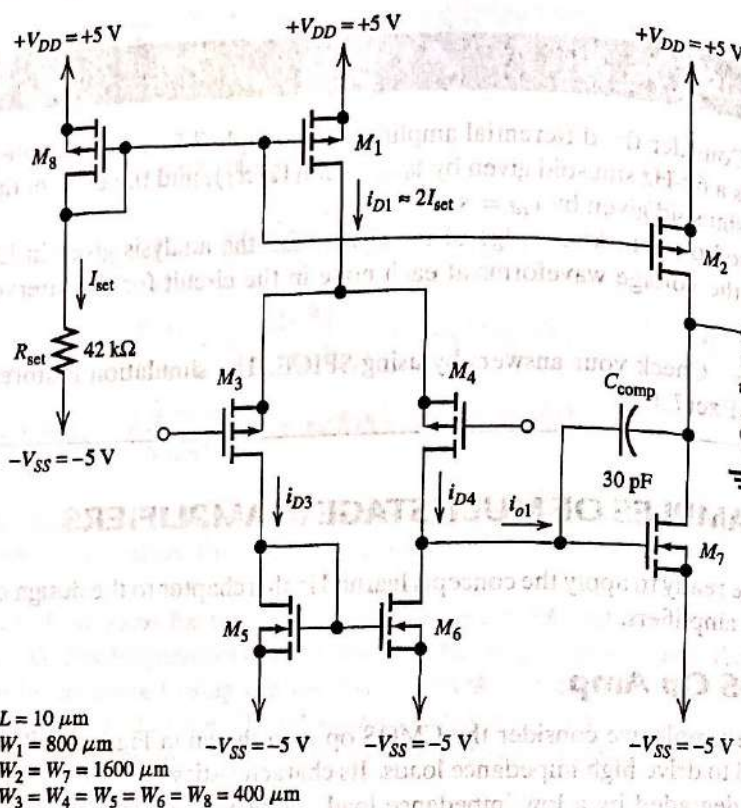


Figure 7.49 CMOS op amp.

I_{set} . Similarly, the width of M_2 is four times the width of M_8 , and therefore, the current available from M_2 is four times the value of I_{set} .

The input stage consists of transistors M_3 and M_4 , which form a source-coupled differential pair. (The source terminals of the PMOS devices are at the top ends of the PMOS symbols.) With zero input voltages at the gates of M_3 and M_4 , the current supplied by M_1 divides equally between M_3 and M_4 . Hence, the Q -point currents of M_3 and M_4 are approximately equal to I_{set} .

Transistors M_5 and M_6 form a current-mirror load for the input stage. This circuit is very similar to the BJT current-mirror active load of Figure 7.30. Thus, the output current of the first stage is

$$i_{o1} = i_{D4} - i_{D3} \quad (7.74)$$

Transistor M_7 is a common-source amplifier, and M_2 is its load. Under quiescent conditions, the drain current of M_7 is four times I_{set} . (The capacitor C_{comp} provides dominant-pole compensation, so the amplifier response is stable with unity feedback. Dominant-pole compensation is discussed in Chapter 9.)

Small-Signal Midband Analysis

Next, we use manual small-signal equivalent-circuit analysis to derive an expression for the differential voltage gain of the circuit at low frequencies.

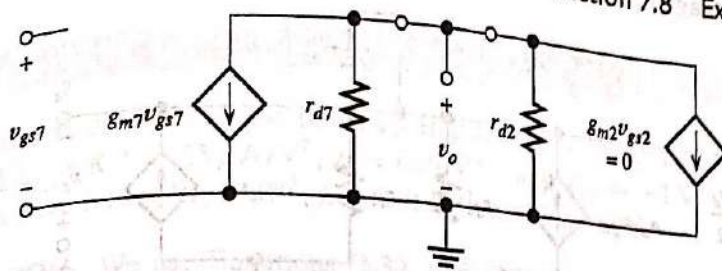


Figure 7.50 Small-signal equivalent circuit for the output stage consisting of M_7 and M_2 .

The small-signal equivalent circuit for the output stage (consisting of M_7 and its load M_2) is illustrated in Figure 7.50. Because we want to find the low-frequency gain, we have treated C_{comp} as an open circuit. Notice that we have included the drain resistance r_d in the models for the MOSFETs. Previously, we often ignored the drain resistance. However, the performance of this circuit is sensitive to the output resistance of the MOSFETs. The drain resistance is

$$r_d = \frac{1}{\lambda I_{DQ}} \quad (7.75)$$

Transistor M_2 forms the output device of a current mirror, and its gate-to-source voltage is pure dc with no signal component. In other words, we have $v_{gs2} = 0$, and the controlled source $g_{m2}v_{gs2}$ becomes an open circuit. Thus, the output voltage is

$$v_o = -g_{m7}(r_{d7} || r_{d2})v_{gs7} \quad (7.76)$$

Rearranging this equation, we find the voltage gain of the output stage:

$$A_{v2} = \frac{v_o}{v_{gs7}} = -g_{m7}(r_{d7} || r_{d2}) \quad (7.77)$$

Next, we analyze the source-coupled pair to find its differential voltage gain. The small-signal equivalent circuit is illustrated in Figure 7.51. For a pure differential input signal, the input voltages are $v_d/2$ and $-v_d/2$, as shown in the figure.

With a pure differential input, the signal voltage at the source terminals of M_3 and M_4 is zero, because the circuit is symmetrical. Therefore, we have shown the source terminals of M_3 and M_4 connected to ground in the small-signal equivalent circuit. (Connecting these source terminals to ground would not be appropriate for a common-mode signal. This is similar to the BJT differential pair examined in Section 7.5.)

Writing a current equation at the drain of M_5 , we have

$$i_{d5} = -i_{d3} \quad (7.78)$$

The currents through the resistances r_{d3} and r_{d5} are small compared with the currents in the controlled sources, so we can write

$$i_{d3} \cong g_{m3}v_{gs3} = -g_{m3}v_d/2 \quad (7.79)$$

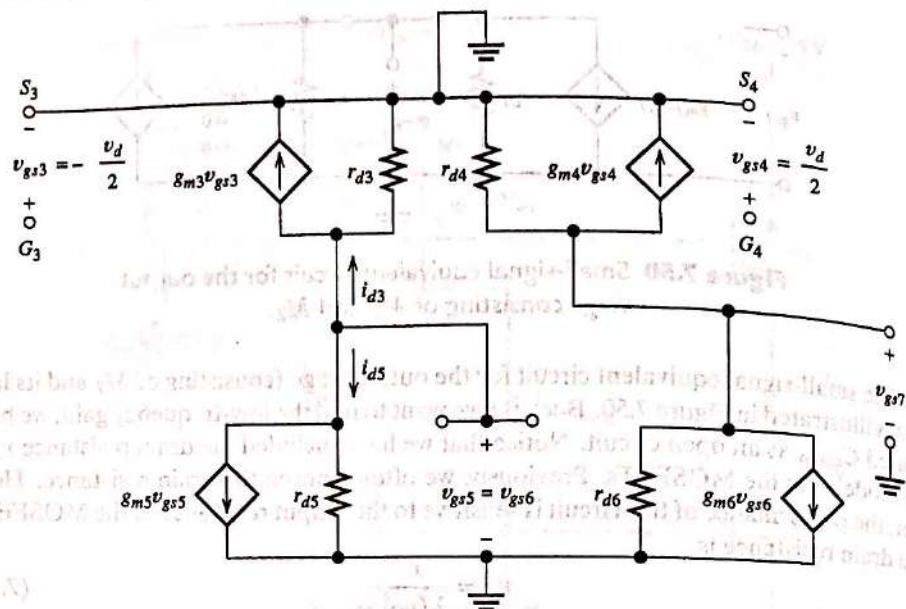


Figure 7.51 Small-signal equivalent circuit for the source-coupled input stage.

and

$$i_{d5} \cong g_{m5}v_{gs5} \quad (7.80)$$

Using Equations (7.79) and (7.80) to substitute into Equation (7.78), we obtain

$$g_{m5}v_{gs5} \cong g_{m3}v_d/2 \quad (7.81)$$

Because $v_{gs6} = v_{gs5}$ and $g_{m6} \cong g_{m5}$, we can write

$$g_{m6}v_{gs6} = g_{m5}v_{gs5} \cong g_{m3}v_d/2 \quad (7.82)$$

Notice that the resistances r_{d4} and r_{d6} are in parallel. The output voltage is

$$v_{gs7} = -(g_{m6}v_{gs6} + g_{m4}v_{gs4})(r_{d4}||r_{d6}) \quad (7.83)$$

Using the fact that $v_{gs4} = v_d/2$ and substituting Equation (7.82) into Equation (7.83), we obtain

$$v_{gs7} = -(g_{m3}\frac{v_d}{2} + g_{m4}\frac{v_d}{2})(r_{d4}||r_{d6}) \quad (7.84)$$

Because of symmetry, $g_{m3} = g_{m4}$, and we have

$$A_{v1} = \frac{v_{gs7}}{v_d} = -g_{m4}(r_{d4}||r_{d6}) \quad (7.85)$$

Finally, the overall gain of the op amp is the product of the gains of the first and second stages given by Equations (7.77) and (7.85):

$$A_v = \frac{v_o}{v_d} = A_{v1}A_{v2} \quad (7.86)$$

Example 7.6 CMOS-Op-Amp Analysis

Compute the differential gain of the op amp illustrated in Figure 7.49. The PMOS devices have $KP = 25 \mu\text{A}/\text{V}^2$, $\lambda = 0.01 \text{ V}^{-1}$, and $V_{to} = -1 \text{ V}$. The NMOS devices have $KP = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0.01 \text{ V}^{-1}$, and $V_{to} = 1 \text{ V}$.

SOLUTION We use Equations (5.30) and (7.75) to compute the required small-signal parameters:

$$g_m \cong \sqrt{2KP I_{DQ} \left(\frac{W}{L} \right)}$$

$$r_d \cong \frac{1}{\lambda I_{DQ}}$$

For M_4 , we have $I_{DQ} = I_{\text{set}} = 200 \mu\text{A}$, $W = 400 \mu\text{m}$, and $L = 10 \mu\text{m}$. Substituting values, we find $r_{d4} = 500 \text{ k}\Omega$ and $g_{m4} = 632 \mu\text{S}$. Similarly, the Q -point current of M_6 is $I_{DQ} = I_{\text{set}} = 200 \mu\text{A}$, and we have $r_{d6} = 500 \text{ k}\Omega$. Substituting values into Equation (7.85), we obtain

$$A_{v1} = -g_{m4}(r_{d4} || r_{d6}) = -632 \times 10^{-6} \times 250 \times 10^3 = -158$$

In decibels, we have

$$A_{v1} = 20 \log |A_{v1}| = 44.0 \text{ dB}$$

The Q -point currents for M_7 and M_2 are $I_{DQ} = 4 \times I_{\text{set}} = 800 \mu\text{A}$. Substituting values into the equations given for g_m and r_d yields $g_{m7} = 3577 \mu\text{S}$ and $r_{d7} = r_{d2} = 125 \text{ k}\Omega$. Substituting values into Equation (7.76) results in

$$A_{v2} = -g_{m7}(r_{d7} || r_{d2}) = -3577 \times 10^{-6} \times 62.5 \times 10^3 = -224$$

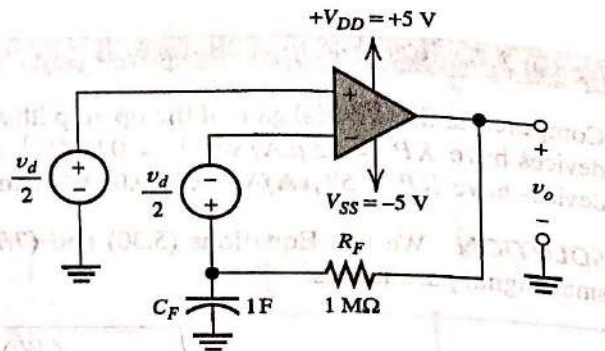
In decibels, we have $A_{v2} = 47 \text{ dB}$.

Finally, the overall differential voltage gain is

$$A_v = A_{v1} \times A_{v2} = 35392 = 91.0 \text{ dB}$$

Next, we use PSpice to plot the gains versus frequency. In order to display the open-loop gain, the op amp must be properly biased. This is accomplished by the use of the circuit shown in Figure 7.52. The feedback network consisting of the resistor R_F and capacitor C_F ensure that the op amp is biased in the active region. However, the feedback through the R_F - C_F network is negligible for ac signals above about 1 Hz. Therefore, above 1 Hz, the circuit gain is the same as the open-loop gain. In the simulation, we choose $C_F = 1 \text{ F}$. Of course, in actual laboratory measurements, we would use a more practical value, such as $100 \mu\text{F}$.

Figure 7.52
Test circuit
for open-loop gain.
The internal
circuit for
the op amp
is shown in
Figure 7.49.



The schematic is stored in the file named Fig7_52. After the simulation was run, Probe was used to plot A_{v1} , A_{v2} , and A_v against frequency, as shown in Figure 7.53. At low frequencies, the gain values agree very well with our manual calculations. The gains drop at higher frequencies due to the compensation capacitor. Notice that the overall gain is similar to Figure 2.25.

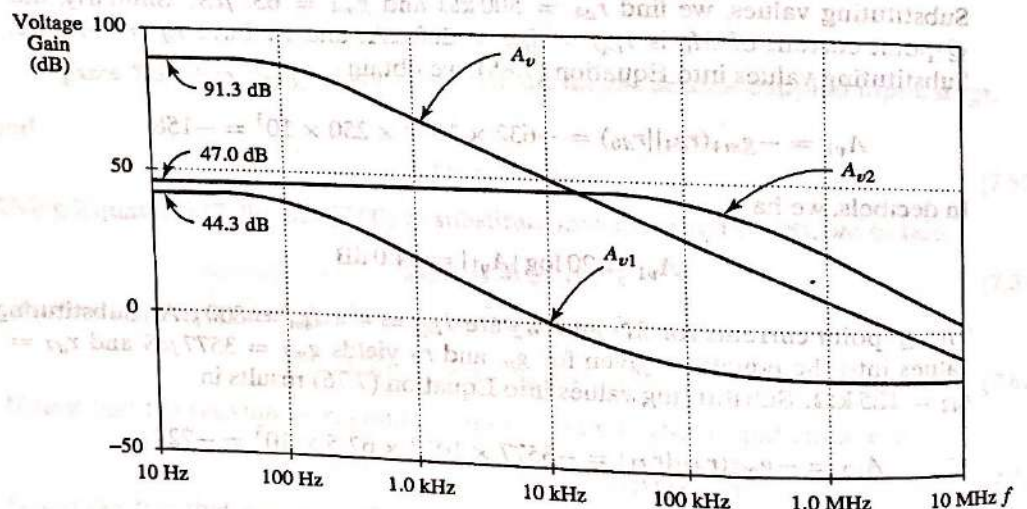
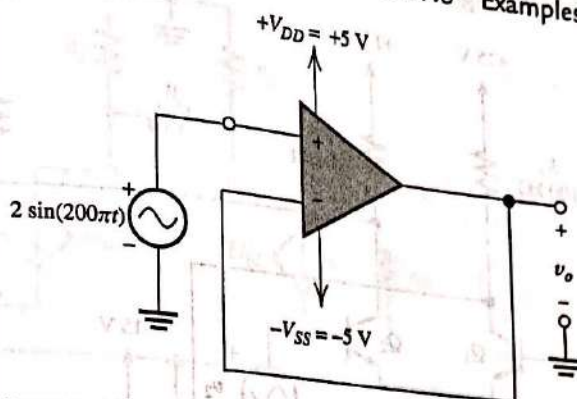


Figure 7.53 Open-loop gain versus frequency for the CMOS op amp.

EXERCISE

7.16 Consider the circuit of Figure 7.54. The internal circuit diagram of the op amp is shown in Figure 7.49, except that the value of R_{set} is changed to $7.6 \text{ k}\Omega$ for this exercise. The circuit is configured as a unity-gain noninverting amplifier (or voltage follower). Thus, $v_o \cong v_{in}$.

Figure 7.54
Unity-gain buffer
amplifier of Ex-
ercise 7.16.



- For $R_{\text{set}} = 7.6 \text{ k}\Omega$, it turns out that $I_{\text{set}} \cong 1 \text{ mA}$. Use manual analysis to find the approximate Q -point drain current of each transistor in the op amp.
- Use SPICE to check your answers from part (a). In case of gross discrepancy, find and correct the error.
- Manually sketch the voltage against time at each node in the circuit, including the interior nodes of the op amp. Use information that you have learned about the circuit in Example 7.6 and in parts (a) and (b) of this exercise to help in formulating the sketches.
- Use a SPICE transient analysis to obtain plots of the voltage waveforms, and check your sketches from part (c). If necessary, revise your thinking about the circuit until your predictions approximately match the simulated waveforms.

Answer

- $I_{DQ8} = I_{\text{set}} = 1 \text{ mA}$, $I_{DQ1} \cong 2 \text{ mA}$, $I_{DQ2} = I_{DQ7} = 4 \text{ mA}$, $I_{DQ3} = I_{DQ4} = I_{DQ5} = I_{DQ6} = 1 \text{ mA}$.
- The schematic is stored in the file named Exer7_16, and it gives results that are in good agreement with the answers to part (a).
- and (d) Use the simulation to observe the waveforms.

A BJT Op Amp

Figure 7.55 shows a BJT op amp that uses many of the circuits we have discussed in this chapter, plus some from Chapter 4. The input sources are v_1 and v_2 , and the output is v_o . In the following exercises, you have an opportunity to apply what we have discussed to a realistic IC.

EXERCISE

- 7.17** List the functions of each of the BJTs shown in Figure 7.55.

Answer Q_1 and Q_2 form a differential amplifier with a balanced output. Q_3 and Q_4 form a differential amplifier with a single-ended output. Q_5 is a *pnp* common-emitter amplifier with unbypassed emitter resistance. Q_6 is an emitter follower. Q_7 , Q_8 , and Q_9 form a double current mirror.

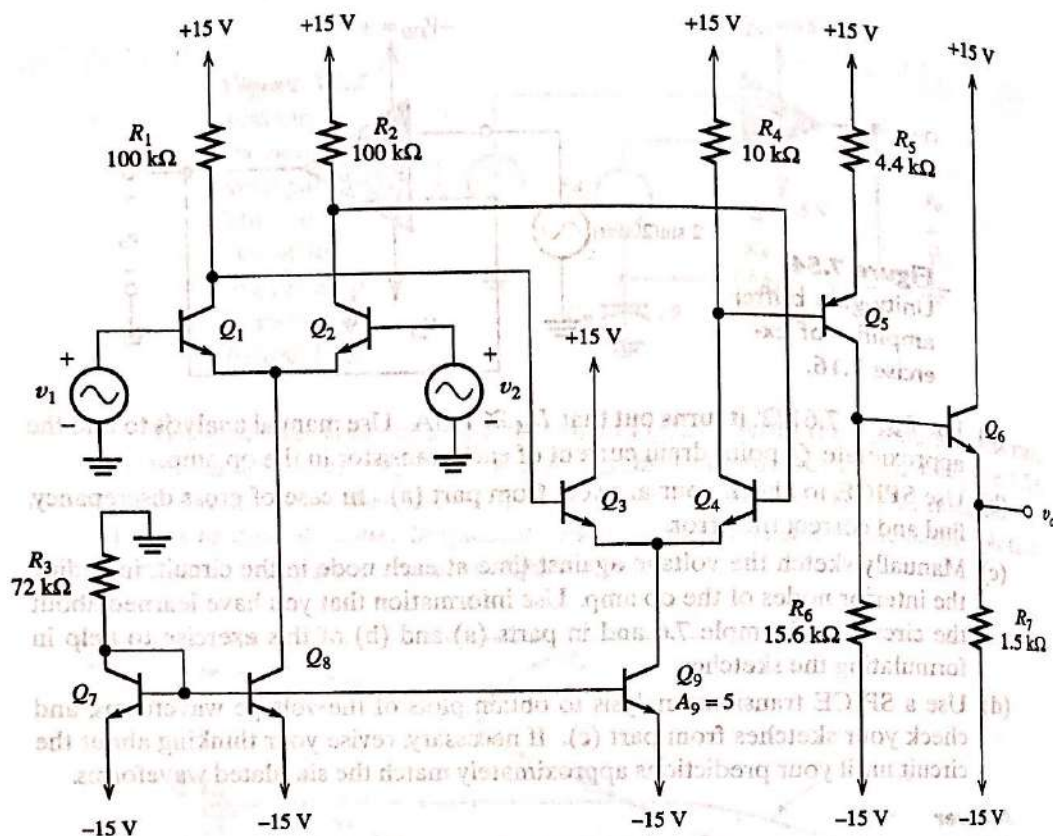


Figure 7.55 A BJT op amp.

EXERCISE

7.18 The relative areas of the transistors are all unity, except for Q_9 , which has a relative area of 5. Assume that the transistors are matched (except for the larger area of Q_9), that the input voltages v_1 and v_2 are zero, that the base currents can be neglected, and that $V_{BEQ} \cong 0.6$ V for all transistors. Determine the Q -point collector currents for all of the transistors, and find the output voltage v_o .

Answer $I_{CQ1} = I_{CQ2} = 0.1$ mA, $I_{CQ3} = I_{CQ4} = 0.5$ mA, $I_{CQ5} = 1$ mA, $I_{CQ6} = 10$ mA, $I_{CQ7} = 0.2$ mA, $I_{CQ8} = 0.2$ mA, $I_{CQ9} = 1$ mA, and $v_o = 0$. Notice that the bias currents become larger as we move from the input toward the output, which is typical in amplifiers. Also, for zero input voltages, the output voltage is zero, which is a desirable characteristic for an op amp.

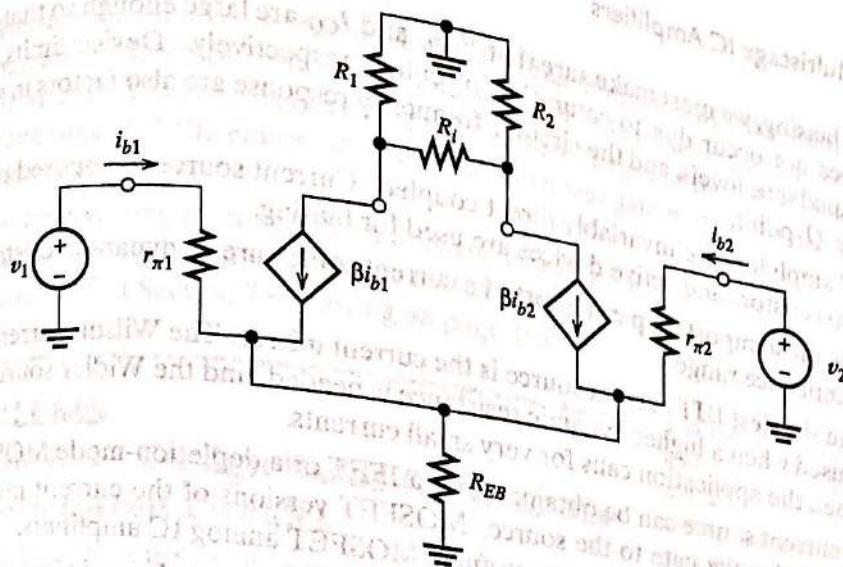


Figure 7.56 Equivalent circuit for the first stage of Figure 7.52. R_{EB} represents the output impedance of current sink Q_8 . $R_i = r_{\pi 3} + r_{\pi 4}$ is the differential input impedance of the second stage.

EXERCISE

- 7.19** (a) Assuming that $\beta = 200$ for all transistors, and using the bias currents obtained in Exercise 7.18, determine r_{π} for transistors Q_1 through Q_6 . (b) Determine the differential input impedance of the second differential amplifier (Q_3 and Q_4). (c) Draw the small-signal equivalent circuit for the first differential amplifier, including the input impedance of the second stage. Use the r_{π} - β model for the transistors. (d) Assume that the input is a pure differential signal (i.e., $v_1 = v_{id}/2$ and $v_2 = -v_{id}/2$). Determine the differential voltage gain magnitude of the first stage. The gain is the differential output voltage divided by the differential input voltage. (Hint: Because the circuit is symmetrical, we can divide the circuit in half by grounding the top end of R_{EB} and the midpoint of R_i .)

Answer (a) $r_{\pi 1} = r_{\pi 2} = 52 \text{ k}\Omega$, $r_{\pi 3} = r_{\pi 4} = 10.4 \text{ k}\Omega$, $r_{\pi 5} = 5.2 \text{ k}\Omega$, and $r_{\pi 6} = 520 \Omega$; (b) $R_{i2} = r_{\pi 3} + r_{\pi 4} = 20.8 \text{ k}\Omega$; (c) See Figure 7.56; (d) $A_{vdb1} = 31.2 \text{ dB}$.

SUMMARY

- The variety of devices available to the IC designer is limited by the complexity of the fabrication process and the need to minimize chip area. Active device characteristics are tailored to a given application by the selection of device dimensions. Resistors and capacitors are avoided if possible. Inductors are not practical in integrated circuits.
- The design of IC amplifiers heavily exploits device matching.

- In biasing, we must make sure that V_{CEQ} and I_{CQ} are large enough so that clipping does not occur due to saturation or cutoff, respectively. Device limits, desired impedance levels, and the circuit's frequency response are also factors in selecting the Q -point.
- IC amplifiers are invariably direct coupled. Current sources composed of one or two resistors and active devices are used for biasing.
- The most important parameters of a current source are its dynamic resistance and compliance range.
- The simplest BJT current source is the current mirror. The Wilson current source is used when a higher dynamic resistance is needed, and the Widlar source is best when the application calls for very small currents.
- A current source can be obtained with a JFET or a depletion-mode MOSFET by connecting the gate to the source. MOSFET versions of the current mirror and the Wilson current source are useful in MOSFET analog IC amplifiers.
- A simple BJT differential amplifier and its waveforms are shown in Figure 7.23 on page 435. The circuit does not respond to the common-mode component of the input signal. The differential signal steers the current partly toward one side of the circuit or the other, resulting in an amplified signal at the output.
- Figure 7.26 on page 439 shows the large-signal transfer characteristic for the BJT differential amplifier. For $|v_{id}| \leq V_T$, the transfer characteristic is approximately straight, so that amplification occurs without appreciable distortion. For $|v_{id}| \geq 5V_T$, the output voltage is nearly constant.
- The BJT differential amplifier large-signal transfer characteristic becomes linear over a greater range if resistances are added in series with the emitters.
- Either a single-ended or a differential output can be taken from the differential pair, as shown in Figure 7.29 on page 440.
- The current mirror is a more practical load than resistors are for differential pairs in integrated circuits.
- It is convenient to use half-circuits in the analysis of the differential pair.
- Assuming matched devices, the differential pair produces a pure common-mode output in response to the common-mode input component; however, if any components are mismatched, a differential output component can arise from the common-mode input component.
- For good performance in rejecting the common-mode signal, it is important for the devices to be matched, for R_{EB} to have a large value (i.e., the I_{EE} current source should be as nearly ideal as possible), and for R_{EF} to have a small value.
- Many useful results for the emitter-coupled pair are given in Table 7.2 on page 450.
- Suggestions for attaining high input impedance, a high common-mode rejection ratio, and low distortion in the design of emitter-coupled pairs are listed in Section 7.6, starting on page 450.
- The source-coupled pair is an important differential amplifier circuit that can be constructed with either JFETs or MOSFETs.

- The main advantages of the source-coupled pair compared with the emitter-coupled pair are the low input bias current and nearly infinite input impedance of the JFET or MOSFET (at low frequencies). The disadvantages of the source-coupled pair compared with the emitter-coupled pair are lower gain magnitude and higher offset voltage.
- A wide variety of integrated multistage amplifiers can be designed by using the circuits examined in this chapter and in Chapters 4 and 5. Several op amps were discussed in Section 7.8, starting on page 465.

PROBLEMS

Section 7.1: Design Rules for Discrete and Integrated Circuits

- 7.1. Briefly contrast the circuit components available in ICs with those in discrete circuits.
- 7.2. List and briefly discuss the factors that limit the types of components available in ICs.
- 7.3. What advantage do transistors in an IC have compared with discrete transistors?
- 7.4. Ideally, two BJTs, Q_1 and Q_2 , in a certain IC should be exactly matched. Suppose that, due to process variations, the emitter area of Q_1 is 5% larger than that of Q_2 . Determine the difference between V_{BE1} and V_{BE2} needed to attain $I_C = 1$ mA in both transistors. (Hint: The scale current I_s of a BJT is proportional to its emitter area.)
- 7.5. Certain resistors in an IC have a nominal value of 10 k Ω . Due to process variations, the resistors on a given chip have average values that are 20% higher than nominal. However, the resistances on the chip match to within $\pm 2\%$. Determine the highest and lowest values for the resistances on the chip.
- 7.6. Process variations cause the W/L ratios of nominally identical NMOS transistors on a given IC chip to vary by $\pm 5\%$. Suppose that V_{GSQ} , V_{to} , and KP are the same for both transistors. By what percentage does I_{DQ} vary for these transistors?

Section 7.2: IC Biasing with BJTs

- 7.7. List several factors that should be considered in selecting the Q -point for a BJT in an amplifier circuit.
- 7.8. Draw the circuit diagrams of the current mirror, the Widlar current source, and the Wilson current source. Which of these circuits is preferable for extremely small currents? Which is used to achieve a high-impedance current source?
- 7.9. Contrast the term "current sink" with the term "current source."
- D7.10. **Current sink design.** Design a current mirror to function as a 0.5-mA current sink. Assume that matched nnp transistors

and matched pnp transistors having $\beta = 100$, $I_s = 10^{-14}$ A, and $V_A = 50$ V are available. The available supply voltages are ± 15 V. The current should be nearly constant for output voltage ranging from -5 V to $+5$ V. Use SPICE to plot the sink current versus voltage, and find the output impedance of the sink. For a current sink use nnp transistors. To attain the desired compliance range, the emitters of the transistors need to be connected to the negative supply voltage. Consider grounding the upper end of the resistor so a smaller value can be used.

D7.11. **Current source design.** Repeat Problem D7.10 for a current source (rather than a current sink). For a current source use pnp transistors. To attain the desired compliance range, the emitters of the transistors need to be connected to the positive supply voltage. Consider grounding the lower end of the resistor so a smaller value can be used.

D7.12. **Wilson sink design.** Repeat Problem D7.10 for a Wilson sink. Assume $V_A = \infty$ in the initial design. Then simulate the circuit and adjust the values if necessary to attain the desired performance.

D7.13. **Integrated bias circuit design.** In a certain IC, a 1-mA sink, a 0.1-mA sink, and a 5-mA source are required for biasing purposes. Design a circuit (similar to Figure 7.12) to provide these currents if matched nnp transistors and matched pnp transistors with $\beta = 100$, $I_s = 10^{-14}$ A, and $V_A = 50$ V are available. The area multipliers of the transistors are allowed to range from 1 to 5. The available supply voltages are ± 15 V. The currents should be nearly constant for output voltages ranging from -10 V to $+10$ V. Use SPICE to verify your design. Look carefully at Figure 7.12 to gain ideas for this design. Assume $V_A = \infty$ in the initial design. Then simulate the circuit and adjust component values if necessary to attain the desired performance.

D7.14. **Integrated bias circuit design.** Repeat Problem D7.13 if the currents are a 10- μ A sink, a 1-mA sink, a 50- μ A source, and a 5-mA source.

7.15. Find expressions for I_{C3} and I_{C4} in terms of V_{CC} , β , and R_{ref} for the circuit illustrated in Figure P7.15. Assume that all of the transistors are matched and that $V_{BEQ} \cong 0.6$ V.

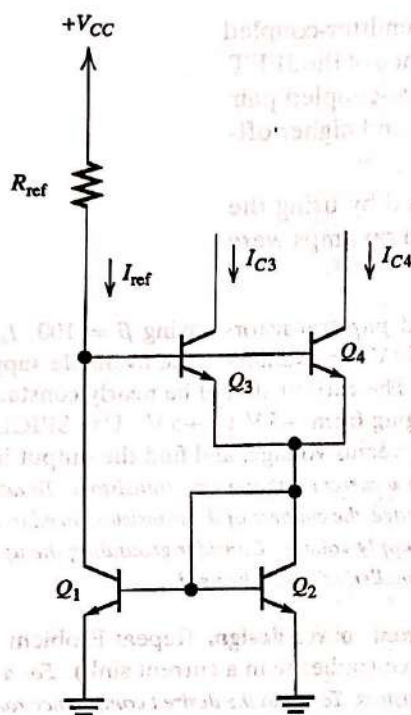


Figure P7.15

7.16. Repeat Problem 7.15, assuming that the area of Q_4 is double that of the other transistors.

D7.17. Widlar sink design. Design a $50\text{-}\mu\text{A}$ Widlar current sink. Assume that matched npn transistors and matched pnp transistors with $\beta = 100$, $I_s = 10^{-14}\text{ A}$, and $V_A = 50\text{ V}$ are available. The available supply voltages are $\pm 15\text{ V}$. The current should be nearly constant for output voltage ranging from -5 V to $+5\text{ V}$. Use SPICE to plot the sink current versus voltage, and find the output impedance of the sink. Select a reasonable value for I_{ref} . Then compute the resistance values needed in the circuit. Finally simulate the circuit and, if necessary, make slight adjustments in the resistance values to attain the desired current.

D7.18. Widlar source design. Repeat Problem D7.17 for a current source. Design a circuit using pnp transistors.

D7.19. IC design. Using the circuit shown in Figure 7.3, design a direct-coupled buffer amplifier suitable for integrated-circuit implementation. Use current mirrors for the current sources. The load resistance is $R_L = 50\text{ }\Omega$. Use pnp and npn transistors that have $\beta = 200$, $I_s = 10^{-14}\text{ A}$, $V_A = 50\text{ V}$, and $|V_{BEQ}| \cong 0.6\text{ V}$. The area multiplier is allowed to range from 1 to 5. An undistorted output signal voltage of 500 mV peak is required. Design for high input impedance and low power-supply drain. The power-supply voltages are $V_{CC} = 5$ and $-V_{EE} = -5\text{ V}$. The source impedance is $R_s = 1\text{ k}\Omega$.

- Draw the detailed circuit diagram, showing values for the resistors and the area multipliers for each transistor.
- Analyze your design using PSpice. Determine the output offset voltage for $v_s = 0$. Compute the peak output current and be sure to provide sufficient bias current in the output stage so that clipping due to cut-off does not occur. Bias the input stage at a lower value of current. Choose a smaller area for the input BJT than for the output BJT so the V_{BEQ} values are equal in magnitude, ensuring that the offset is zero.

7.20. Consider the current mirror shown in Figure 7.1 with $V_{CC} = 15\text{ V}$, $R = 10\text{ k}\Omega$, and $V_{BE} = 0.6\text{ V}$. Suppose that $V_A = \infty$, and the areas of the transistors are equal. If β decreases from 200 to 100 for both transistors, by what percentage does I_{C2} increase?

7.21. Consider the current mirror illustrated in Figure 7.1 with $V_{CC} = 15\text{ V}$, $R = 10\text{ k}\Omega$, and $V_{BE} = 0.6\text{ V}$. Suppose that $V_A = \infty$, $\beta = 100$ for both transistors, the relative area of Q_1 is $A_1 = 1$, and the relative area of Q_2 is $A_2 = 1 \pm 5\%$. By what maximum percentage can I_{C2} vary from circuit to circuit?

7.22. Sometimes we need a current source for which the current is independent of V_{BE} (Because V_{BE} varies with temperature). (a) Derive an expression for the current I_{C2} for the circuit of Figure P7.22, and show that it is independent of V_{BE} . Assume that all transistors are identical, that V_{BE} is the same for all transistors, and that the base currents are negligible. (b) Simulate the circuit for $R_1 = 5\text{ k}\Omega$, $V_{CC} = 15\text{ V}$, and $V_O = 10\text{ V}$. Sweep temperature from 0 to 100°C , and plot I_O versus temperature. (c) Design and simulate a 1.5-mA current mirror.

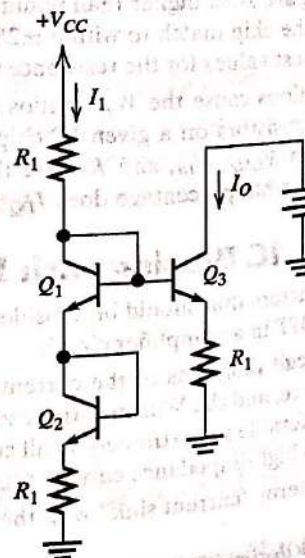


Figure P7.22

7.23. Consider the current source of Figure P7.22 with $R_1 = 5 \text{ k}\Omega$ and $V_{CC} = 15 \text{ V}$. Determine the approximate compliance range of the circuit.

7.24. Consider the current source shown in Figure P7.24.

- Derive an expression for I_{C3} in terms of V_{BE} , β , R_1 , and V_{CC} , assuming that all of the transistors are operating in the active region and have the same value of V_{BE} . Neglect the Early effect (i.e., assume that $V_A = \infty$).
- If $V_{BEQ} = 0.7 \text{ V}$, $R_1 = 30 \text{ k}\Omega$, and $V_{CC} = 15 \text{ V}$, by what percentage does I_{C3} change when β changes from 100 to 110?
- Repeat part (b) for the current mirror of Figure 7.1a, and compare the results with those of part (b). Comment.
- For the values given in part (b), determine the compliance range for the circuit of Figure P7.24.

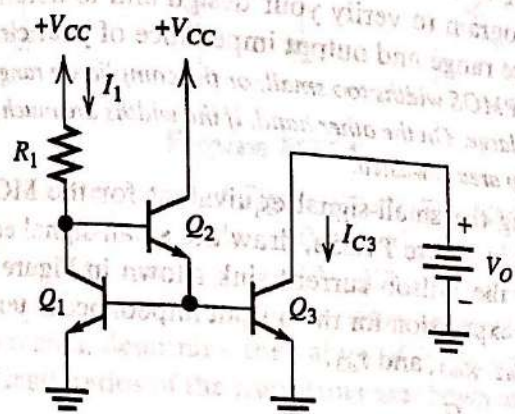


Figure P7.24

7.25. Determine the collector currents of all of the transistors and the value of V_o in Figure P7.25. Assume that the transistors have equal areas and are matched. Furthermore, assume that $|V_{BE}| = 0.7 \text{ V}$, $V_A = \infty$, and the base currents can be neglected.

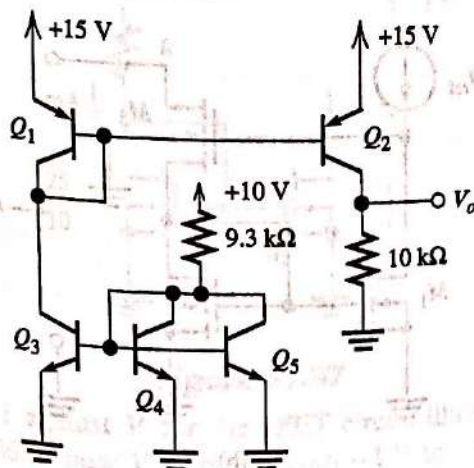


Figure P7.25

7.26. Determine the collector currents of all of the transistors and the value of V_o in Figure P7.26. Assume that the transistors are matched, except that the relative area of Q_4 is double that of the other transistors. Assume also that $|V_{BE}| = 0.7 \text{ V}$, $V_A = \infty$, and the base currents can be neglected. In what region (cutoff, saturation, or active) is each transistor operating?

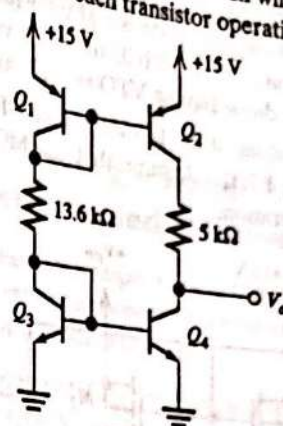


Figure P7.26

7.27. Figure P7.27 shows a circuit known as a cascode current source. Assume that the transistors are matched and have $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, and $V_A = \infty$. Sketch I_o against V_o to approximate scale. Label the compliance range. Check your answer by using SPICE. For the simulation, use the parameters $\text{BF} = 100$, $\text{VAF} = 50 \text{ V}$, and $\text{IS} = 10^{-14} \text{ A}$.

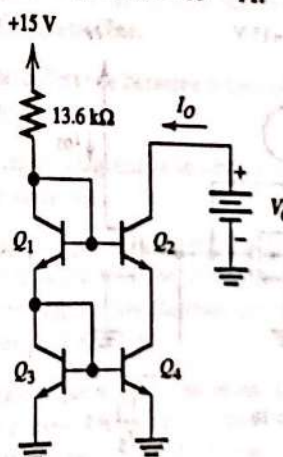


Figure P7.27 Cascode current source.

7.28. Design a simple 1-mA current mirror using $V_{CC} = 15 \text{ V}$ and matched transistors with $V_A = 100 \text{ V}$, $\beta = 100$, and $I_s = 10^{-14} \text{ A}$. Then, simulate the mirror and the cascode current source of Figure P7.27 by using SPICE. Obtain plots of the output resistance versus voltage for both the simple mirror and the cascode current source. Which has the higher output resistance?

Section 7.3: IC Biasing with FETs

7.29. Draw the circuit diagrams of a current mirror and of a Wilson current sink using n -channel enhancement MOSFETs. In general, which circuit has the largest compliance range? The largest output impedance?

7.30. A constant-current diode is a JFET with the gate connected to the source. Use SPICE to plot I versus V for a constant-current diode having $V_{TO} = -1$ V and $\beta = 10^{-3}$.

7.31. Find the values of the labeled currents for the circuits shown in Figure P7.31. Assume that the MOSFETs are operating in saturation.

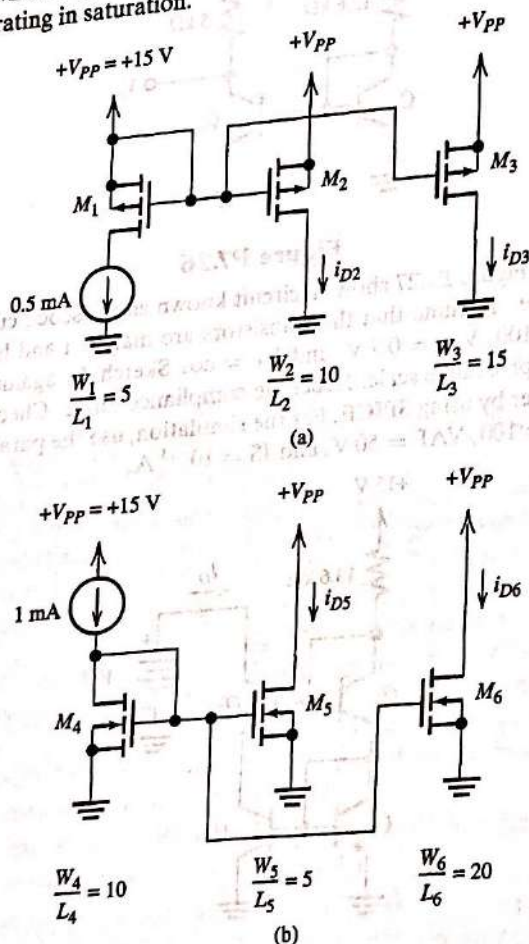


Figure P7.31

D7.32. NMOS current-mirror design. Design a current mirror to provide a current sink of 0.5 mA with a compliance range from 3 V to 15 V. A single resistor of 50 k Ω is to be used. The power-supply voltage is +15 V. Use enhancement NMOS devices with $K_P = 50 \mu\text{A}/\text{V}^2$, $V_{TO} = 1$ V, $\text{LAMBDA} = 0.02$, and a channel length of 5 μm . (The design consists of the circuit

diagram and the width of each MOSFET.) Use SPICE to verify your design and to determine the compliance range and output impedance of your circuit. Don't choose the NMOS widths too small, or the compliance range will not be sufficiently large. On the other hand, if the widths are much greater than needed, chip area is wasted.

D7.33. High-impedance current sink design. Using the devices specified in Problem D7.32, design a 0.5-mA current sink that has an output impedance of at least 500 k Ω and a compliance range from 5 V to 15 V. Use SPICE to verify your design. Consider using a Wilson source to attain the high output impedance required.

D7.34. PMOS current-mirror design. Design a current mirror to provide a current source (rather than a sink) of 0.5 mA to provide a current range from 0 V to 12 V. A single resistor with a compliance range from 0 V to 12 V. The power-supply voltage is +15 V. of 50 k Ω is to be used. The power-supply voltage is +15 V. Use PMOS devices with $K_P = 25 \mu\text{A}/\text{V}^2$, $V_{TO} = -1$ V, $\text{LAMBDA} = 0.02$, and a channel length of 5 μm . Write a SPICE program to verify your design and to determine the compliance range and output impedance of your circuit. Don't choose the PMOS widths too small, or the compliance range will not be sufficiently large. On the other hand, if the widths are much greater than needed, chip area is wasted.

7.35. Using the small-signal equivalent for the MOSFET illustrated in Figure P7.35a, draw the small-signal equivalent circuit for the Wilson current sink shown in Figure P7.35b. Derive an expression for the output impedance in terms of g_{m1} , r_{d1} , g_{m2} , r_{d2} , g_{m3} , and r_{d3} .

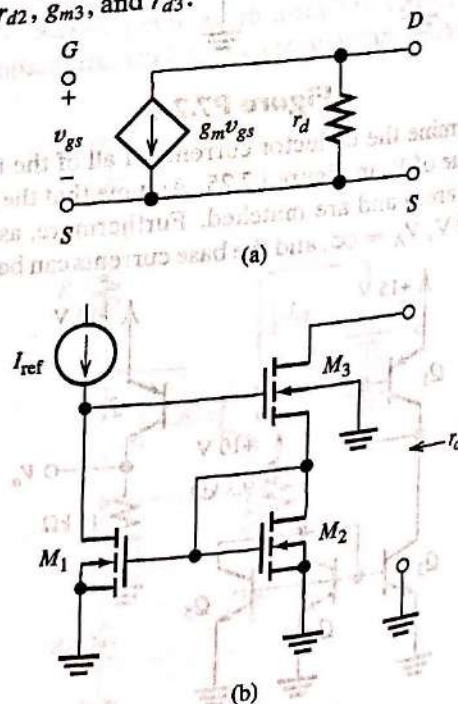


Figure P7.35

7.36. Consider the circuit illustrated in Figure P7.36. The transistors have $V_{to} = 1\text{ V}$, $KP = 50\text{ }\mu\text{A/V}^2$, and $\lambda = 0$. Assuming that all of the transistors are operating in the saturation region, determine the values of R , I_2 , and I_3 . The width-to-length ratios of the transistors are shown in the figure.

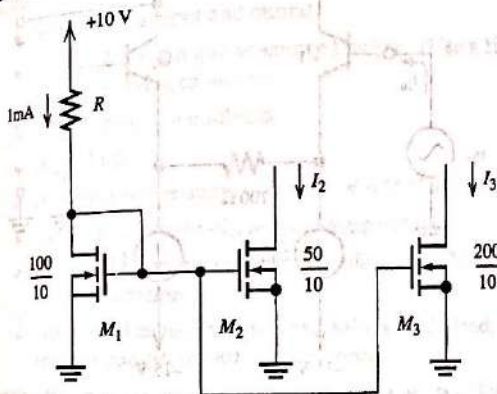


Figure P7.36

7.37. Consider the circuit of Figure P7.37. The NMOS transistors have $V_{ton} = 1\text{ V}$, $KP_n = 50\text{ }\mu\text{A/V}^2$, and $\lambda_n = 0$. The PMOS transistors have $V_{top} = -1\text{ V}$, $KP_p = 25\text{ }\mu\text{A/V}^2$, and $\lambda_p = 0$. Assuming that all of the transistors are operating in the saturation region, determine the values of R , I_3 , and I_4 . The width-to-length ratios of the transistors are shown in the figure.

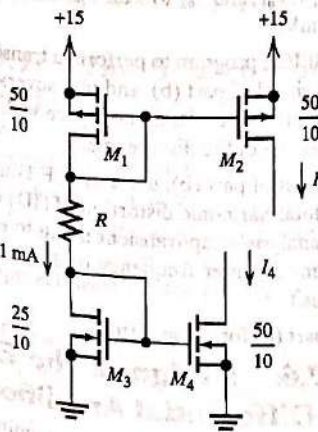


Figure P7.37

7.38. Plot I against V for the JFET circuit illustrated in Figure P7.36. Allow V to range from -1 V to 10 V . The parameters of the transistor are $I_{DSS} = 4\text{ mA}$, $V_{to} = -2\text{ V}$, and $\lambda = 0.01$.

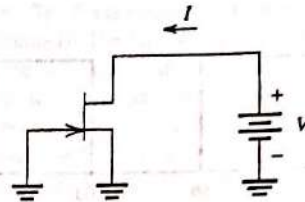


Figure P7.38

Section 7.4: Large-Signal Analysis of the Emitter-Coupled Differential Pair

7.39. Ideally, what is the response of a differential amplifier to the common-mode component of the input signal? To the differential-mode component?

7.40. For what range of differential input voltage is the BJT differential pair approximately linear?

7.41. Sketch to scale the transfer characteristic (i.e., the differential output voltage versus the differential input voltage) of the emitter-coupled differential amplifier of Figure 7.22. Assume that $V_{CC} = 10\text{ V}$, $I_{EE} = 2\text{ mA}$, $R_C = 1\text{ k}\Omega$, and $V_T = 25\text{ mV}$.

7.42. The differential input voltage of the amplifier shown in Figure 7.22 is $v_{id} = 1\sin(2000\pi t)$. Assume that $V_{CC} = 10\text{ V}$, $I_{EE} = 2\text{ mA}$, and $R_C = 1\text{ k}\Omega$. Sketch the differential output signal v_{od} to scale against time.

7.43. Explain the difference between a balanced output and a single-ended output.

7.44. Draw the circuit diagram of an emitter-coupled pair with a current mirror as its load.

7.45. Consider the emitter-coupled pair shown in Figure 7.22. Find the value of the differential input voltage required to cause 90% of the current I_{EE} to flow through Q_1 . Repeat for 99%. Assume a temperature of 300 K.

D7.46. Sine-wave-to-square-wave converter. Design an emitter-coupled pair to convert a 10-kHz, 2-V-peak sinusoid into a square wave with voltage levels of 0 V and 5 V. The ideal output waveform is illustrated in Figure P7.46. The load is a 5-k Ω resistor having one end grounded. The available power-supply voltages are 15 V and -15 V. Use SPICE to verify your design. Assume that both *npn* and *pnp* BJTs with $I_s = 10^{-14}\text{ A}$, $\beta = 200$, and $V_A = 100\text{ V}$ are available. Consider the circuit configuration of Figure 7.37 with the coupling capacitor replaced with a short circuit. Choose the resistor values so that $V_o = +5\text{ V}$ when Q_1 is cutoff and so that $V_o = 0\text{ V}$ when Q_1 is cutoff.

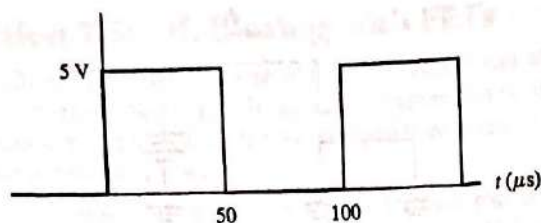


Figure P7.46

D7.47. Sinewave-to-square-wave converter. Repeat Problem D7.46 if the voltage levels of the output are changed to 0 V and -10 V. Consider a circuit configuration like that of Figure 7.37 but implemented with pnp BJTs and with a short circuit in place of the capacitor.

Section 7.5: Small-Signal Equivalent-Circuit Analysis of the Emitter-Coupled Differential Pair

7.48. With what is an ideal dc voltage source replaced in a small-signal equivalent circuit? Why? Repeat for an ideal current source.

7.49. Find the small-signal voltage gain and input resistance of the amplifier depicted in Figure P7.49. Assume that $\beta = 200$.

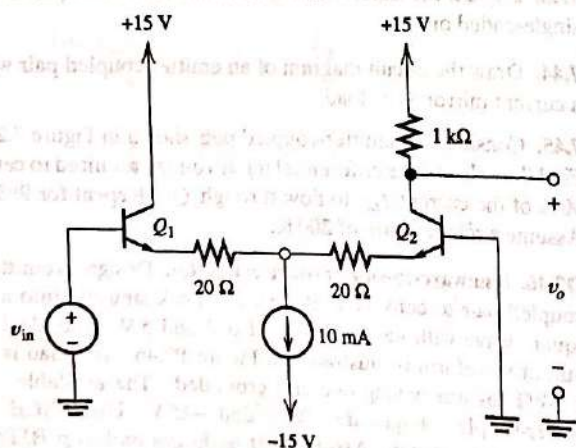


Figure P7.49

7.50. Find the small-signal voltage gain and input resistance of the amplifier shown in Figure P7.50. Assume that $\beta = 200$.

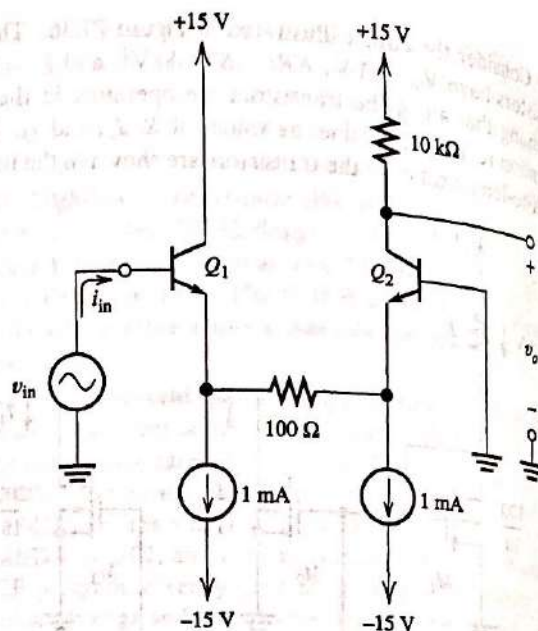


Figure P7.50

7.51. Consider the emitter-coupled pair illustrated in Figure 7.22. The transistors have $I_s = 10^{-13}$ A and $\beta = 200$. Assume that $I_{EE} = 10$ mA, $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and $R_C = 1$ k Ω .

- Compute the voltage gain v_{o2}/v_{id} .
- Suppose that $v_{i1} = V_m \sin(2000\pi t)$ and $v_{i2} = 0$. Sketch v_{i1} , i_{C1} , i_{C2} , v_{o1} , and v_{o2} to scale against time. Assume that $V_m = 10$ mV.
- Write a SPICE program to perform a transient analysis for the input signal of part (b), and plot several cycles of each waveform. If the results do not agree with your sketches, find the source of the disagreement.
- For the input of part (b), use a SPICE Fourier analysis to find the total harmonic distortion (THD) of v_{o2} . (Hint: Use the analysis/setup/transient menu to enable Fourier analysis for a center frequency of 1000 Hz and nine harmonics.)
- Repeat part (d) for $V_m = 50$ mV.

Section 7.6: Design of the Emitter-Coupled Differential Amplifier

7.52. List the factors in the design of an emitter-coupled differential amplifier that are important for obtaining a large CMRR.

7.53. List the factors in the design of an emitter-coupled differential amplifier that are important for obtaining a large input impedance.

7.54. List the factors in the design of an emitter-coupled differential amplifier that are important for obtaining low distortion.

D7.55. Differential-amplifier design. Design an emitter-coupled pair differential amplifier having the following specifications:

- Single-ended input and output.
- Dc-coupled input and ac-coupled output. (Use a $10\text{-}\mu\text{F}$ output coupling capacitor.)
- $A_v \cong -25$ in the midband.
- $R_L = 1\text{ k}\Omega$.
- Available power-supply voltages of $+15\text{ V}$ and -15 V .
- Circuit suitable for discrete implementation.
- Maximum output amplitude capability of 0.1 V without severe distortion.
- Number of capacitors and their values minimized, in a manner consistent with good practice.

Assume that matched transistors having the same model as the 2N2222A are available. Use SPICE to verify your design and to obtain a plot of gain versus frequency. This circuit can consist of two 2N2222A BJTs and some resistors. The configuration can be similar to Figure 7.39 except that the output must be taken from the collector of Q_1 to achieve an inverting amplifier.

D7.56. Common-emitter amplifier design. Repeat Problem D7.55, using a common-emitter amplifier configuration. Use a $1000\text{-}\mu\text{F}$ emitter bypass capacitor. Insert a small unbypassed resistance in series with the emitter to adjust the gain to the desired value.

Section 7.7: The Source-Coupled Differential Pair

7.57. What are the advantages of the source-coupled differential amplifier compared with the emitter-coupled differential amplifier? What are disadvantages?

7.58. Starting from the equivalent circuit illustrated in Figure 7.46, derive an expression for $A_{v_{cm}} = v_{o1}/v_{i_{cm}}$. (Hint: Follow the approach used for the emitter-coupled pair in Section 7.5.)

7.59. Repeat Problem 7.58 for $A_{v_{ds}} = v_{o1}/v_{i_d}$.

D7.60. Source-coupled amplifier design. Design a source-coupled differential pair amplifier with a CMRR of at least 70 dB at a frequency of 60 Hz . The active devices that are available are matched n -channel JFETs with $I_{DSS} = 5\text{ mA}$, $V_{to} = -2\text{ V}$, and $\lambda = 0.02$. In addition, matched $n\text{pn}$ BJTs with $\beta = 200$, $I_s = 10^{-14}\text{ A}$, and $V_A = 100\text{ V}$ may be used. Resistors and capacitors of any value may also be used. The available power-supply voltages are $V_{DD} = +15\text{ V}$ and

$-V_{SS} = -15\text{ V}$. The $5\text{-k}\Omega$ resistive load is single ended (i.e., one end is grounded). The inputs can be dc coupled, but the output should be ac coupled with a $100\text{-}\mu\text{F}$ capacitor. Use a SPICE program to demonstrate that your design meets all of the desired specifications. There are many solutions to this problem. To attain the desired CMRR, a high-impedance current source may be needed. Consider using a Wilson BJT current source to bias the JFET pair.

D7.61. Source-coupled amplifier design. Repeat Problem D7.60, using FETs exclusively. In addition to the n -channel JFETs, matched p -channel JFETs with $I_{DSS} = 4\text{ mA}$, $V_{to} = 1\text{ V}$, and $\lambda = 0.02$ can be used. Consider cascading two BJT differential stages as illustrated in Figure 7.29a with BJTs. Biasing is easier to achieve if one stage is an n -channel and the other is a p -channel. In the model statement for the p -channel device, specify $V_{TO} = -1\text{ V}$. SPICE assumes that V_{TO} is negative for depletion devices and positive for enhancement devices. Of course, all JFETs are depletion devices.

Section 7.8: Examples of Multistage IC Amplifiers

7.62. Look at the op-amp circuit shown in Figure 7.49. Which of the input terminals (the gate of M_3 or the gate of M_4) is the inverting input?

7.63. Repeat Example 7.6 with a $1\text{-k}\Omega$ load resistance connected from the output terminal of the op amp to ground. Assume that the transistor bias points do not change when the load resistance is connected. Notice that the open-loop gain is reduced significantly when the load resistance is connected.

7.64. Look at the op-amp circuit shown in Figure 7.55. Which of the input terminals (the base of Q_1 or the base of Q_2) is the inverting input?

7.65. Determine the open-loop differential voltage gain of the op amp illustrated in Figure 7.55. Make use of the assumptions and results of Exercises 7.17, 7.18, and 7.19.

7.66. Consider the op amp shown in Figure 7.55. Suppose that the input voltages are zero. Use the assumptions and results of Exercises 7.17, 7.18, and 7.19. Determine the voltages at the collectors of Q_1 and Q_2 , at the collector of Q_4 , at the collector of Q_5 , and finally, at the output. Ideally, the output voltage should be zero for zero input voltages. In an $n\text{pn}$ differential amplifier or common-emitter amplifier, the voltage is higher at the output than at the input. Why do you think that the designer included the $p\text{np}$ stage (Q_5) in this op amp?

7.67. After working problems 7.65 and 7.66, consider the circuit of Figure 7.54 with the op amp of Figure 7.55. (Hint: The base of Q_2 is the inverting input terminal.) Sketch the voltage, including both the dc and ac components at each input, at the emitter of Q_1 , at the collector of Q_4 , at the collector of Q_5 , and at the output. Finally, use SPICE to check your answers.

7.68. Use SPICE to determine the open-loop voltage gain for the op amp depicted in Figure 7.55. Assume that $\beta = 200$ and that $I_s = 10^{-14}$ A. Assume the default value for V_A (which is ∞). Repeat for $V_A = 50$ V. Compare the results.

7.69. Consider the op amp illustrated in Figure P7.69. Which of the input terminals (the base of Q_1 or the base of Q_2) is the inverting input? Which is the noninverting input?

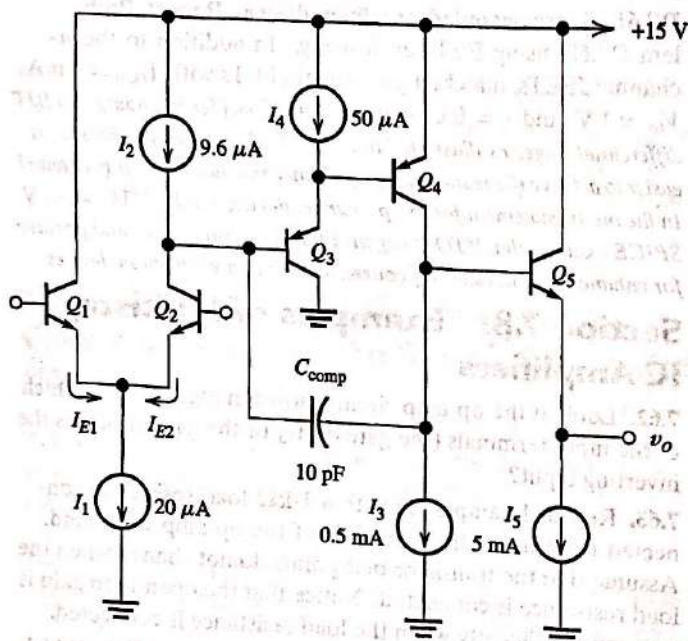


Figure P7.69 An integrated-circuit amplifier.

7.70. List the function (emitter-coupled pair, emitter follower, common-emitter amplifier, etc.) of each of the BJTs in Figure P7.69. Ignore the capacitor.

D7.71. Integrated bias circuit design. Design the current sources (I_1 through I_5) for the op amp shown in Figure P7.69. Assume that matched transistors are available, that the relative areas can range from 1 to 10, and that $\beta = 200$, $|V_{BEQ}| \cong 0.6$ V, and $I_s = 10^{-14}$ A. Use SPICE to verify your design. Look at Figure 7.12 to get some ideas for the bias-circuit design.

7.72. Draw the small-signal equivalent circuit for each stage of the op amp shown in Figure P7.69, including a $1\text{-k}\Omega$ resistance connected from output to ground. Ignore the capacitor, and use the r_π - β model for the transistors with $\beta = 200$. Assume that the current sources are ideal. (a) Determine the input resistance seen looking into the base of Q_5 and the voltage gain for Q_5 . (b) Determine the input resistance and voltage gain of Q_4 . (c) Determine the input resistance and voltage gain of Q_3 . (d) Determine the differential voltage gain of the differential pair formed by Q_1 and Q_2 . (e) Finally, determine the differential voltage gain of the op amp.

7.73. Determine the value of the input bias current for the op amp shown in Figure P7.69. Assume that $\beta = 200$ for all transistors.

7.74. Determine the value of the input bias current for the op amp illustrated in Figure 7.55. Assume that $\beta = 200$ for all transistors.

7.75. With the transistors matched, the offset voltage of the op amp shown in Figure 7.55 is zero. Assuming that all of the other transistors are matched, determine the ratio of relative areas for Q_1 and Q_2 that results in an input offset voltage of 2 mV.

Frequency Response

In this chapter, we consider the frequency response of various amplifier configurations, such as the common-source, the common-emitter, and the differential pair. We will see that the high-frequency equivalent circuits of FETs and BJTs contain capacitances that reduce gain in the high-frequency region. In discrete amplifiers, coupling and bypass capacitors cause gain to fall off at low frequencies.

We begin the chapter with a discussion of Bode plots. Using Bode-plot techniques, we can readily plot gain against frequency for many amplifier configurations. Furthermore, the terminology associated with Bode plots permeates electrical-engineering literature.

8

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8.1 BODE PLOTS

In this section, we consider the frequency response of some RC circuits that appear frequently in amplifiers. Our objective is to show how circuit functions can be quickly and easily plotted against frequency—at least for simple circuits. These plots are known as **Bode plots**.

Motivation

There are several reasons that we might want to plot the magnitude and phase of a circuit function. We can consider a signal to consist of a summation of sinusoidal components. Audio signals contain components ranging from about 20 Hz to 20 kHz. Electrocardiograms range from 0.05 Hz to about 100 Hz, and video signals range from dc to 4.5 MHz. In order to amplify a signal without distortion, the amplifier gain magnitude must be the same for all of the frequency components. If we have a plot of the gain magnitude versus frequency, we can see whether or not the gain is constant for all of the frequency components contained in the signal of interest.

Another application for Bode plots is in designing feedback amplifiers. In Chapter 9, we show that partial feedback of the output signal to the input terminals can be very useful. Oscillation (the spontaneous generation of signals) is a problem that can occur in amplifiers with feedback. Bode plots of the amplifier gain magnitude and phase shift versus frequency are very useful in avoiding unwanted oscillations.

Use of the Laplace Transform Variable

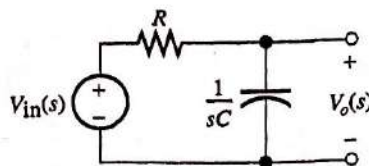
In our discussion, we use the Laplace transform variable s . Actually, we don't make much use of Laplace transform theory, but we use the notation and some of the terminology of Laplace transforms, so you will be able to relate this discussion to material you have studied or will study in other courses. Eventually, we substitute $s = j\omega$. If you haven't studied the Laplace transform, for now you can consider s to be simply a shorthand notation for $j\omega$. Thus, in the analysis of circuits, a capacitor is replaced by an impedance $1/sC$, and an inductor, L , is replaced by an impedance sL . Resistors have impedances equal to their resistances.

An Example: The Lowpass RC Circuit

As a first example, we consider the voltage transfer function of the circuit displayed in Figure 8.1. By applying the voltage-divider principle, we can find the ratio of the output voltage to the input voltage:

$$A_v(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1/sC}{R + 1/sC} \quad (8.1)$$

Figure 8.1
Low-pass RC filter.



Multiplying the numerator and denominator by sC , we obtain

$$A_v(s) = \frac{1}{RCs + 1} \quad (8.2)$$

Network functions for lumped linear time-invariant circuits can always be expressed as a ratio of polynomials in s . In this case, the numerator is simply a constant, and the denominator is a first-order polynomial. In more complex circuits, the numerator and denominator can both be high-order polynomials.

Poles and Zeroes

The values of s that cause the denominator polynomial to become zero are called **poles** of the network function. The magnitude of the network function is unbounded at the poles. The values of s that cause the numerator to become zero are called **zeroes** of the network function. Thus, the poles are roots of the denominator polynomial, and the zeroes are roots of the numerator polynomial. For example, the voltage transfer ratio given in Equation (8.2) has a pole at $s = -1/RC$, but no zeroes. (Sometimes we say that it has a zero at $s = \infty$, because the transfer function goes to zero as s approaches infinity.)

Break Frequencies

In the sinusoidal steady-state analysis of a network, we use $j2\pi f$ in place of the Laplace transform variable s . If we substitute $j2\pi f$ into Equation (8.2), we have

$$A_v(f) = \frac{1}{1 + j2\pi RCf} \quad (8.3)$$

This is a complex quantity that gives the magnitude and phase of the voltage transfer ratio as a function of frequency. For example, if we evaluate the equation for $f = 1/2\pi RC$, we obtain

$$A_v(f) = \frac{1}{1 + j1} = 0.707 \angle -45^\circ \quad (8.4)$$

The meaning of this result is that, if we apply a sinusoid of frequency $f = 1/2\pi RC$ to the input, the output will have an amplitude that is 0.707 times the input amplitude. Furthermore, the output will be phase shifted by -45° with respect to the input.

It is convenient to express Equation (8.3) as

$$A_v(f) = \frac{V_o}{V_{in}} = \frac{1}{1 + j(f/f_b)} \quad (8.5)$$

where

$$f_b = \frac{1}{2\pi RC} \quad (8.6)$$

is called the **break frequency**. Alternative names for f_b are the **corner frequency**, **half-power frequency**, and **3-dB frequency**.

Network functions for lumped circuits can be expressed as ratios of polynomials in the Laplace variable s . The roots of the numerator are called zeroes, and the roots of the denominator are called poles.

Gain Magnitude Expressed in Decibels

As discussed in Section 1.7, we often express gains in decibels by taking 20 times the common logarithm of the gain magnitude. Taking the magnitudes of both sides of Equation (8.5), we have

$$|A_v(f)| = \frac{1}{\sqrt{1 + (f/f_b)^2}} \quad (8.7)$$

Now, if this equation is expressed in decibels, we obtain

$$|A_v(f)|_{\text{dB}} = -20 \log \sqrt{1 + (f/f_b)^2} \quad (8.8)$$

which can also be written as

$$|A_v(f)|_{\text{dB}} = -10 \log [1 + (f/f_b)^2] \quad (8.9)$$

Logarithmic Frequency Scales

On a logarithmic scale, the variable is multiplied by a constant for a given distance along the axis. On a linear scale, a constant is added to the variable for a given distance along the axis.

In Bode plots, we use a **logarithmic scale** for frequency. On this kind of scale, the variable is *multiplied* by a given factor for equal increments of length along the axis. (On a linear scale, equal lengths on the scale correspond to *adding* a given amount to the variable.) A logarithmic frequency scale is shown in Figure 8.2.

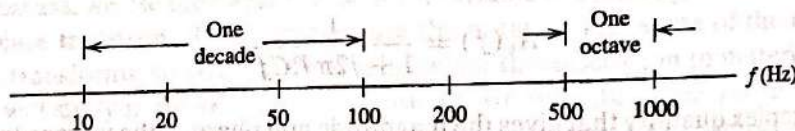


Figure 8.2 Logarithmic frequency scale.

A **decade** is a range of frequencies for which the ratio of the highest frequency to the lowest is 10. The frequency range from 2 Hz to 20 Hz is one decade. Similarly, the range from 50 Hz to 500 Hz is one decade, and 500 Hz to 5000 Hz is another decade.

An **octave** is a two-to-one change in frequency. For example, 10 Hz to 20 Hz is one octave. The range from 2 kHz to 16 kHz is three octaves.

The Magnitude Bode Plot

A Bode plot shows the magnitude of a network function in decibels versus frequency, with the latter on a logarithmic scale.

A Bode plot shows the magnitude of a network function in decibels versus frequency, with the latter on a logarithmic scale. It turns out that such plots of network functions can often be closely approximated by straight-line segments.

To illustrate, notice that the gain given by Equation (8.9) is approximately 0 dB for $f \ll f_b$. Thus, for low frequencies, the gain is approximated by the horizontal straight line shown in Figure 8.3, labeled as the **low-frequency asymptote**.

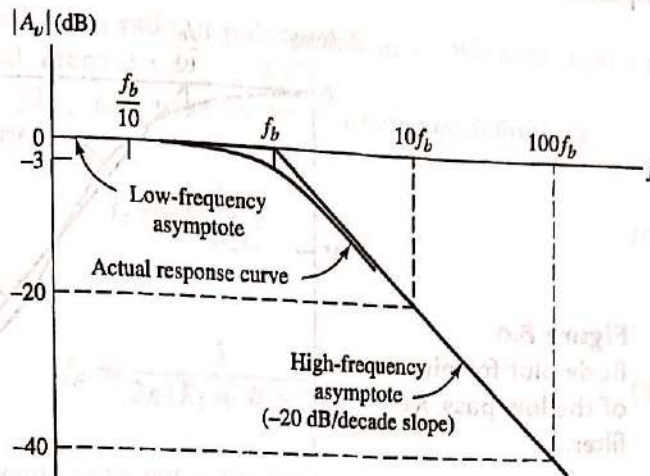


Figure 8.3
Bode plot for the
low-pass RC filter.

On the other hand, for $f \gg f_b$, Equation (8.9) becomes

$$|A_v(f)|_{dB} \cong -10 \log [(f/f_b)^2] \quad (8.10)$$

which is equivalent to

$$|A_v(f)|_{dB} \cong -20 \log (f/f_b) \quad (8.11)$$

Evaluating Equation (8.11) for various values of f , we obtain the results shown in Table 8.1. Plotting these values results in the straight line shown sloping downward on the right-hand side of Figure 8.3, labeled as the **high-frequency asymptote**.

Notice that the two straight-line asymptotes intersect at the break frequency f_b . The slope of the high-frequency asymptote is -20 dB per decade of frequency. This slope can also be stated as -6 dB per octave.

If we evaluate Equation (8.9) at $f = f_b$, we find that

$$|A_v(f_b)|_{dB} \cong -3 \text{ dB} \quad (8.12)$$

Thus, the asymptotes are in error by only 3 dB at the corner frequency. Very likely, we would not be off by more than a fraction of a decibel by drawing a freehand curve through this point, asymptotically approaching the straight-line approximations for large and small values of f . The actual curve for $|A_v(f)|_{dB}$ is also shown in Figure 8.3.

The Phase Plot

From Equation (8.5), we find that the phase of $A_v(f)$ is

$$\theta = -\arctan(f/f_b)$$

Evaluating, we find that the phase approaches zero at very low frequencies, equals -45° at the corner frequency, and approaches -90° at high frequencies.

Table 8.1. Values of the high-frequency asymptote of $|A_v(f)|_{dB}$ for selected frequencies.

f	$ A_v(f) _{dB}$
f_b	0
$2f_b$	-6
$10f_b$	-20
$100f_b$	-40
$1000f_b$	-60

The slope of the high-frequency asymptote is -20 dB per decade of frequency. This slope can also be stated as -6 dB per octave.

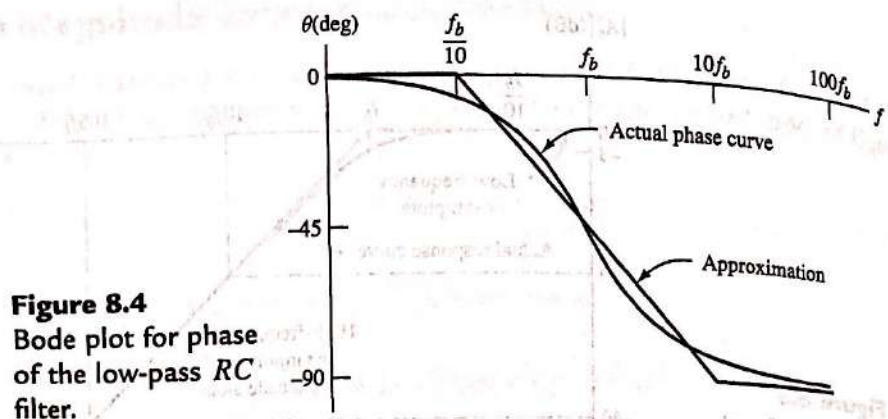


Figure 8.4
Bode plot for phase
of the low-pass RC
filter.

Figure 8.4 shows a plot of phase versus frequency. Notice that the curve can be approximated by the following straight-line segments: a horizontal line at zero for $f < f_b/10$; a sloping line from zero phase at $f_b/10$ to -90° at $10f_b$; and a horizontal line at -90° for $f > 10f_b$. The actual phase curve departs from these straight-line approximations by less than 6° . Thus, working by hand, we can easily construct an approximate plot of phase versus frequency.

Many circuit functions can be plotted by the methods that we have just demonstrated for the simple lowpass RC circuit.

Example 8.1 Bode Plot for an RC Circuit with One Pole and One Zero

Prepare Bode plots of the magnitude and phase of the voltage transfer function $A_v(f) = V_o/V_{in}$ for the circuit shown in Figure 8.5. (The component values have been selected to result in convenient break frequencies.)

SOLUTION First, we write an expression for the transfer function by applying the voltage-divider principle. Accordingly, the voltage-transfer function is the ratio of the series impedance of R_2 and C to the sum of the impedances of R_1 , R_2 , and C . Thus, we have

$$A_v(s) = \frac{V_o}{V_{in}}(s) = \frac{R_2 + 1/sC}{R_1 + R_2 + 1/sC} \quad (8.13)$$

Rearranging Equation (8.13), we get

$$A_v(s) = \frac{V_o}{V_{in}}(s) = \frac{sR_2C + 1}{s(R_1 + R_2)C + 1} \quad (8.14)$$

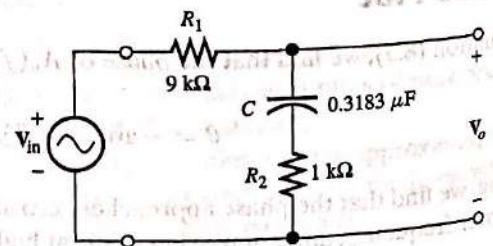


Figure 8.5
Circuit for
Example 8.1.

As expected, the result is a ratio of polynomials in s . We have a pole at $s = -1/(R_1 + R_2)C$ and a zero at $s = -1/R_2C$.

If we substitute $s = j2\pi f$ and make the break frequency definitions

$$f_z = \frac{1}{2\pi R_2 C} \quad (8.15)$$

and

$$f_p = \frac{1}{2\pi(R_1 + R_2)C} \quad (8.16)$$

the expression for the gain can be put in the form

$$A_v(f) = \frac{1 + j(f/f_z)}{1 + j(f/f_p)} \quad (8.17)$$

Notice that f_z is the break frequency associated with the zero, and f_p is associated with the pole. For the circuit values given in Figure 8.5, the break frequencies are $f_p = 50$ Hz and $f_z = 500$ Hz.

Taking the magnitude of both sides of Equation (8.17), we obtain

$$|A_v(f)| = \frac{\sqrt{1 + (f/f_z)^2}}{\sqrt{1 + (f/f_p)^2}} \quad (8.18)$$

Expressing this equation in decibels, we have

$$|A_v(f)|_{dB} = 20 \log \sqrt{1 + (f/f_z)^2} - 20 \log \sqrt{1 + (f/f_p)^2} \quad (8.19)$$

Each of the terms on the right-hand side of this expression is similar to the right-hand side of Equation (8.8). Thus, for $f > f_p$, the second term on the right-hand side is approximated as a straight line starting from 0 dB at $f = f_p$, with a slope of -20 dB/decade. For $f < f_p$, the second term is approximated by 0 dB.

The first term on the right-hand side of Equation (8.19) is identical to the second term, except for the algebraic sign and except for the replacement of f_p by f_z . Thus, for $f > f_z$, the first term is approximated as a line starting from 0 dB at $f = f_z$ with a $+20$ dB/decade slope. For $f < f_z$, the first term is approximately 0 dB. The approximations for each term of Equation (8.19) are displayed in Figure 8.6.

At the respective break frequencies, the actual values are -3 dB for the second term and $+3$ dB for the first term. The overall transfer function plot is obtained by adding the contributions from both terms. A plot of the actual transfer function is compared with the straight-line asymptotes in Figure 8.7.

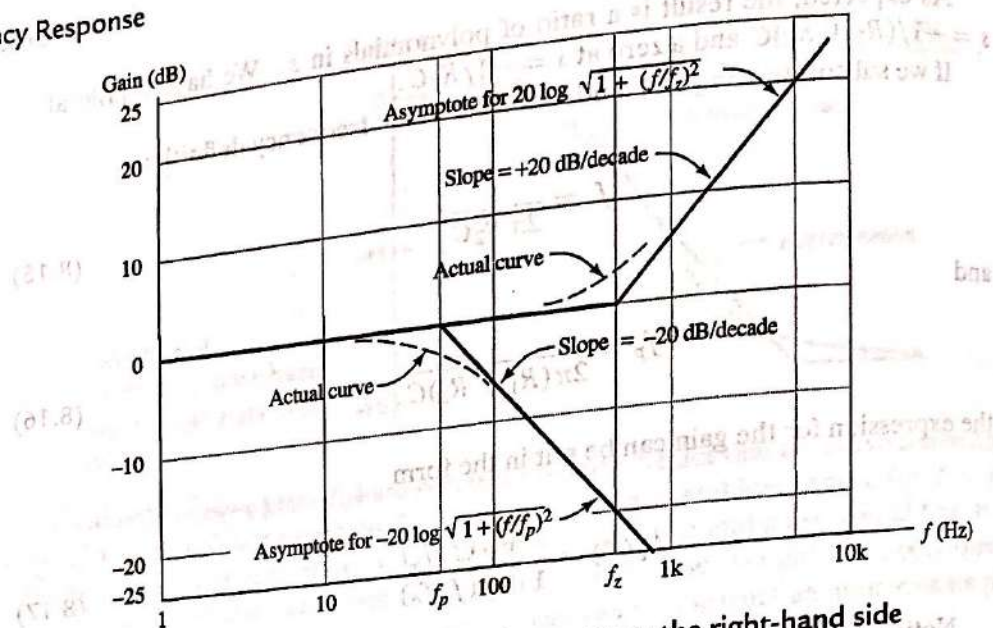


Figure 8.6 Bode plots of the terms on the right-hand side of Equation (8.19).

Referring to Equation (8.17), we find that the phase is

$$\theta = \arctan(f/f_z) - \arctan(f/f_p) \quad (8.20)$$

Again, we have two terms, each of which is similar to the phase for the lowpass RC circuit analyzed earlier. Approximations for each of the terms on

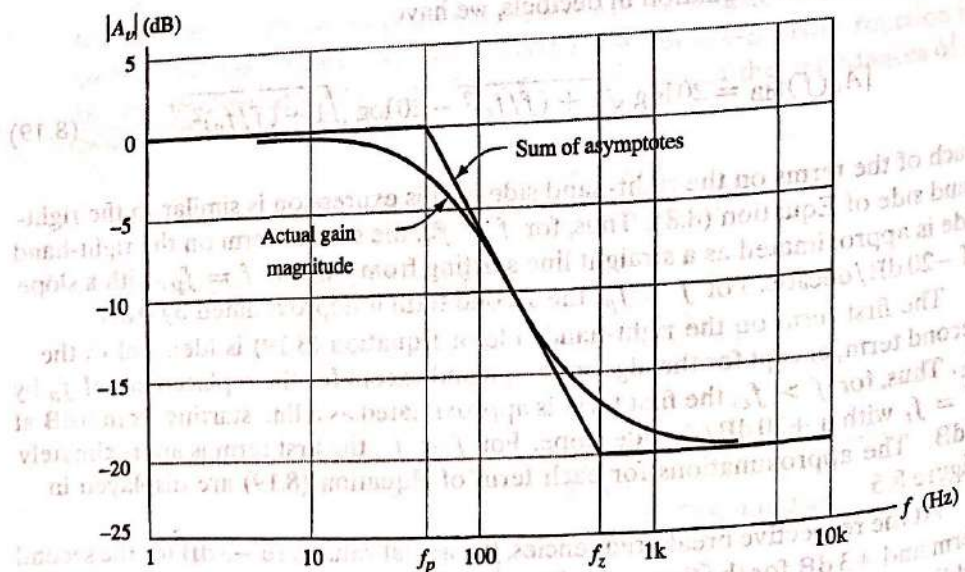


Figure 8.7 Bode plot of the magnitude of A_v for the circuit of Figure 8.5.

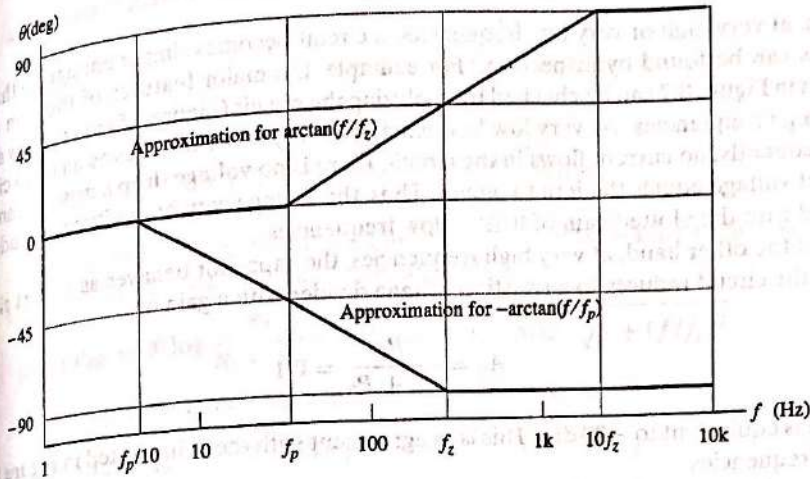


Figure 8.8 Approximate plots of the terms of Equation (8.20).

the right-hand side of Equation (8.20) are illustrated in Figure 8.8. The first term is approximated as zero for $f < f_z/10$ and $+90^\circ$ for $f > 10f_z$. A sloping line connects 0° at $f_z/10$ to 90° at $10f_z$. The approximation for the second term in Equation (8.20) is constructed in a similar fashion.

An approximation for the overall phase is obtained by adding the approximations for the separate terms. Figure 8.9 compares the actual phase with the approximation. □

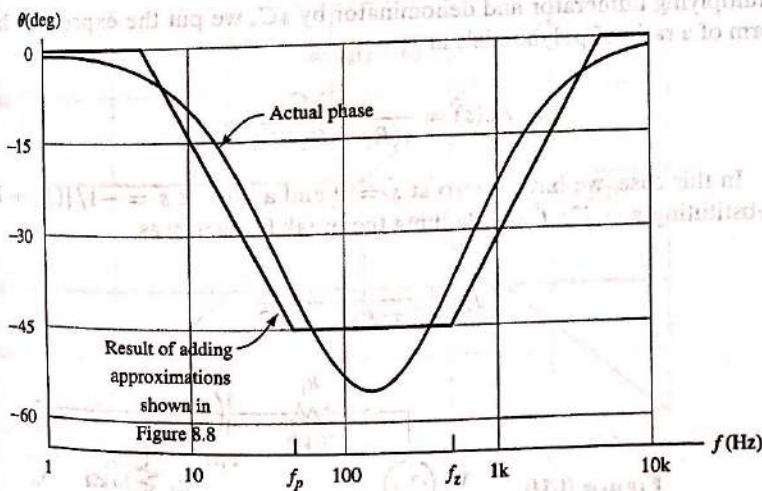


Figure 8.9 Bode phase plot of the voltage-transfer function for the circuit of Figure 8.5.

Often, at very high or very low frequencies, a circuit becomes simple enough so that the results can be found by inspection.

At very low frequencies, capacitors behave as open circuits. At very high frequencies, they behave as short circuits.

Simple Checks of the Bode Plot

Often, at very high or very low frequencies, a circuit becomes simple enough so that the results can be found by inspection. For example, the major features of the gain curve shown in Figure 8.7 can be checked by analyzing the circuit (Figure 8.5) at very low and at very high frequencies. At very low frequencies, the capacitor behaves as an open circuit. Consequently, no current flows in the circuit, there is no voltage drop across R_1 , and the output voltage equals the input voltage. Thus, the voltage gain has unity magnitude—in accord with the plotted gain of 0 dB at low frequencies.

On the other hand, at very high frequencies, the capacitor behaves as a short circuit. Then the circuit reduces to a resistive voltage divider with a gain of

$$A_v = \frac{R_2}{R_1 + R_2} = 0.1$$

which is equivalent to -20 dB. This is in agreement with the gain plotted in Figure 8.7 at high frequencies.

Example 8.2 Bode Plot for a High Pass RC Filter

Prepare Bode plots of the magnitude and phase of the voltage transfer function $A_v = V_o/V_{in}(f)$ for the circuit illustrated in Figure 8.10.

SOLUTION Again, we can write an expression for the gain with the use of the voltage-divider principle. The result is

$$A_v(s) = \frac{V_o}{V_{in}}(s) = \frac{R_2}{R_1 + R_2 + 1/sC}$$

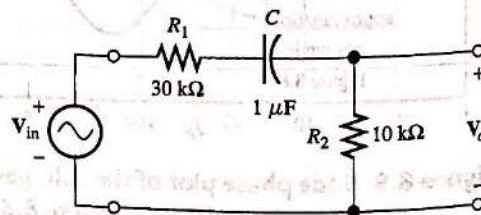
Multiplying numerator and denominator by sC , we put the expression into the form of a ratio of polynomials in s :

$$A_v(s) = \frac{sR_2C}{s(R_1 + R_2)C + 1} \quad (8.21)$$

In this case, we have a zero at $s = 0$ and a pole at $s = -1/[(R_1 + R_2)C]$. Substituting $s = j2\pi f$ and defining the break frequency as

$$f_p = \frac{1}{2\pi(R_1 + R_2)C} \quad (8.22)$$

Figure 8.10
Circuit of
Example 8.2.



we can put Equation (8.21) into the form

$$A_v(f) = \frac{R_2}{R_1 + R_2} \times \frac{j(f/f_p)}{1 + j(f/f_p)} \quad (8.23)$$

The magnitude of this equation is

$$|A_v(f)| = \frac{R_2}{R_1 + R_2} \times \frac{f/f_p}{\sqrt{1 + (f/f_p)^2}}$$

Taking 20 times the logarithm of the magnitude of both sides of the preceding equation converts the gain magnitude to decibels:

$$|A_v(f)|_{dB} = 20 \log \frac{R_2}{R_1 + R_2} + 20 \log(f/f_p) - 20 \log \sqrt{1 + (f/f_p)^2} \quad (8.24)$$

Substituting the component values, we have

$$|A_v(f)|_{dB} = -12 + 20 \log(f/3.98) - 20 \log \sqrt{1 + (f/3.98)^2} \quad (8.25)$$

Notice that the first term on the right-hand side of Equation (8.25) is constant at all frequencies. The second term is a straight line passing through 0 dB at $f = 3.98$ Hz and having a slope of +20 dB/decade.

The last term is similar to those contributed by poles in the previous examples. The asymptotes for the last term are a horizontal line at zero decibels for low frequencies and a line starting at the point (0 dB, f_p) with a slope of -20 dB/decade.

Figure 8.11 shows plots of the asymptotes for all three terms. Figure 8.12 displays the Bode magnitude plot for the gain obtained by adding the asymptotes. The actual gain plot is also shown for comparison.

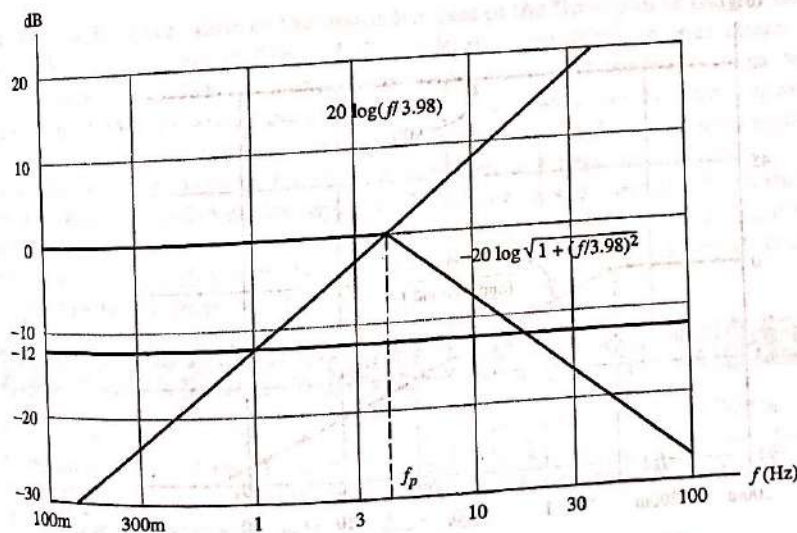


Figure 8.11 Plots of the terms on the right-hand side of Equation (8.25).

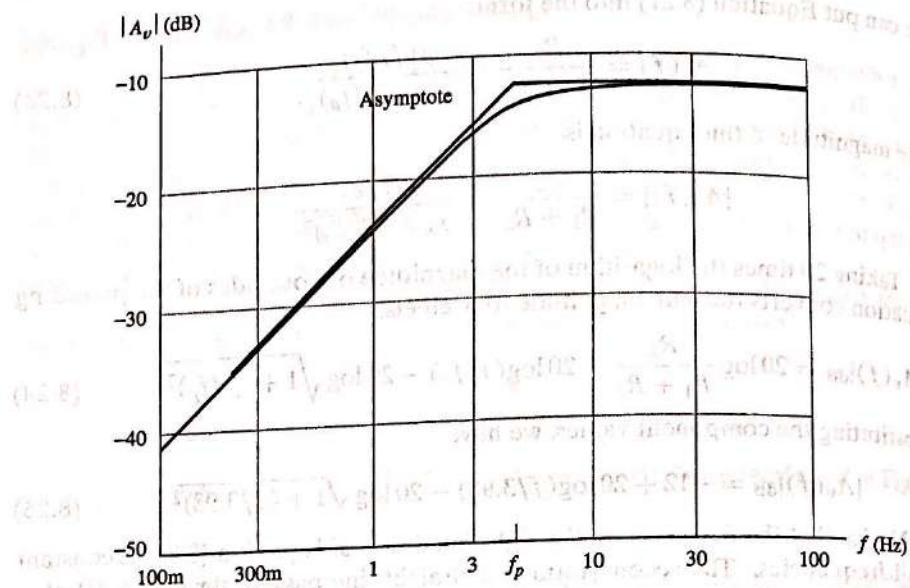


Figure 8.12 Magnitude Bode plot for the circuit of Figure 8.10.

The phase of Equation (8.23) is

$$\theta = 90^\circ - \arctan(f/3.98) \quad (8.26)$$

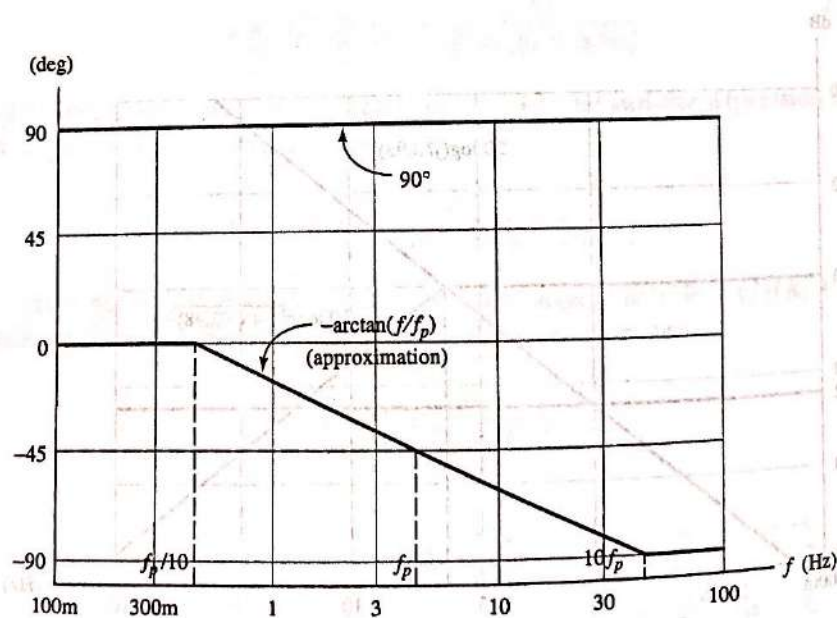


Figure 8.13 Plots of the terms on the right-hand side of Equation (8.26).

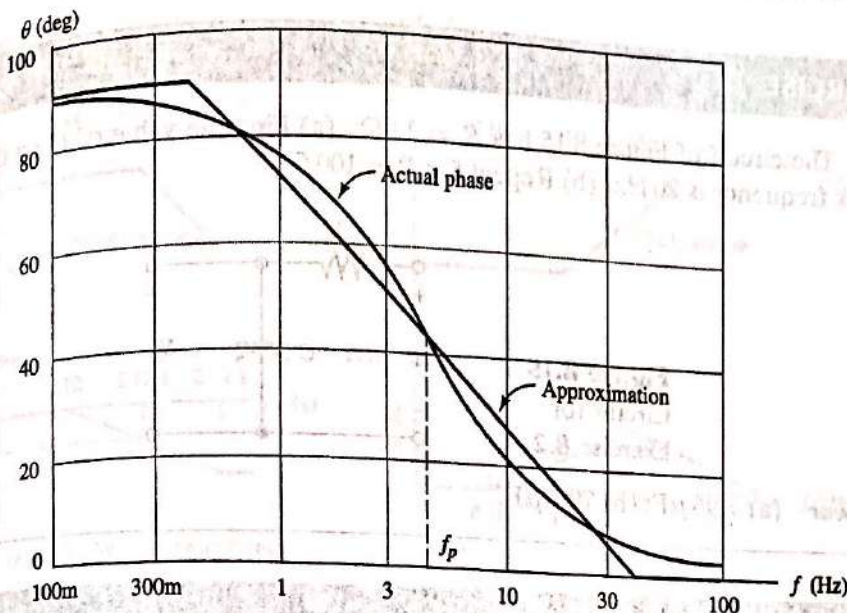


Figure 8.14 Bode phase plot for the voltage-transfer function of the circuit shown in Figure 8.10.

The j in the numerator of Equation (8.23) is responsible for the constant 90° phase shift. The denominator contributes the second term. The two terms of Equation (8.26) are plotted in Figure 8.13. A straight-line approximation is shown for the second term. Figure 8.14 plots the overall phase.

We can easily check some of the major features of the Bode plot of the last example. Consider the circuit shown in Figure 8.10. At dc, the capacitor is an open circuit, so the gain magnitude is zero. This observation is in agreement with the Bode magnitude plot of Figure 8.12, which shows the gain declining by 20 dB/decade as frequency approaches zero. (On a logarithmic scale, zero is infinitely far to the left. Thus, the gain approaches $-\infty$ dB, which is equivalent to zero gain magnitude, as f approaches zero.)

At very high frequencies, the capacitor behaves as a short circuit. Then the circuit becomes a resistive voltage divider. The output voltage is one-quarter of the input voltage. Expressed in decibels, this is $20 \log(0.25) = -12$ dB. Notice that the result is the gain approached by the Bode plot of Figure 8.12 for high frequencies.

EXERCISE

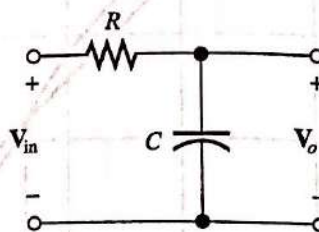
8.1 A certain circuit has an input voltage given by $v_{in}(t) = 5 \cos(2000\pi t - 30^\circ)$. Examination of the Bode plots for the voltage transfer function V_o/V_{in} at a frequency of 1000 Hz yields a gain magnitude of -6 dB and a phase shift of $+45^\circ$. Find the steady-state output voltage $v_o(t)$ for the circuit.

Answer $v_o(t) = 2.5 \cos(2000\pi t + 15^\circ)$.

EXERCISE

8.2 The circuit of Figure 8.15 has $R = 1 \text{ k}\Omega$. (a) Find the value of C so that the break frequency is 20 Hz. (b) Repeat for $R = 100 \Omega$.

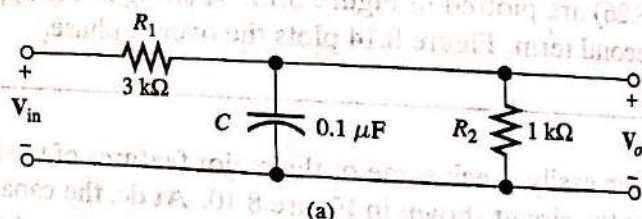
Figure 8.15
Circuit for
Exercise 8.2.



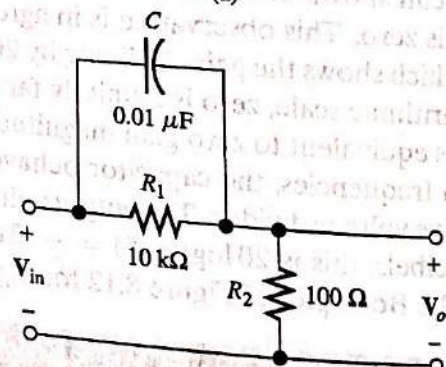
Answer (a) $7.96 \mu\text{F}$; (b) $79.6 \mu\text{F}$.

EXERCISE

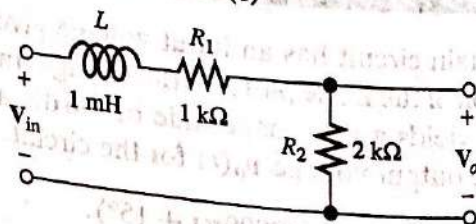
8.3 Prepare Bode magnitude and phase plots for the voltage-transfer function of each of the circuits displayed in Figure 8.16. Use straight-line approximations rather than the actual curves. Use a range of frequencies that extends above and below each break frequency by at least one decade.



(a)



(b)



(c)

Figure 8.16
Circuits for
Exercise 8.3.

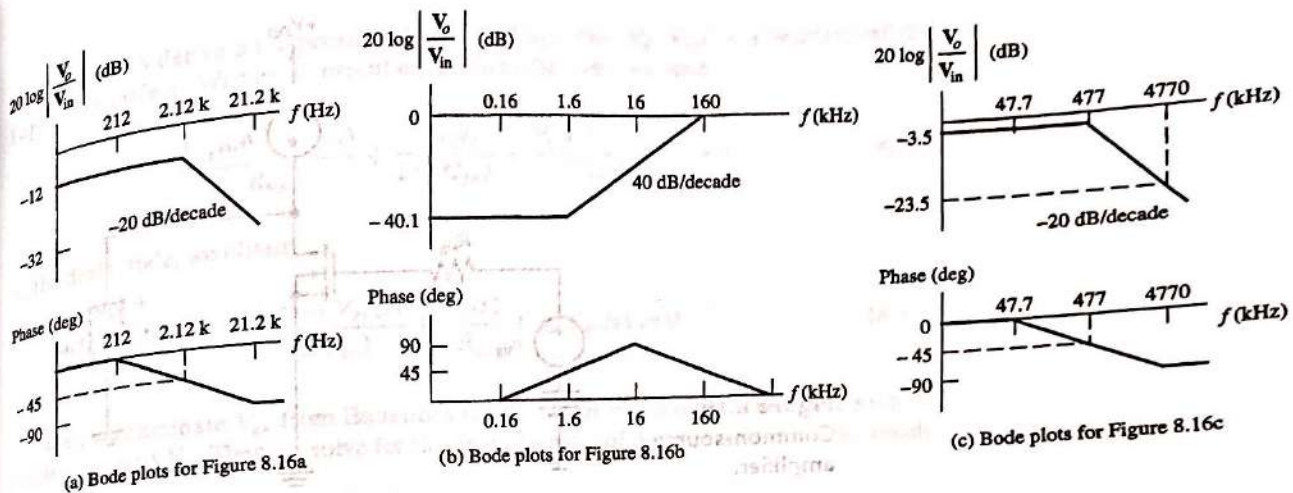


Figure 8.17 Answers for Exercise 8.3.

Answer See Figure 8.17.

8.2 THE FET COMMON-SOURCE AMPLIFIER AT HIGH FREQUENCIES

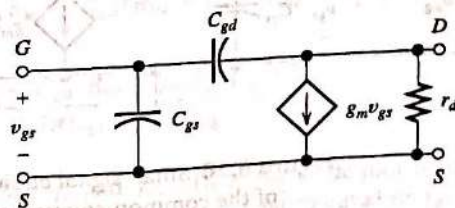
In this section, we analyze a common-source amplifier and obtain Bode plots of its gain magnitude.

A High-Frequency Equivalent Circuit for FETs

The high-frequency FET equivalent circuit that we use in this book is illustrated in Figure 8.18. It is the same as the low-frequency equivalent circuit shown in Figure 5.23, except for the addition of the gate-to-source capacitance C_{gs} and the gate-to-drain capacitance C_{gd} .

Actually, Figure 8.18 is an approximate equivalent circuit, because the gate capacitance is distributed along the length of the channel rather than being lumped. Furthermore, for accurate modeling of FETs in ICs, it is sometimes necessary to include capacitances from source and drain to the bulk terminal, which is normally connected to ground. However, the equivalent circuit shown in Figure 8.18 is adequate for most purposes.

Figure 8.18
High-frequency FET
equivalent circuit.



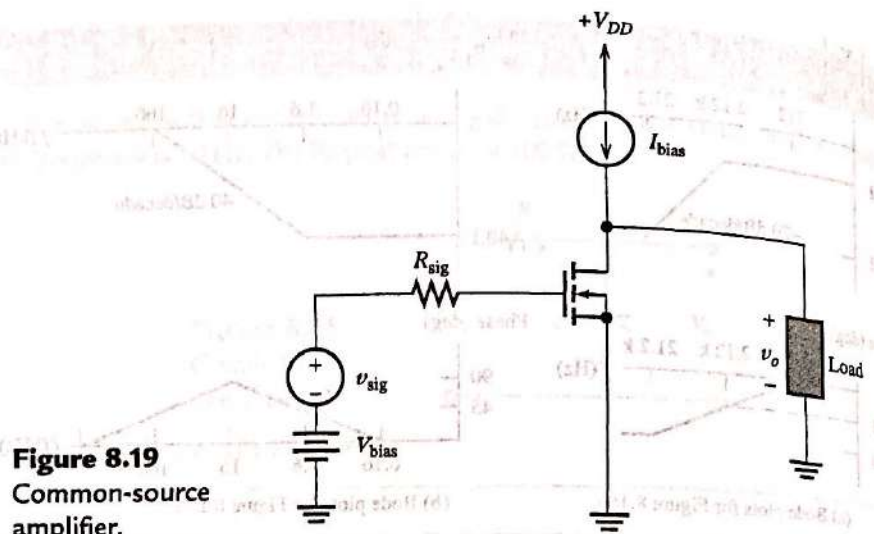


Figure 8.19
Common-source
amplifier.

The Common-Source Amplifier

Figure 8.19 shows a common-source amplifier in which v_{sig} represents the signal to be amplified and R_{sig} is the internal impedance of the signal source. V_{bias} represents the bias voltage applied to the gate of the FET by the preceding stage. The bias current source I_{bias} can be implemented by a current mirror as discussed in Chapter 7. We assume that the FET is biased in the active (saturation) region. The load represents the input to the next stage in a multistage amplifier, or the actual load if the common source is the last stage in a multistage amplifier.

The Equivalent Circuit

The equivalent circuit for the common-source amplifier is displayed in Figure 8.20. The FET has been replaced by its high-frequency equivalent circuit. As usual, we replace the dc sources V_{bias} and V_{DD} by short circuits. R_{bias} represents the output resistance of the current source, and R_L is the load resistance. We denote the parallel combination of R_{bias} , r_d , and R_L as

$$R'_L = \frac{1}{1/r_d + 1/R_{bias} + 1/R_L} \quad (8.27)$$

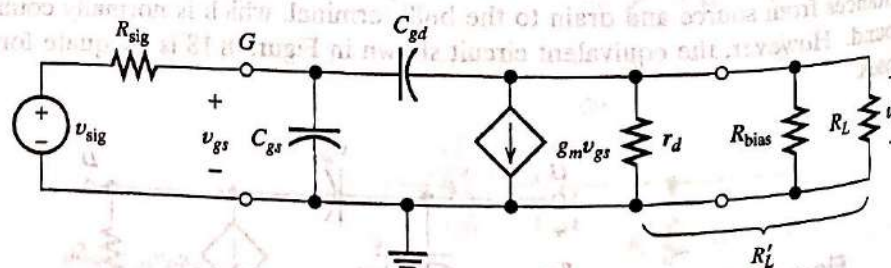


Figure 8.20 Small-signal equivalent circuit
of the common-source amplifier.

We want to derive an expression for the voltage gain V_o/V_{sig} as a function of the Laplace variable s . Writing a current equation at the gate, we have

$$\frac{V_{gs}(s) - V_{sig}(s)}{R_{sig}} + \frac{V_{gs}(s)}{1/(sC_{gs})} + \frac{V_{gs}(s) - V_o(s)}{1/(sC_{gd})} = 0 \quad (8.28)$$

At the drain node, we obtain

$$\frac{V_o(s) - V_{gs}(s)}{1/(sC_{gd})} + \frac{V_o(s)}{R'_L} + g_m V_{gs}(s) = 0 \quad (8.29)$$

Next, we eliminate V_{gs} from Equations (8.28) and (8.29) to obtain a single equation relating V_{sig} and V_o . Then we solve for the gain as a ratio of polynomials in s . The result is

$$A_v(s) = \frac{V_o}{V_{sig}} = -g_m R'_L \times \frac{1 - s(C_{gd}/g_m)}{1 + s[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)] + s^2 C_{gs} C_{gd} R_{sig} R'_L} \quad (8.30)$$

This equation can be written in the form

$$A_v(s) = A_{mid} \frac{1 + s/\omega_z}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \quad (8.31)$$

in which

$$A_{mid} = -g_m R'_L \quad (8.32)$$

is the midband gain. Notice that $A_v(s)$ has two poles and one zero. The corresponding break frequencies are

$$f_z = \frac{g_m}{2\pi C_{gd}} \quad (8.33)$$

$$f_{p1} = \frac{1}{2\pi [C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]} \quad (8.34)$$

and

$$f_{p2} = \frac{C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)}{2\pi C_{gs}C_{gd}R'_L R_{sig}} \quad (8.35)$$

Usually, f_{p1} is much lower than f_z and f_{p2} . Then, the Bode plot is similar to Figure 8.21, and the upper half-power frequency is approximately equal to f_{p1} .

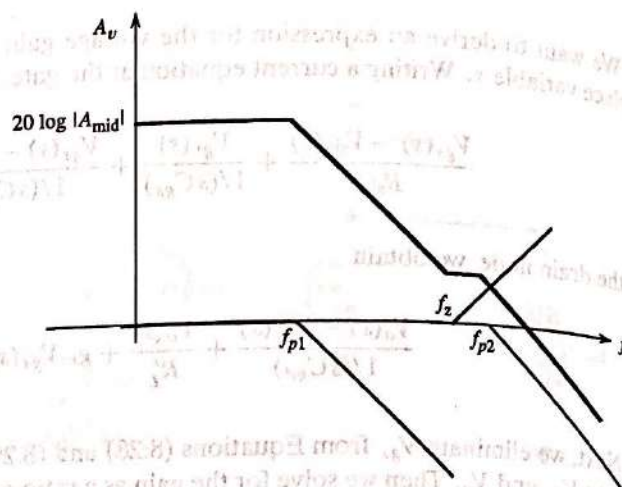


Figure 8.21
Bode plot of voltage gain for a typical common-source stage.

Some important lessons about the common-source amplifier can be gained from Equation (8.34). To attain a higher value for the upper half-power frequency we should

1. Reduce the device capacitances C_{gs} and C_{ds} .
2. Reduce the source and load resistances R_{sig} and R_L .

Furthermore, the dominant term in the denominator of Equation (8.34) is normally $C_{gd}g_m R'_L R_{sig} = C_{gd}|A_{mid}|R_{sig}$. (We have used Equation 8.32 to substitute $|A_{mid}|$ for $g_m R'_L$.) Thus, two more important observations are that

3. Reducing C_{gd} is more important than reducing C_{gs} .
4. Lower gain magnitude leads to wider bandwidth.

These observations can be made more apparent by considering a numerical example.

Example 8.3 Common-Source Amplifier Analysis

Consider the circuit shown in Figure 8.22. The load is connected to the drain through a $1\text{-}\mu\text{F}$ coupling capacitor, which is treated as a short circuit in the high-frequency equivalent circuit. The bias current source is ideal (i.e., $R_{bias} = \infty$) and

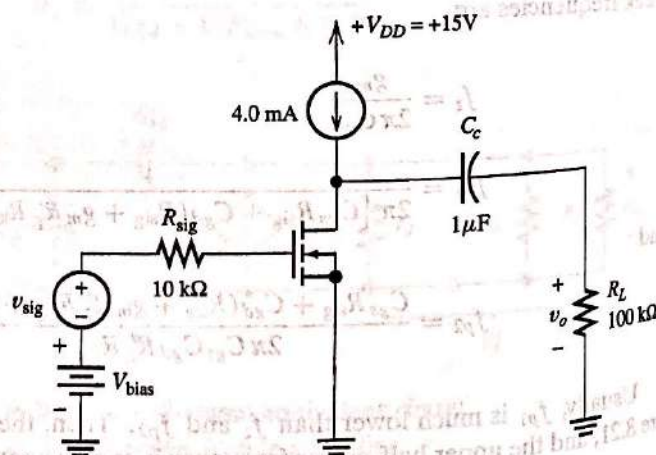


Figure 8.22
Common-source stage of Examples 8.3 and 8.4.

supplies 4 mA. The FET operates in the saturation region with $V_{DSQ} = 10$ V. The FET has $KP = 50 \mu\text{A}/\text{V}^2$, $W/L = (400 \mu\text{m})/(10 \mu\text{m})$, $V_{to} = 1$ V, $\lambda = 0.01$, $C_{gs} = 1$ pF, and $C_{gd} = 1$ pF. Determine the midband gain, the break frequencies, and the approximate upper half-power frequency for A_v .

SOLUTION The high-frequency equivalent circuit is identical to Figure 8.20, and the results that we derived in this section are applicable. First, we need to determine g_m and r_d for the FET. Using Equation (5.3), we have

$$K = \left(\frac{W}{L}\right) \frac{KP}{2} = 40 \times \frac{50 \times 10^{-6}}{2} = 1 \text{ mA}/\text{V}^2$$

Then, from Equation (5.29), we compute

$$g_m \cong 2\sqrt{KI_{DQ}} = 4 \text{ mS}$$

and we also have

$$r_d \cong \frac{1}{\lambda I_{DQ}} = \frac{1}{0.01(4 \times 10^{-3})} = 25 \text{ k}\Omega$$

(The value that we have found for g_m is approximate, because the formula that we have used was derived assuming that $\lambda = 0$.) The effective load resistance is

$$R'_L = \frac{1}{1/r_d + 1/R_{\text{bias}} + 1/R_L} = \frac{1}{1/25 + 0 + 1/100} = 20 \text{ k}\Omega$$

The midband gain is

$$A_{\text{mid}} = -g_m R'_L = -(4 \times 10^{-3}) \times (20 \times 10^3) = -80$$

Converting to decibels, we have

$$A_{\text{mid}} = 20 \log(80) = 38.1 \text{ dB}$$

The frequencies associated with the zero and the poles are

$$f_z = \frac{g_m}{2\pi C_{gd}} = 637 \text{ MHz}$$

$$f_{p1} = \frac{1}{2\pi [C_{gs} R_{\text{sig}} + C_{gd}(R_{\text{sig}} + g_m R'_L R_{\text{sig}} + R'_L)]} = 189 \text{ kHz}$$

$$\text{and } f_{p2} = \frac{C_{gs} R_{\text{sig}} + C_{gd}(R_{\text{sig}} + g_m R'_L R_{\text{sig}} + R'_L)}{2\pi C_{gs} C_{ds} R'_L R_{\text{sig}}} = 668 \text{ MHz}$$

As is often the case for common-source amplifiers, f_{p1} is much smaller than either f_z or f_{p2} . Thus, the overall half-power frequency is nearly equal to f_{p1} . $\square$

High-Frequency SPICE Models for the MOSFET

SPICE models for the MOSFET include parameters that account for the device capacitances. We will consider only the gate-to-source and gate-to-drain capacitances. The SPICE parameters relating to these capacitances are CGSO and CGDO, which are the gate-to-source and gate-to-drain capacitances per unit of gate width, respectively. For example, if we have $C_{gs} = C_{ds} = 1 \text{ pF}$ and $W = 400 \mu\text{m}$, then $\text{CGSO} = \text{CGDO} = 10^{-12} / (400 \times 10^{-6}) = 2.5 \times 10^{-9} \text{ F/m}$.

Example 8.4 SPICE Analysis of a Common-Source Amplifier

Determine the value of the bias voltage V_{bias} in the circuit of Example 8.3. Then use SPICE to verify that the half-power frequency of the amplifier is approximately 189 kHz.

SOLUTION In the circuit of Figure 8.22, we have $V_{GSQ} = V_{\text{bias}}$. From Equation (5.11), we have, for the Q -point values,

$$I_{DQ} = K(V_{GSQ} - V_{to})^2(1 + \lambda V_{DSQ})$$

Substituting values and solving for V_{GSQ} , we find that

$$V_{\text{bias}} = V_{GSQ} = 2.907 \text{ V}$$

The circuit schematic is stored in the file named Fig8.22. First, we click on the MOSFET symbol and use the **edit/model/edit instance model** command to bring up the window displayed in Figure 8.23, in which we enter the device parameters, including the capacitances as shown.

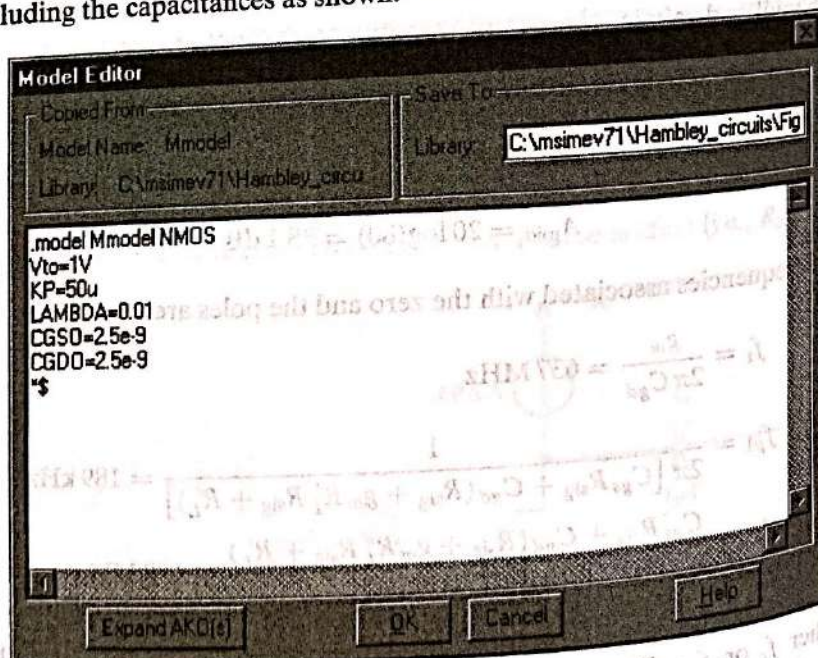


Figure 8.23 Model parameters for the MOSFET of Examples 8.3 and 8.4.

Subsequently, we use the `simulate/setup/ac sweep` command to bring up the ac sweep window, in which we select an ac sweep from 10 kHz to 10 MHz. Finally, we simulate the circuit and use Probe to obtain a Bode plot of the gain magnitude. Using the cursor, we find that the midband gain is 39.1 dB. The half-power frequency is the frequency at which the gain magnitude is $39.1 - 3 = 36.1$ dB. Using the cursor, we find that the half-power frequency is 168 kHz, which is in close agreement with the value computed for f_{p1} in Example 8.3.

The SPICE results do not agree exactly with the results that we calculated earlier, because we neglected λ in some of the manual calculations. However, in practice, we usually do not know the circuit parameters any closer than $\pm 10\%$; hence, exact calculations are not meaningful, anyway.

Review

In this section, we have shown how to determine the response of an amplifier at high-frequencies by exact analysis of the equivalent circuit. The step-by-step approach is as follows:

1. Draw the small-signal equivalent circuit. Replace dc voltage sources and current sources with their internal impedances. (Ideal voltage sources become short circuits, and ideal current sources become open circuits.) Treat coupling or bypass capacitors as short circuits.
2. Write circuit equations that relate the input voltage, output voltage, and other currents and/or voltages to each other.
3. Use algebra to obtain the voltage gain V_o/V_{sig} as a ratio of polynomials in s .
4. Factor the numerator and denominator polynomials to determine break frequencies.
5. Substitute values and draw the Bode plot.

Step-by-step approach to high-frequency amplifier analysis.

Most amplifier circuits can be analyzed by these methods. However, except for relatively simple circuits, the work can be very time consuming and tedious. Of course, we can use SPICE to find numerical results for any particular circuit, but it is often difficult to see how to improve a design from the results of numerical simulations. Analytical results are better in that they show how the break frequencies depend on component values and which component values are most critical. In the next section, we consider an approximate method of analysis that is easier to apply than the exact method and that gives us some good insight into the design of amplifiers for extended high-frequency response.

EXERCISE

- 8.4 (a) In general, what happens to the pole frequency f_{p1} of the common-source amplifier if the load resistance increases? (b) If the source resistance R_{sig} increases?

Answer (a) decreases; (b) decreases.

EXERCISE

8.5 Repeat the calculation of f_{p1} in Example 8.3 if (a) $C_{gs} = 1$ pF and $C_{gd} = 2$ pF; (b) $C_{gs} = 2$ pF and $C_{gd} = 1$ pF. (c) Which of the two capacitances C_{gs} or C_{gd} is more critical in determining the upper half-power frequency?

Answer (a) $f_{p1} = 95.3$ kHz; (b) $f_{p1} = 187$ kHz; (c) C_{gs} is more critical.

EXERCISE

8.6 Verify that Equations (8.28) and (8.29) are correct. Then use them to derive Equation (8.30).

8.3 THE MILLER EFFECT

In this section, we discuss a situation that arises repeatedly in electronic circuits: An impedance is connected between the input and the output of an amplifier. We will see that this can have a dramatic effect on the equivalent input impedance of the circuit as a whole. Sometimes such an arrangement is intentional, and other times it is undesirable, but cannot be avoided. (For example, the capacitance C_{gd} appears between the input terminal and the output terminal in Figure 8.20.)

Figure 8.24a shows an impedance Z_f connected between the input and the output terminals of an amplifier. We call Z_f a **feedback impedance** because it returns current from the amplifier output to the input. (We give a detailed discussion of the important topic of feedback amplifiers in Chapter 9.) The phasor voltages and currents are represented by boldface symbols such as V_i , V_o , and I_f .

Notice that the lower input terminal and the lower output terminal are common. The following discussion does not apply unless there is a common terminal for the input and output.

The voltage across the feedback impedance is

$$V_f = V_i - V_o$$

Substituting

$$V_o = A_v V_i$$

we obtain

$$V_f = V_i(1 - A_v)$$

where A_v is the voltage gain with the impedance Z_f in place. (A_v is a complex quantity having both magnitude and phase.) The current through the feedback impedance is

$$I_f = \frac{V_f}{Z_f} = \frac{V_i(1 - A_v)}{Z_f}$$

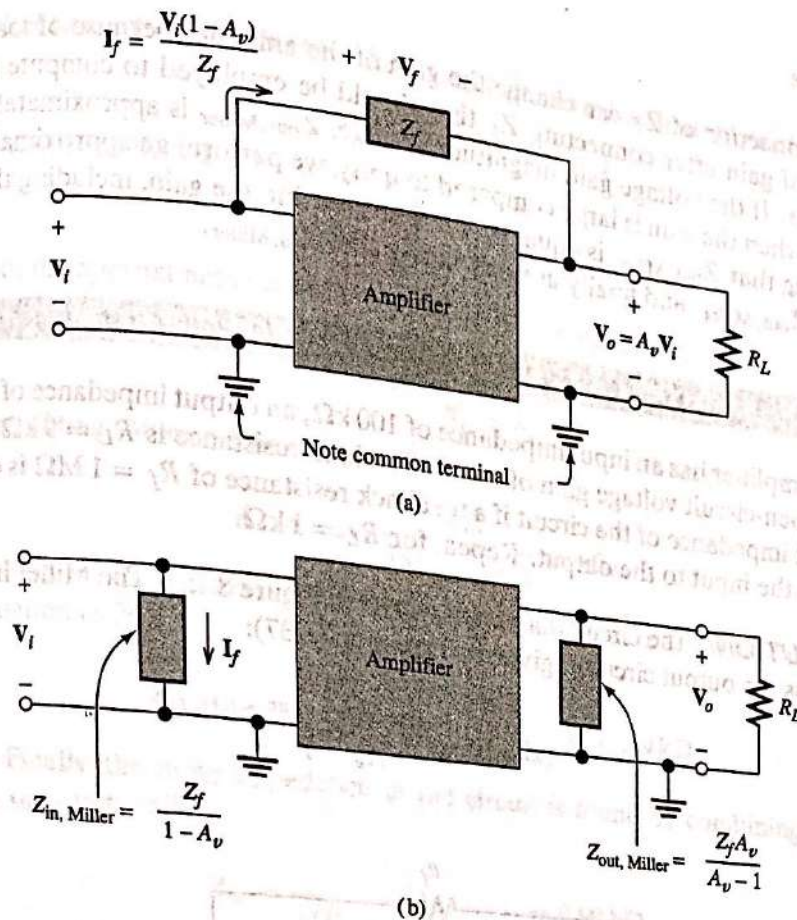


Figure 8.24 A feedback impedance can be replaced by impedances in parallel with the input and output terminals.

Now notice that this same current flows from the top input terminal if an impedance

$$Z_{\text{in, Miller}} = \frac{Z_f}{1 - A_v} \quad (8.36)$$

is connected across the input terminals, as illustrated in Figure 8.24b.

Thus, the effect seen at the input terminals that results from connecting an impedance Z_f from the input to the output is the same as the effects that result from connecting an impedance $Z_{\text{in, Miller}}$ across the input terminals. This is known as the **Miller effect** and is an important concept.

For example, if the amplifier gain is $A_v = -100$ and $Z_f = 1 \text{ k}\Omega$, we find that $Z_{\text{in, Miller}} \cong 9.9 \Omega$. Thus, if the voltage gain magnitude is large, the effective impedance seen across the input terminals is dramatically different from the value of Z_f .

Similarly, an equivalent impedance given by

$$Z_{\text{out, Miller}} = \frac{Z_f A_v}{A_v - 1} \quad (8.37)$$

can be connected across the output terminals to account for the loading of the output circuit by the feedback impedance.

An impedance Z_f connected from the input of an amplifier to the output can be replaced by an impedance

$Z_{in, \text{Miller}} = Z_f / (1 - A_v)$ across the input terminals and an impedance

$Z_{out, \text{Miller}} = Z_f A_v / (A_v - 1)$. This is known as the Miller effect.

The connection of Z_f can change the gain of the amplifier because of loading. It is the value of gain after connecting Z_f that should be employed to compute the Miller impedances. If the voltage gain magnitude is large, $Z_{out, \text{Miller}}$ is approximately equal to Z_f . Thus, when the gain is large compared to unity, we perform an approximate analysis by assuming that $Z_{out, \text{Miller}}$ is equal to Z_f . Then we find the gain, including the loading effects of $Z_{out, \text{Miller}}$, and finally use this gain to find $Z_{in, \text{Miller}}$.

Example 8.5 Using the Miller Effect to Determine Input Impedance

An amplifier has an input impedance of $100 \text{ k}\Omega$, an output impedance of $1 \text{ k}\Omega$, and an open-circuit voltage gain of -100 . The load resistance is $R_L = 9 \text{ k}\Omega$. Find the input impedance of the circuit if a feedback resistance of $R_f = 1 \text{ M}\Omega$ is connected from the input to the output. Repeat for $R_L = 1 \text{ k}\Omega$.

SOLUTION The circuit diagram is shown in Figure 8.25a. The Miller impedance across the output circuit is given by Equation (8.37):

$$Z_{out, \text{Miller}} = \frac{Z_f A_v}{A_v - 1}$$

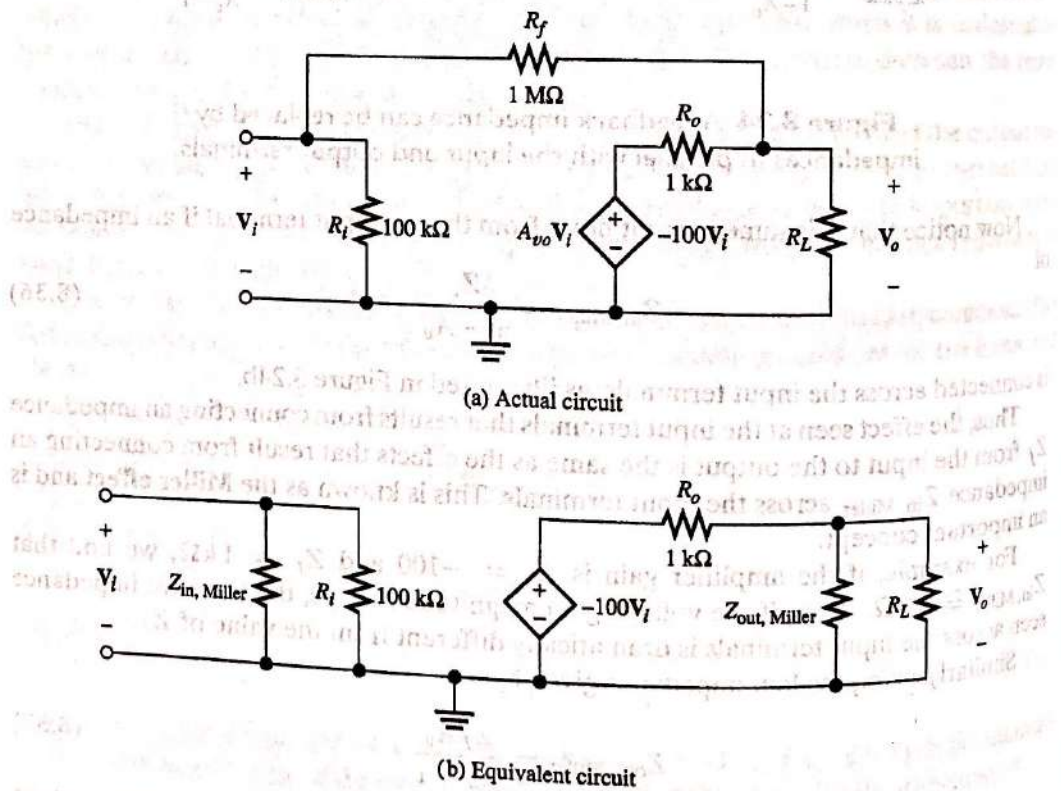


Figure 8.25 Circuit for Example 8.5.

Because we anticipate that $|A_v|$ is large compared with unity, we assume

$$Z_{\text{out, Miller}} \cong Z_f = R_f = 1 \text{ M}\Omega$$

We define the equivalent load resistance as

$$R'_L = R_L || Z_{\text{out, Miller}} \cong 1 \text{ k}\Omega$$

Next, the approximate loaded voltage gain can be computed:

$$A_v = A_{vo} \frac{R'_L}{R'_L + R_o}$$

Substituting values, we have

$$A_v = -100 \frac{9 \text{ k}\Omega}{9 \text{ k}\Omega + 1 \text{ k}\Omega} = -90$$

Now we can compute the impedance reflected into the input circuit by using

Equation (8.36):

$$Z_{\text{in, Miller}} = \frac{Z_f}{1 - A_v} = \frac{1 \text{ M}\Omega}{1 - (-90)} = 10.99 \text{ k}\Omega$$

Finally, the input impedance of the circuit is found by combining R_i and $Z_{\text{in, Miller}}$ in parallel:

$$Z_{\text{in}} = \frac{1}{1/R_i + 1/Z_{\text{in, Miller}}} = 9.90 \text{ k}\Omega$$

Repeating the calculations for $R_L = 1 \text{ k}\Omega$, we find that

$$A_v = -50$$

$$Z_{\text{in, Miller}} = 19.61 \text{ k}\Omega$$

$$Z_{\text{in}} = 16.4 \text{ k}\Omega$$

Notice that the input impedance of this circuit depends on the value of the load impedance. $\square$

EXERCISE

8.7 An amplifier has an open-circuit voltage gain $A_{vo} = -1000$, an input resistance $R_i = 1 \text{ M}\Omega$, and an output resistance $R_o = 1 \text{ k}\Omega$. The input and output of the amplifier have a common ground. A load $R_L = 2 \text{ k}\Omega$ is connected across the output terminals, and a feedback resistance $R_f = 1 \text{ M}\Omega$ is connected from input to output. (a) Find the voltage gain and input impedance of the circuit. (b) Repeat if the load is changed to an open circuit. (Hint: The solution can be simplified by assuming that $R_{o, \text{Miller}}$ is equal to R_f . This is justified because A_v is large in magnitude.)

Answer (a) $A_v = -666.2$ and $Z_{\text{in}} = 1497 \Omega$. (b) $A_v = -999.0$ and $Z_{\text{in}} = 999 \Omega$.

Miller Effect Applied to Feedback Capacitance

If the feedback impedance is a capacitor C_f , then we have

$$Z_f = \frac{1}{j\omega C_f}$$

Applying Equation (8.36), we find that the Miller impedance reflected across the input terminals is

$$Z_{\text{in, Miller}} = \frac{1}{j\omega C_f(1 - A_v)}$$

Therefore, connecting a capacitance C_f from input to output is equivalent to connecting a capacitance $C_f(1 - A_v)$ across the input terminals.

This observation is important because many amplifier circuits have a large negative gain and the devices used in these amplifiers often have a small capacitance between the input and output. Because of the Miller effect, this small feedback capacitance appears across the input terminals as a much larger equivalent capacitance. For example, if $A_v = -100$ and $C_f = 2$ pF, then the effective capacitance across the input terminals is $C_f(1 - A_v) = 202$ pF. At high frequencies, this capacitance has a low impedance that tends to short out the input signal.

The exact high-frequency analysis of amplifiers can be tedious. Approximate calculations based on the Miller approximation in which we ignore the effects of $Z_{\text{out, Miller}}$ are often useful.

Example 8.6 Upper Half-Power Frequency Using the Miller Effect

Use the Miller effect to compute the approximate upper half-power frequency for $A_{vs} = V_o/V_{\text{sig}}$ of the amplifier of Example 8.3. The amplifier is illustrated in Figure 8.22. Neglect $Z_{\text{out, Miller}}$.

SOLUTION The equivalent circuit is shown in Figure 8.26a. Notice that C_{gd} is connected from the input (gate) terminal to the output (drain) terminal. Replacing C_{gd} by its Miller equivalent, we obtain the circuit displayed in Figure 8.26b. In Example 8.3, we determined that $R'_L = 20$ k Ω and that the midband voltage gain is

$$A_v = V_o/V_i = -g_m R'_L = -80$$

Hence, the Miller equivalent for C_{gd} is

$$C_{\text{Miller}} = (1 - A_v)C_{gd} = 81 \text{ pF}$$

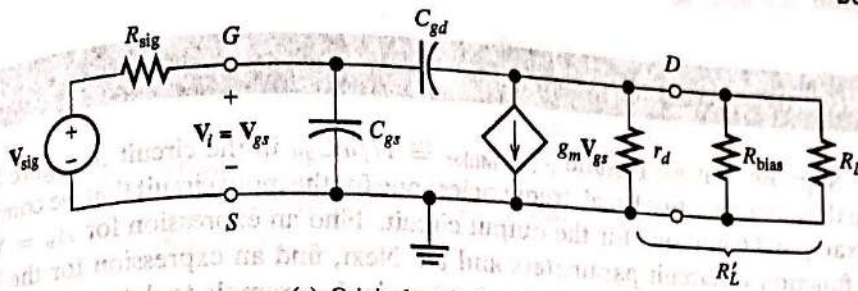
The total capacitance is

$$C_{\text{total}} = C_{gs} + C_{\text{Miller}} = 82 \text{ pF}$$

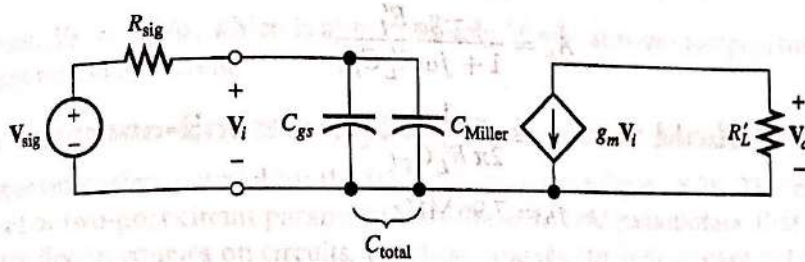
Now notice that R_{sig} and C_{total} form an RC lowpass filter similar to the filter illustrated in Figure 8.1. The break frequency is

$$f_b = \frac{1}{2\pi R_{\text{sig}} C_{\text{total}}} = 194 \text{ kHz}$$

which is very close to the value (189 kHz) computed in Example 8.3. $\square$



(a) Original equivalent circuit



(b) Equivalent circuit after applying the Miller approximation

Figure 8.26 Equivalent circuits for Example 8.6.

Gain-Bandwidth Product

Notice that $C_{\text{total}} \cong C_{\text{Miller}} \cong |A_{\text{mid}}|C_{gd}$. Thus, the approximate half-power frequency is

$$f_b \cong \frac{1}{2\pi R_{\text{sig}} |A_{\text{mid}}| C_{gd}}$$

Now we define the **gain-bandwidth product** GB of the amplifier to be the product of the midband gain and the upper half-power frequency:

$$GB = |A_{\text{mid}}| f_b$$

For the common-source amplifier under consideration, we have

$$GB = \frac{1}{2\pi R_{\text{sig}} C_{gd}}$$

If we increase the gain by increasing R'_L or g_m , GB is unchanged, and the bandwidth of the amplifier is reduced.

If we increase the gain magnitude of the common-source amplifier, the bandwidth is reduced such that the product of gain and bandwidth is constant.

EXERCISE

8.8 Suppose that we include $Z_{\text{out, Miller}} \cong 1/j\omega C_{gd}$ in the circuit of Figure 8.26b. Then the circuit has two break frequencies: one for the input circuit that we computed in Example 8.6 and one for the output circuit. Find an expression for $A_v = V_o/V_i$ as a function of circuit parameters and ω . Next, find an expression for the break frequency. Finally, substitute the values given in the example to determine the value of the break frequency for the output circuit.

Answer

$$A_v = \frac{-g_m R'_L}{1 + j\omega R'_L C_{gd}}$$

$$f_b = \frac{1}{2\pi R'_L C_{gd}}$$

$$f_b = 7.96 \text{ MHz}$$

Notice that the break frequency for the output circuit is much higher than that of the input circuit, so the half-power bandwidth is determined almost entirely by the input circuit.

8.4 THE HYBRID- π MODEL FOR THE BJT

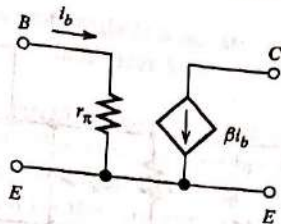
A large number of models, varying in complexity, have been developed for the BJT. Some models take nonlinear effects into account, whereas others are linear—valid only for small-signal analysis. Some models take device capacitances into account and can be accurate over a wide range of frequencies. However, simpler models are easier to use for low-frequency analysis.

We tend to select simple models for basic understanding and manual analysis. Complex nonlinear models are used mainly in computer-aided analysis. For example, the BJT model used by PSpice includes over 50 parameters, which would certainly be excessive for manual analysis.

The r_π - β Model

In Section 4.6, we developed the small-signal model for the BJT shown in Figure 8.27. This model applies for small voltage and current swings around a bias point in the active region. It is a low-frequency model that does not account for junction capacitances. It also ignores secondary effects such as base-width modulation. However, even this simple model is often sufficiently accurate for initial design.

Figure 8.27
The r_π - β model
for the BJT.



If β and the Q -point are known, the value of r_π can be calculated:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \quad (8.38)$$

As usual, $V_T = kT/q$, which is approximately 26 mV at room temperature. I_{CQ} is the Q -point collector current.

The Common-Emitter Hybrid-Parameter Model

Another small-signal model for the BJT is illustrated in Figure 8.28. This model is based on a set of two-port circuit parameters, known as **hybrid parameters**, that you probably have studied in courses on circuits. (In these courses, the hybrid parameters are usually denoted as h_{11} , h_{12} , h_{21} , and h_{22} .)

This equivalent circuit is completely general for small-signal conditions. Given the proper values of the four parameters, the h -parameter model accounts for all of the secondary effects in the device. If the parameters are allowed to be complex-valued functions of frequency, the model is valid for all frequencies. However, the model parameters are related to the internal device physics in complex ways, so their variation with frequency is not easy to predict. Consequently, other models that are more closely related to the device physics are usually used for high-frequency analysis.

In terms of the h -parameters, the small-signal currents and voltages are related by

$$v_{be} = h_{ie}i_b + h_{re}v_{ce} \quad (8.39)$$

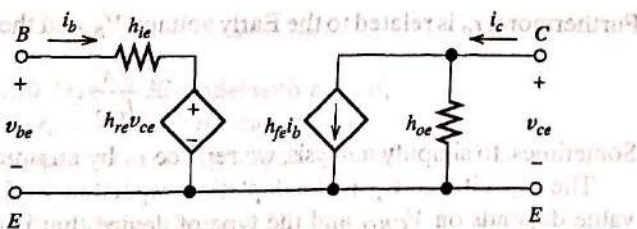
and

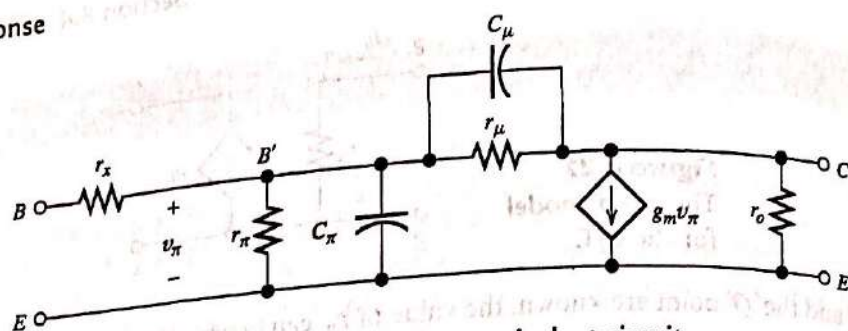
$$i_c = h_{fe}i_b + h_{oe}v_{ce} \quad (8.40)$$

Notice that h_{ie} has units of resistance, h_{re} and h_{fe} are unitless, and h_{oe} is a conductance.

We do not intend to make much use of the h -parameter equivalent circuit in design or analysis. However, data sheets sometimes contain information about the h -parameters. We have discussed them mainly so that you will be familiar with these parameters as you encounter them in the literature or on data sheets. For example, the data sheet for the 2N2222A in Appendix B gives values for the h -parameters at two operating points.

Figure 8.28
Common-emitter
 h -parameter small-
signal equivalent
circuit. (Note: h_{ie}
is resistance and h_{oe}
is conductance.)



Figure 8.29 Hybrid- π equivalent circuit.

The Hybrid- π Model

A very useful small-signal equivalent circuit for the BJT known as the **hybrid- π model** is shown in Figure 8.29. Motivated by the internal physics of the device, this model includes device capacitances and gives accurate results over a wide range of frequencies. We use the hybrid- π model for high-frequency analysis of BJT amplifiers later in this chapter. First, we discuss each of the parameters and see how to determine their values using information typically given on data sheets.

The resistance r_x , called the **base-spreading resistance**, accounts for the ohmic resistance of the base region. Typically, r_x is small compared with r_π , ranging from 10 to 100 Ω for small-signal devices. Its value is nearly independent of the operating point.

The resistance r_π represents the dynamic resistance of the base-emitter junction, as seen from the base terminal. It is the same as the r_π shown in Figure 8.27, and its value is given by Equation (8.38).

The resistance r_μ accounts for the effect of base-width modulation on the input characteristic. In other words, r_μ represents feedback from the collector to the base. In this sense, it plays essentially the same role that h_{re} does in the h -parameter equivalent circuit. The following approximate formula relates these parameters:

$$h_{re} = \frac{r_\pi}{r_\pi + r_\mu} \cong \frac{r_\pi}{r_\mu} \quad (8.41)$$

The value of r_μ is very large—several megohms is typical. To simplify analysis, we often replace r_μ by an open circuit. At high frequencies, this is justified even further because r_μ is shunted by the much lower impedance of C_μ .

The resistance r_o accounts (approximately) for the upward slope of the output characteristics of the transistor. Thus, it plays approximately the same role as h_{oe} of the h -parameter equivalent circuit. Thus, we can write

$$r_o \cong \frac{1}{h_{oe}} \quad (8.42)$$

Furthermore, r_o is related to the Early voltage V_A and the Q -point collector current I_{CQ} :

$$r_o \cong \frac{V_A}{I_{CQ}} \quad (8.43)$$

Sometimes, to simplify analysis, we replace r_o by an open circuit.

The capacitance C_μ is the depletion capacitance of the collector-base junction. Its value depends on V_{CBQ} and the type of device that is used. Values are often given on

data sheets as C_{obo} . (Unfortunately, the use of symbols is not standardized throughout the electronics community.) For example, the data sheet for the 2N2222A model lists a maximum C_{obo} of 8 pF for $V_{CBQ} = 10$ V.

Sometimes the time constant of the RC circuit between the collector and base terminals is given on the data sheet. For example, the data sheet for the 2N2222A gives this constant labeled as $r'_b C_c$. This time constant is approximately equal to $r_x C_\mu$. Assuming that C_μ is known, we can use the value given for the time constant to determine r_x .

The capacitance C_π accounts for the diffusion capacitance of the base-emitter junction. The value of C_π depends on the Q-point and the type of transistor. Values typically range from 10 pF to 1000 pF for small-signal devices.

Usually, data sheets do not give values for C_π directly. However, data sheets do generally give the **transition frequency** f_t , which is the frequency at which the common-emitter current gain magnitude $|I_c/I_b|$ is unity when the transistor is operated with an ac short circuit from collector to ground. The transition frequency is related to the hybrid- π parameters by the approximate formula

$$f_t \cong \frac{\beta}{2\pi r_\pi (C_\mu + C_\pi)} \quad (8.44)$$

The controlled source $g_m v_\pi$ shown in Figure 8.29 accounts for the amplification properties of the transistor. If we consider low-frequency operation, the capacitors become open circuits. Furthermore, as a reasonable approximation, we can replace r_x by a short circuit and replace r_μ and r_o by open circuits. The resulting circuit is illustrated in Figure 8.30. Comparing this with the r_π - β model displayed in Figure 8.27, we see that the input circuits both consist of a resistance r_π . The controlled sources must produce the same collector current. Therefore, we can write

$$g_m v_\pi = \beta i_b \quad (8.45)$$

Solving for g_m , we obtain

$$g_m = \beta (i_b / v_\pi) \quad (8.46)$$

However, $i_b / v_\pi = 1 / r_\pi$, so we have

$$g_m = \beta / r_\pi \quad (8.47)$$

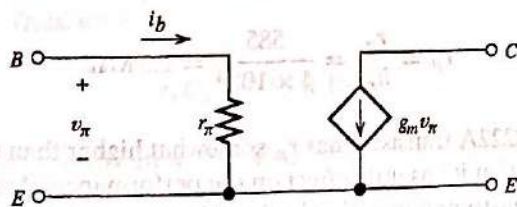


Figure 8.30 Hybrid- π model with $r_x = 0$, $r_\mu = \infty$, $r_o = \infty$, and the capacitors replaced by open circuits. This approximate low-frequency model is equivalent to the r_π - β model of Figure 8.27.

The hybrid- π model is useful in mathematical analysis of the high-frequency response of BJT amplifiers. The model parameters can often be calculated from the data published by manufacturers.

Using Equation (8.38) to substitute for r_π , we get

$$g_m = \frac{I_{CQ}}{V_T} \quad (8.48)$$

Thus, we can compute g_m from knowledge of the Q -point and temperature.

Example 8.7 Determining the Hybrid- π Parameters by Using the Data Sheet

Use the data sheet in Appendix B to determine values for the hybrid- π equivalent circuit for a typical 2N2222A transistor at a Q -point of $I_{CQ} = 10 \text{ mA}$ and $V_{CEQ} = 10 \text{ V}$. Assume that $V_T = 26 \text{ mV}$.

SOLUTION First, we use Equation (8.48) to compute the transconductance:

$$g_m = \frac{I_{CQ}}{V_T} = \frac{10 \text{ mA}}{26 \text{ mV}} = 0.385 \text{ S}$$

The range given on the data sheets for $\beta = h_{fe}$ at a bias point of $I_{CQ} = 10 \text{ mA}$ is 75 to 375. We will use the average value

$$\beta = \frac{375 + 75}{2} = 225$$

Then, using Equation (8.38), we have

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{225 \times 0.026}{0.01} = 585 \Omega$$

(The data sheet lists values for $h_{ie} = r_\pi$ ranging from 250 to 1250 Ω , which is fairly consistent with the value we have found.)

The data sheet gives a maximum value for h_{re} of 4×10^{-4} , which we use in computing r_μ . Equation (8.41) yields

$$r_\mu \cong \frac{r_\pi}{h_{re}} = \frac{585}{4 \times 10^{-4}} = 1.5 \text{ M}\Omega$$

The typical 2N2222A transistor has r_μ somewhat higher than this. In any case, the value is so high that it has little effect on the performance of most circuits. Almost certainly, the unit-to-unit variation in β will have a much larger effect. This is why, to simplify analysis, we often drop r_μ from the equivalent circuit.

We can use Equation (8.42) to find a value for r_o :

$$r_o \cong \frac{1}{h_{oe}}$$

The data sheet gives a range for h_{oe} from $25 \mu\text{S}$ to $200 \mu\text{S}$. Thus, r_o ranges from $5 \text{ k}\Omega$ to $40 \text{ k}\Omega$. We take

$$r_o = \frac{5 + 40}{2} = 22.5 \text{ k}\Omega$$

as a typical value.

For $V_{CB} = 10 \text{ V}$ and $I_{EQ} = 0$, the data sheet gives a maximum value of $C_{obo} = C_\mu$ of 8 pF . This is the depletion capacitance of the collector junction and is nearly independent of the emitter current. The capacitance does depend on V_{CBQ} , but the Q -point given in the statement of the problem yields

$$V_{CBQ} = V_{CEQ} - V_{BEQ} \cong 10 - 0.6 = 9.4 \text{ V}$$

which is very close to the data-sheet specification. As is often the case, no information is given concerning typical values of C_{obo} . Thus, we use the maximum value in the equivalent circuit:

$$C_\mu = 8 \text{ pF}$$

Next, we utilize the specification for the transition frequency f_t to determine a value for C_π . According to the data sheet, the minimum value of f_t is 300 MHz for $V_{CEQ} = 20 \text{ V}$ and $I_{CQ} = 20 \text{ mA}$. The transition frequency is a function of both V_{CEQ} and I_{CQ} , and the data sheet does not list any data for the bias point given in the problem statement. However, examination of data published for other similar transistors indicates that f_t should not vary by more than about 20%, due to the difference in Q -points. Therefore, we use $f_t = 300 \text{ MHz}$ in computing a value for C_π . Solving Equation (8.44) for C_π and substituting values, we find that

$$C_\pi \cong \frac{\beta}{2\pi r_\pi f_t} - C_\mu = \frac{225}{2\pi \times 585 \times 300 \times 10^6} - 8 \text{ pF}$$

$$C_\pi \cong 196 \text{ pF}$$

Finally, the data sheet gives a maximum value of 150 ps for the collector-base time constant. Thus, we have

$$r_x C_\mu = 150 \times 10^{-12}$$

Solving for r_x and substituting the value found for C_μ , we get

$$r_x = 19 \Omega$$

Thus, we have used the values published in the data sheet to find values for the parameters of the hybrid- π equivalent circuit. The circuit and values are shown in Figure 8.31. $\square$

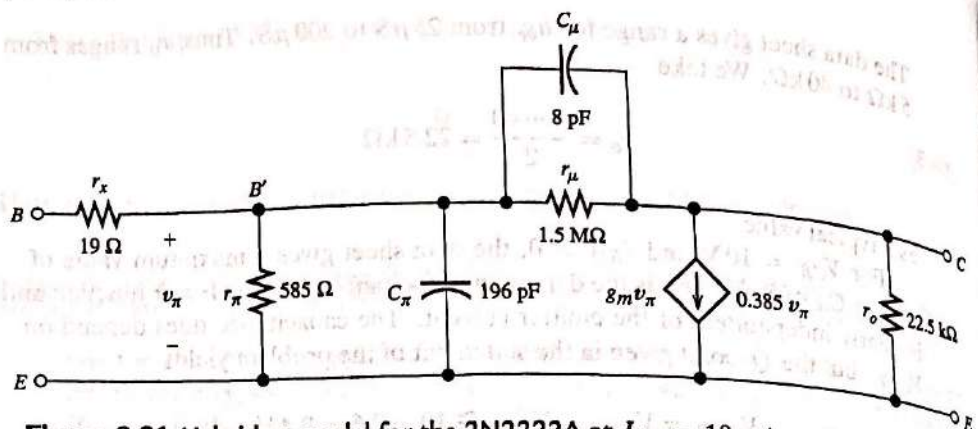


Figure 8.31 Hybrid- π model for the 2N2222A at $I_{CQ} = 10$ mA and $V_{CEQ} = 10$ V. For these values, $\beta \cong 225$.

As you can see, determining parameter values for a BJT model from the data sheet is not an exact science. Many parameters, such as β , show large unit-to-unit variations. Because we must design circuits that work with all of the devices of a given type, the exact model for a particular unit is not important. Often, we use the worst-case device specifications in finding a device model. If our circuit design meets its goals with a range of device model parameters, including the worst-case, we can be reasonably sure that the circuit can be mass produced with an acceptable rejection rate.

EXERCISE

8.9 Suppose that a certain transistor has $f_t = 500$ MHz, $\beta = 100$, and $C_\mu = 4$ pF. Assume that f_t , β , and C_μ are independent of I_{CQ} . (Actually, this is not true: In practice, f_t and β depend on I_{CQ} . However, the dependence is not strong. Assuming constant β and f_t is a reasonable first approximation, at least for a restricted range of currents.) Plot r_π , C_π , and g_m to scale against I_{CQ} . Use logarithmic scales for all axes. Allow I_{CQ} to range from 1 mA to 100 mA.

Answer See Figure 8.32.

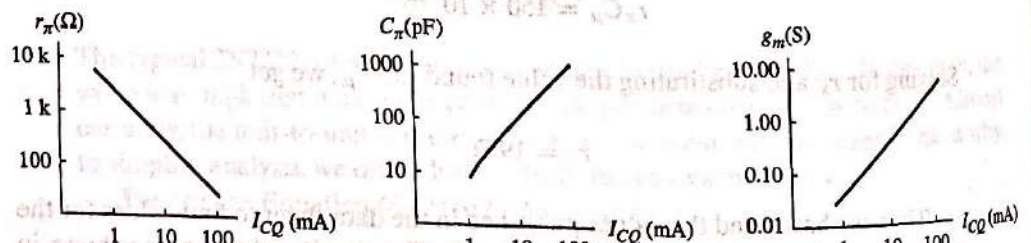


Figure 8.32 Answers to Exercise 8.9.

EXERCISE

8.10 Repeat Example 8.7 for $I_{CQ} = 1$ mA. Assume that $f_i = 90$ MHz at this bias point.

Answer $\beta = 175$; $g_m = 38.5$ mS; $r_\pi = 4.55$ k Ω ; $r_\mu = 5.7$ M Ω ; $r_o = 114$ k Ω ; $C_\mu = 8$ pF; $C_\pi = 60$ pF; $r_x = 19$ Ω .

8.5 COMMON-EMITTER AMPLIFIERS AT HIGH FREQUENCIES

We considered the midband operation of the common-emitter stage in Chapter 4. In this section, we extend our analysis to high frequencies.

The circuit diagram of a common-emitter amplifier is illustrated in Figure 8.33a. For manual analysis of high-frequency response, we use the hybrid- π equivalent circuit for the BJT. The small-signal equivalent circuit for the common-emitter amplifier is shown in Figure 8.33b. Because we are interested in high-frequency response, the coupling and bypass capacitors have been replaced by short circuits.

We could use this equivalent circuit to derive expressions for midband input impedance, midband voltage gain, and so forth. However, we have obtained these results in Section 4.7, based on a simpler transistor model. Our main interest at this time is the high-frequency behavior of the voltage gain $A_{vs} = V_o/V_s$. We anticipate that the gain magnitude declines at high frequencies due to the device capacitances C_π and C_μ .

We can gain better insight by simplifying the equivalent circuit. First, the value of r_μ is very large compared with the impedance of C_μ in the high-frequency range. (Values of the hybrid- π parameters for the 2N2222A BJT are shown in Figure 8.31.) Therefore, with small error, we can omit r_μ from the circuit. Next, we combine the resistances r_o , R_C , and R_L in parallel. We denote this parallel combination as

$$R'_L = R_L || R_C || r_o \quad (8.49)$$

(In Chapter 4, we neglected r_o , and R'_L was defined as the parallel combination of R_L and R_C .) Finally, we replace the signal source and the resistances on the left-hand side of the terminal b' by their Thévenin equivalent circuit. The Thévenin resistance is then

$$R'_s = r_\pi || [r_x + (R_B || R_s)] \quad (8.50)$$

where, as usual, we define

$$R_B = R_1 || R_2 \quad (8.51)$$

Making these changes simplifies the equivalent circuit, as shown in Figure 8.34.

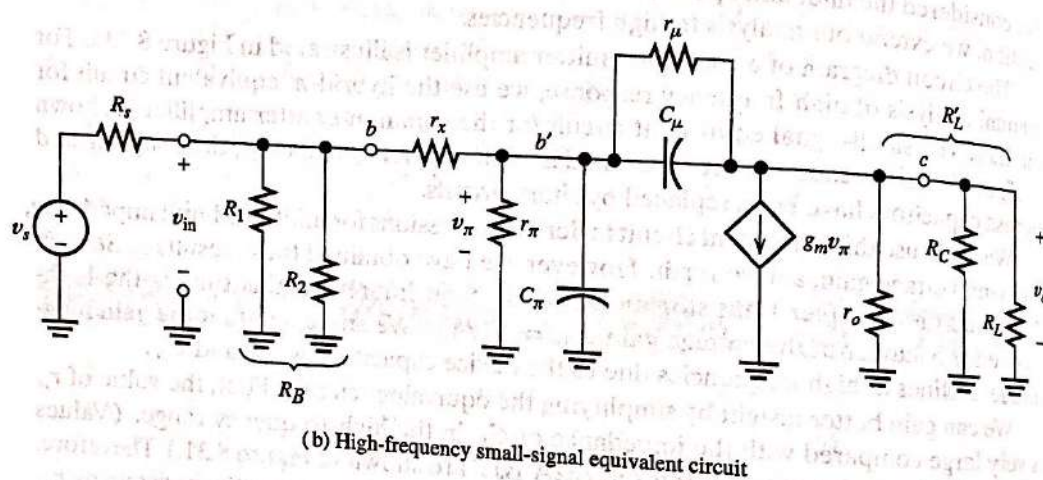
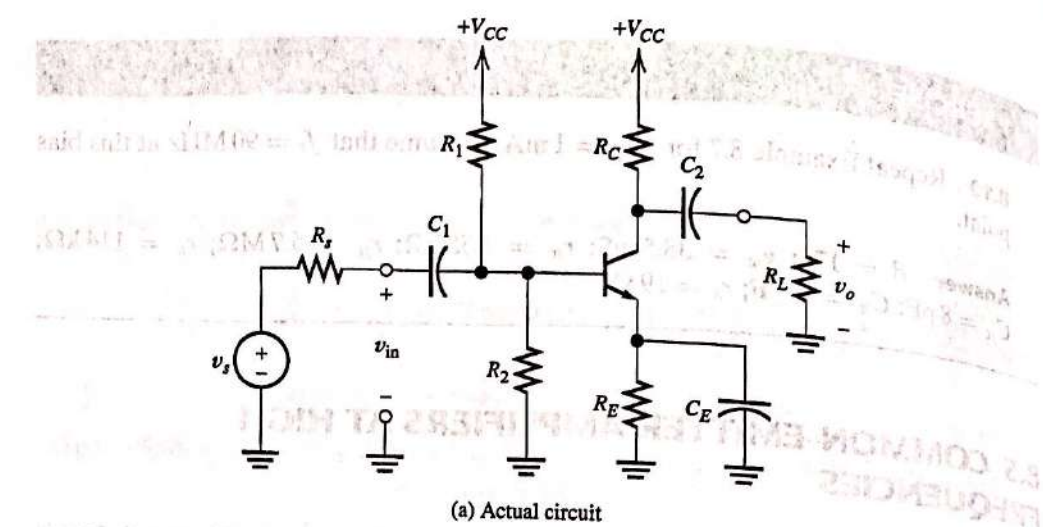


Figure 8.33 Common-emitter amplifier.

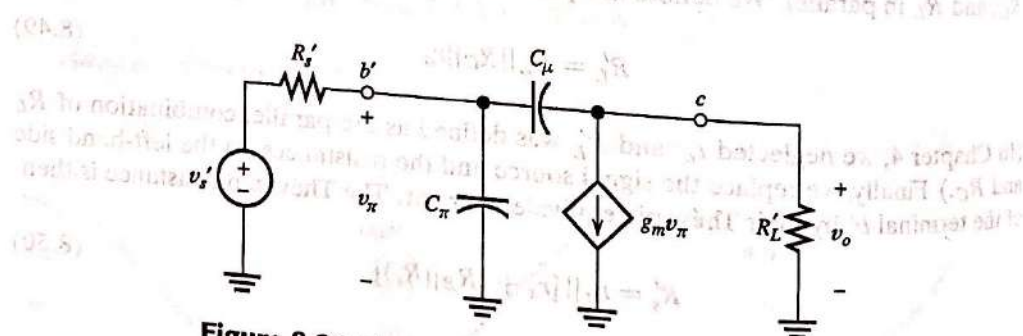


Figure 8.34 Equivalent circuit of Figure 8.33b after removing r_μ , replacing r_o , R_C , and R_L by their parallel equivalent, and replacing the circuit to the left-hand side of b' by its Thévenin equivalent.

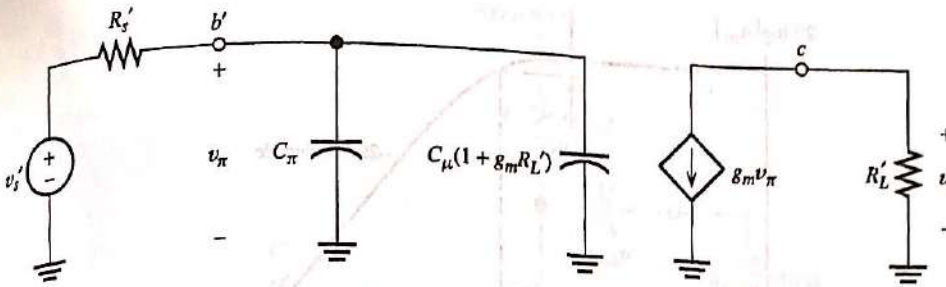


Figure 8.35 Simplified equivalent circuit for the common-emitter amplifier.

If we neglect the (small) current through C_μ , the output voltage in Figure 8.34 is

$$V_o = -g_m V_\pi R_L' \quad (8.52)$$

We can consider the part of the circuit on the right-hand side of terminal b' to form an amplifier with terminal b' as its input and terminal c as its output. The voltage gain of this amplifier is

$$A_{vb'} = \frac{V_o}{V_\pi} = -g_m R_L' \quad (8.53)$$

Notice that the capacitance C_μ is connected from the input terminal b' of this inverting amplifier to the output terminal c . In Section 8.3, we showed that, due to the Miller effect, connecting a capacitance C_f from the input terminal of an amplifier to the output terminal is equivalent to connecting a capacitance of $C_f(1 - A_v)$ across the input terminals. In this case, we have $C_f = C_\mu$ and $A_v = A_{vb'} = -g_m R_L'$. Thus, the capacitance C_μ can be replaced by a capacitance $C_\mu(1 + g_m R_L')$ connected from terminal b' to ground. This results in the simplified equivalent circuit illustrated in Figure 8.35.

We denote the total capacitance between terminal b' and ground of Figure 8.35 as

$$C_T = C_\pi + C_\mu(1 + g_m R_L') \quad (8.54)$$

Notice that the input circuit of Figure 8.35 forms a simple RC lowpass filter. The break frequency is

$$f_H = \frac{1}{2\pi R_s' C_T} \quad (8.55)$$

Above f_H , the gain of the amplifier rolls off at 20 dB per decade. A Bode plot of the magnitude of the gain in the high-frequency range is shown in Figure 8.36.

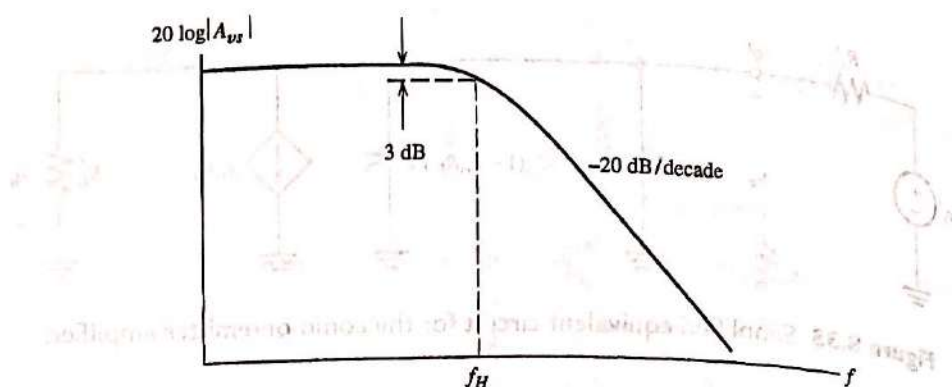


Figure 8.36 High-frequency behavior of the common-emitter amplifier.

Example 8.8 High-Frequency Response of the Common-Emitter Amplifier

Consider the common-emitter amplifier shown in Figure 8.37. Initially, we assume that $R_{E1} = 0$, and then this circuit has the same small-signal equivalent circuit as the circuit illustrated in Figure 8.33. It can be demonstrated that the Q -point is at approximately $I_{CQ} = 10$ mA and $V_{CEQ} = 10$ V. The values of the hybrid- π parameters for the transistor at this Q -point are shown in Figure 8.31. Use the results derived in this section to find the upper half-power frequency and the formulas of Chapter 4 to find the midband value for A_{vs} . Then, verify the results with SPICE. Finally, use SPICE to obtain a plot of the amplifier gain magnitude versus frequency for $R_{E1} = 24$ Ω .

SOLUTION As shown in Figure 8.31, the parameters for the hybrid- π equivalent circuit are

$$r_x = 19 \Omega$$

$$r_\pi = 585 \Omega$$

$$r_o = 22.5 \text{ k}\Omega$$

$$r_\mu = 1.5 \text{ M}\Omega$$

$$C_\pi = 196 \text{ pF}$$

$$C_\mu = 8 \text{ pF}$$

$$g_m = 0.385 \text{ S}$$

Substituting values into Equations (8.49) and (8.50) yields

$$R'_L = R_L || R_C || r_o = 510 || 510 || 22.5 \text{ k}\Omega = 252 \Omega$$

and

$$R'_s = r_\pi || [r_x + (R_B || R_s)] = 585 || [19 + (10 \text{ k}\Omega || 50)] \\ = 61.5 \Omega$$

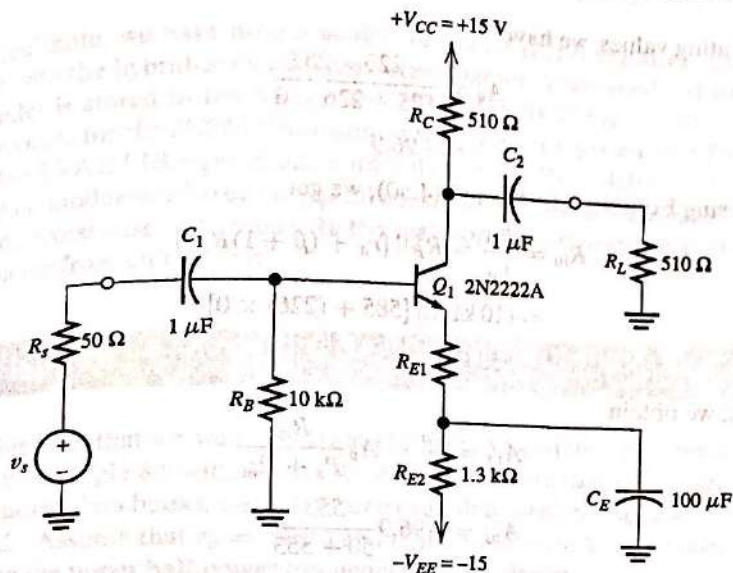


Figure 8.37 Circuit for Example 8.8.

Next, Equation (8.54) gives

$$\begin{aligned} C_T &= C_\pi + C_\mu(1 + g_m R'_L) \\ &= 196 + 8(1 + 0.385 \times 252) \\ &= 196 + 784 \\ &= 980 \text{ pF} \end{aligned}$$

Notice that the Miller effect causes the 8-pF capacitance C_μ to appear as a 784-pF capacitor in parallel with C_π . Thus, even though C_μ is much smaller than C_π , we see that C_μ has a greater effect in reducing gain at high frequencies.

Now we can compute the upper half-power frequency by using Equation (8.55):

$$\begin{aligned} f_H &= \frac{1}{2\pi R'_s C_T} \\ f_H &= \frac{1}{2\pi \times 61.5 \times 980 \times 10^{-12}} \\ f_H &= 2.64 \text{ MHz} \end{aligned}$$

Next, we use Equation (8.47) to compute β for this transistor:

$$\beta \cong r_\pi g_m = 585 \times 0.385 = 225$$

Now we employ Equation (4.47) to compute the midband gain:

$$A_v = \frac{v_o}{v_{in}} = \frac{-\beta R'_L}{r_\pi + (\beta + 1)R_{E1}}$$

Substituting values, we have

$$A_v = \frac{-225 \times 252}{585 + 226 \times 0} = -96.9$$

Also, using Equations (4.49) and (4.50), we get

$$\begin{aligned} R_{in} &= \frac{v_{in}}{i_{in}} = R_B || [r_\pi + (\beta + 1)R_{E1}] \\ &= (10 \text{ k}\Omega) || [585 + (226) \times 0] \\ &= 553 \Omega \end{aligned}$$

Finally, we obtain

$$\begin{aligned} A_{vs} &= \frac{v_o}{v_s} = A_v \frac{R_{in}}{R_s + R_{in}} \\ A_{vs} &= -96.9 \frac{553}{50 + 553} \\ A_{vs} &= -88.9 \end{aligned}$$

In decibels, the gain magnitude becomes

$$A_{vs} = 39.0 \text{ dB}$$

Next, we use PSpice to perform an ac analysis of the amplifier. The circuit schematic is stored in the file named Fig8.37. Bode magnitude plots for A_{vs} are illustrated in Figure 8.38. The PSpice analysis gives values for midband gain and the upper half-power frequency that are in very good agreement with the manual calculations for $R_{E1} = 0$. Notice that the bandwidth is increased, but that the midband gain is reduced, for $R_{E1} = 24 \Omega$.

The effect of C_μ on the high-frequency response of a high-gain common-emitter amplifier is greatly increased by the Miller effect. Bandwidth can be extended by reducing R_s or by reducing the midband gain (either by reducing R_L or adding a small unbypassed emitter resistance).

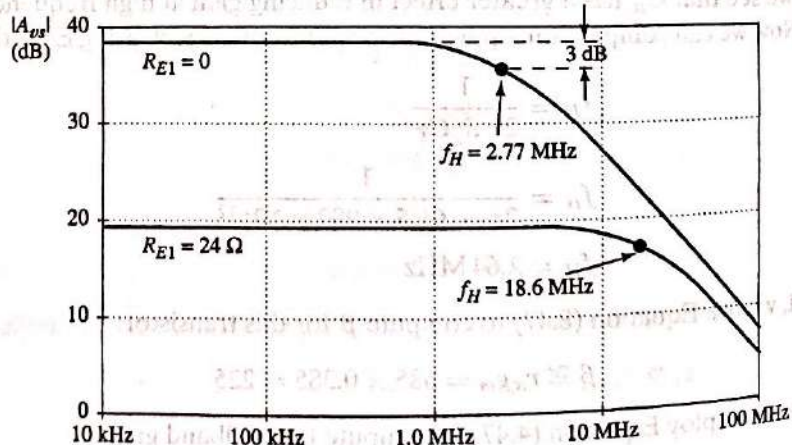


Figure 8.38 Gain magnitude versus frequency for the common-emitter amplifier of Example 8.8.

As a final note, we have used a model for the 2N2222A transistor that is in close agreement with the hybrid- π model parameters that we determined in Section 8.4. Our SPICE model is stored in the library file `DEVICE.LIB`. If the circuits are simulated using the models for the 2N2222 transistor in the libraries supplied with PSpice, such as `NOM.LIB` or `EVAL.LIB`, significantly different results will be obtained. This is due to the fact that some models are based on typical parameters from the data sheet, while others are based on worst-case parameters. In the real world, we can expect similar variations in performance from unit-to-unit.

EXERCISE

8.11 Suppose that we want to obtain the highest possible cutoff frequency for the circuit of Example 8.8 with $R_{E1} = 0$. We decide to try to select a better transistor. After studying data books, we select three candidates with the specifications shown in Table 8.2. Assume that $r_o = 20 \text{ k}\Omega$ and that $I_{CQ} \cong 10 \text{ mA}$ for all three transistors. Compute the upper half-power frequency for each device.

Answer (a) $f_H \cong 5.13 \text{ MHz}$; (b) $f_H \cong 8.33 \text{ MHz}$; (c) $f_H \cong 13.1 \text{ MHz}$.

Table 8.2. Device Specifications for Exercise 8.11.

Device	f_i (MHz)	C_μ (pF)	β	r_x (Ω)
(a)	400	5	100	10
(b)	350	2	100	15
(c)	500	2	50	5

EXERCISE

8.12 Use manual analysis to find the upper half-power frequency for $A_v = V_o/V_{in}$ in the circuit of Example 8.8 with $R_{E1} = 0$. (In Example 8.8, we found the upper half-power frequency for $A_{vs} = V_o/V_s$.) Use SPICE to check your answer. (Hint: If we assume that $R_s = 0$, then $v_{in} = v_s$. Thus, by substituting $R_s = 0$, the equations derived in this section can be used to find the upper half-power frequency for A_v .)

Answer By manual calculation, we obtain $f_H \cong 8.83 \text{ MHz}$. To check this value by using PSpice, run the program stored in the file named `Exer8.12`. From the simulation, we find that $f_H = 8.65 \text{ MHz}$, which is in good agreement with the manual computation.

8.6 COMMON-BASE, CASCODE, AND DIFFERENTIAL AMPLIFIERS

We have seen that the capacitance C_μ is an important factor in limiting the high-frequency response of the common-emitter amplifier because of the Miller effect. Thus, when we need an amplifier with wide bandwidth, we are led to consider amplifier configurations that do not have capacitance connected directly from the output to the input.

... when we need an amplifier with wide bandwidth, we are led to consider amplifier configurations that do not have capacitance connected directly from the output to the input.

The Common-Base Amplifier

One possibility is the common-base amplifier depicted in Figure 8.39a. The small-signal equivalent circuit is shown in Figure 8.39b. The base-spreading resistance r_x is small enough that terminal b' can be considered to be grounded. Thus, C_μ is connected from the output to ground, and C_π is connected from the input to ground. Except for stray wiring capacitance, there is no capacitance connected from the output directly to the input.

An approximate analysis of $A_{vs} = V_o/V_s$ can be carried out by replacing r_μ and r_o with open circuits and by replacing r_x with a short circuit. The resulting simplified equivalent circuit is illustrated in Figure 8.39c. Analysis of this circuit yields two break frequencies on the high end, which are given by the formulas

$$f_{H1} = \frac{1}{2\pi C_\pi R'_s} \quad (8.56)$$

and

$$f_{H2} = \frac{1}{2\pi C_\mu R'_L} \quad (8.57)$$

in which

$$R'_s = R_s || R_E || r_\pi || (1/g_m) \quad (8.58)$$

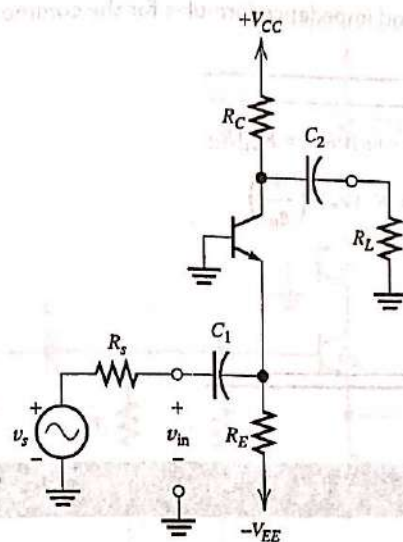
and

$$R'_L = R_C || R_L \quad (8.59)$$

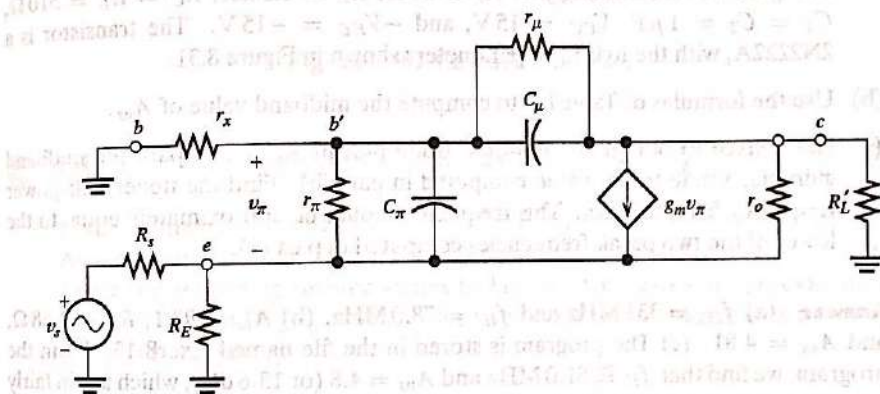
(According to this simplified analysis, A_{vs} eventually rolls off at 40 dB per decade.)

Typically, the break frequencies are much higher than those of the common-emitter amplifier, assuming similar devices and impedance levels.

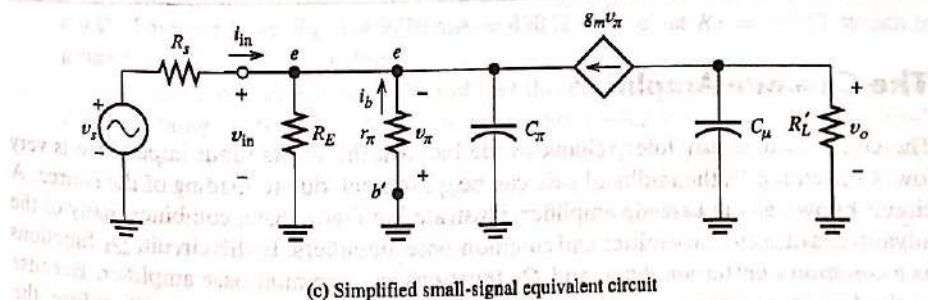
We obtain the midband equivalent circuit by replacing the capacitors in Figure 8.39c by open circuits. (The $g_m v_\pi$ controlled source can be labeled as βi_b if desired.) The midband gains and impedances of the common-base amplifier are given in Table 8.3. The common-base amplifier is noninverting and potentially has high voltage gain. The current gain is less than unity. The input impedance is low and the output impedance is moderate compared with other BJT amplifiers.



(a) Actual circuit



(b) Small-signal equivalent circuit



(c) Simplified small-signal equivalent circuit

Figure 8.39 Common-base amplifier.

Table 8.3. Midband gain and impedance formulas for the common-base amplifier shown in Figure 8.39.

$$\begin{aligned}
 A_v &= \frac{v_o}{v_{in}} = \frac{\beta R'_L}{r_\pi} = g_m R'_L \text{ in which } R'_L = R_L || R_C \\
 R_{in} &= \frac{v_{in}}{i_{in}} = R_E || \left(\frac{r_\pi}{\beta + 1} \right) = R_E || r_\pi || \left(\frac{1}{g_m} \right) \\
 R_o &= R_C \\
 A_i &= \frac{i_o}{i_{in}} = A_v \frac{R_{in}}{R_L} \\
 A_{vs} &= \frac{v_o}{v_s} = A_v \frac{R_{in}}{R_s + R_{in}}
 \end{aligned}$$

EXERCISE

- 8.13** (a) Compute the (high-end) break frequencies for the common-base amplifier of Figure 8.39a, assuming that $R_s = 50 \Omega$, $R_E = 1.3 \text{ k}\Omega$, $R_C = R_L = 510 \Omega$, $C_1 = C_2 = 1 \mu\text{F}$, $V_{CC} = 15 \text{ V}$, and $-V_{EE} = -15 \text{ V}$. The transistor is a 2N2222A, with the hybrid- π parameters shown in Figure 8.31.
- (b) Use the formulas of Table 8.3 to compute the midband value of A_{vs} .
- (c) Use PSpice to obtain a magnitude Bode plot of A_{vs} . Compare the midband gain magnitude to the value computed in part (b). Find the upper half-power frequency from the plot. This frequency should be approximately equal to the lower of the two break frequencies computed in part (a).

Answer (a) $f_{H1} = 331 \text{ MHz}$ and $f_{H2} = 78.0 \text{ MHz}$. (b) $A_{vs} = 98.1$, $R_{in} = 2.58 \Omega$, and $A_{vs} = 4.81$. (c) The program is stored in the file named Exer8.13. From the program, we find that $f_H \cong 51.0 \text{ MHz}$ and $A_{vs} = 4.8$ (or 13.6 dB), which are in fairly good agreement with the values computed in part (b) considering the wide tolerances of the BJT parameters.

The Cascode Amplifier

The common-base amplifier achieves wide bandwidth, but its input impedance is very low. Consequently, the midband gain can be quite small due to loading of the source. A circuit known as the **cascode** amplifier, illustrated in Figure 8.40, combines many of the advantages of common-emitter and common-base amplifiers. In this circuit, Q_1 functions as a common-emitter amplifier, and Q_2 functions as a common-base amplifier. Because of the low input impedance of Q_2 , the voltage gain of Q_1 is very low. Therefore, the Miller effect on C_μ of Q_1 is slight, and the bandwidth is wider than for a high-gain common-emitter stage.

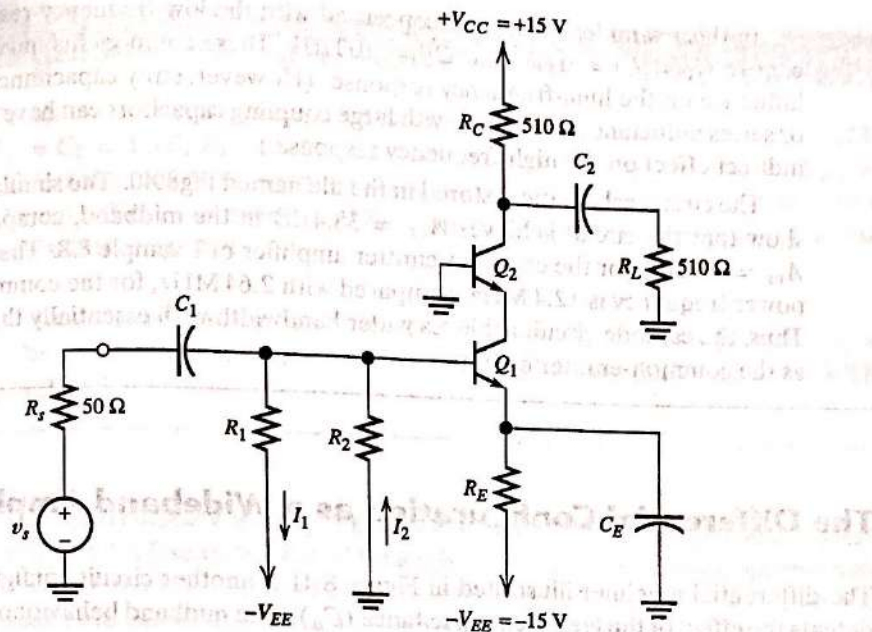


Figure 8.40 Cascode amplifier.

Example 8.9 SPICE Analysis of a Cascode Amplifier

Consider the cascode circuit using the 2N2222A transistor shown in Figure 8.40. Assume that $\beta = 225$, $R_C = R_L = 510\ \Omega$, $V_{CC} = 15\text{ V}$, and $-V_{EE} = -15\text{ V}$. Select the remaining resistor values to bias the transistors at approximately $I_{CQ} = 10\text{ mA}$ and $V_{CEQ} = 10\text{ V}$. Use PSpice to find the midband gain and upper half-power frequency.

SOLUTION A total voltage of 30 V is available. The dc voltage drop across R_C is $(10\text{ mA}) \times (510\ \Omega) = 5.1\text{ V}$. Furthermore, a voltage of 20 V is required to be dropped across the transistors. Therefore, the voltage across R_E is approximately 4.9 V. Thus, we have $R_E \cong 4.9/10\text{ mA} = 490\ \Omega$. We select $R_E = 510\ \Omega$, which is a standard 5%-tolerance value.

Assuming that $V_{BEQ1} = 0.7\text{ V}$ and that there is a 5-V drop across R_E , we find that the voltage at the base of Q_1 is approximately -9.3 V with respect to ground.

As shown in Figure 8.40, I_2 is the current through R_2 . For good bias stability, we should have $I_2 \gg I_{BQ1}$. The value of R_2 must not be so large that this requirement is not met. On the other hand, R_2 should not be so small that I_2 presents an undue load on the power supply. Somewhat arbitrarily, we choose $R_2 = 10\text{ k}\Omega$. Then the current through R_2 is $I_2 = (9.3\text{ V})/(10\text{ k}\Omega) = 0.93\text{ mA}$.

The current through R_1 is $I_1 = I_2 - I_{BQ1} = 0.93 - 10/225 = 0.89\text{ mA}$. Furthermore, the voltage across R_1 is 5.7 V, and we compute $R_1 = (5.7\text{ V})/(0.89\text{ mA}) = 6.40\text{ k}\Omega$. Thus, we choose the standard value $R_1 = 6.8\text{ k}\Omega$.

In this example, we are not concerned with the low-frequency response. We choose $C_1 = C_2 = 1\ \mu\text{F}$ and $C_E = 100\ \mu\text{F}$. These components have no direct influence on the high-frequency response. (However, stray capacitance to ground or series inductance associated with large coupling capacitors can have a significant indirect effect on the high-frequency response.)

The circuit schematic is stored in the file named Fig8_40. The simulation results show that the circuit achieves $A_{v_s} = 38.4\ \text{dB}$ in the midband, compared with $A_{v_s} = 39.0\ \text{dB}$ for the common-emitter amplifier of Example 8.8. The upper half-power frequency is $12.4\ \text{MHz}$, compared with $2.64\ \text{MHz}$, for the common-emitter. Thus, the cascode circuit achieves wider bandwidth with essentially the same gain as the common-emitter circuit.

The Differential Configuration as a Wideband Amplifier

Some amplifier configurations that have improved high-frequency performance compared with the common-emitter stage are the common base, the cascode connection, and the emitter-coupled differential pair. FET versions of these circuits are also useful.

The differential amplifier illustrated in Figure 8.41 is another circuit configuration that defeats the effect of the feedback capacitance (C_μ). The midband behavior of this circuit was considered in Chapter 7.

Notice that the single-ended output is taken from the collector of Q_2 . Because the base of Q_2 is grounded, feedback through C_μ of Q_2 is virtually eliminated. [This circuit can also be viewed as an emitter follower (Q_1) cascaded with a common-base amplifier (Q_2).]

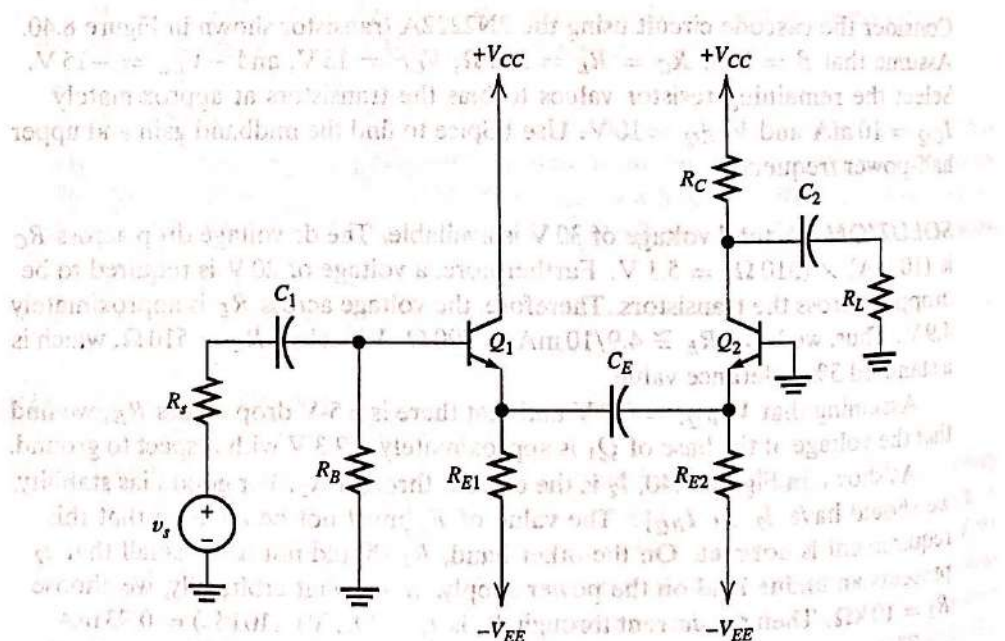


Figure 8.41 Emitter-coupled differential pair as a wideband amplifier.

EXERCISE

8.14 Consider the circuit of Figure 8.41 using the 2N2222A. Assume that $\beta = 225$, $C_1 = C_E = C_2 = 1 \mu\text{F}$, $R_s = 50 \Omega$, $R_C = R_L = 510 \Omega$, $V_{CC} = 15 \text{ V}$, and $-V_{EE} = -15 \text{ V}$. Select the remaining resistor values to bias the transistors at approximately $I_{CQ} = 10 \text{ mA}$. Write and execute a PSpice program to find the midband gain and upper half-power frequency.

Answer Suitable component values are $R_B = 10 \text{ k}\Omega$, $R_{E1} = 1.3 \text{ k}\Omega$, and $R_{E2} = 1.3 \text{ k}\Omega$. The program is stored in the file named Exer8.14 and yields $f_H = 9.7 \text{ MHz}$ and $A_{vs} = 33.3 \text{ dB}$.

It is interesting to compare the upper half-power frequencies for the circuits of Exercise 8.13, Exercise 8.14, Example 8.8, and Example 8.9. The type of device, approximate operating point, source resistance, and load resistance are the same for all of the circuits. The results are shown in Table 8.4. Depending on our requirements for gain and bandwidth, we could select the best configuration from this list. Of course, the best configuration depends on many factors, such as the source resistance, type of device, power-supply voltages, and so forth. In a given design, we consider several alternatives and select the best one.

Table 8.4. Performance Comparisons for Various Amplifier Configurations.

	Configuration	$A_{vs} \text{ (dB)}$	$f_H \text{ (MHz)}$
Example 8.8	Common emitter ($R_{E1} = 0$)	38.6	2.8
Example 8.8	Common emitter ($R_{E1} = 24 \Omega$)	19.4	18.6
Exercise 8.13	Common base	13.6	51.0
Example 8.9	Cascode	38.4	12.4
Exercise 8.14	Emitter-coupled differential	33.3	9.7

8.7 EMITTER FOLLOWERS

An emitter follower is useful for obtaining high input impedance or low output impedance. However, the voltage gain of the emitter follower is less than unity. If a voltage gain magnitude greater than unity is required, one of the amplifiers discussed in the previous section can be used in cascade with the emitter follower.

An emitter follower is displayed in Figure 8.42a. The high-frequency small-signal equivalent circuit is shown in Figure 8.42b. We derive an approximate expression for the upper half-power frequency of this circuit.

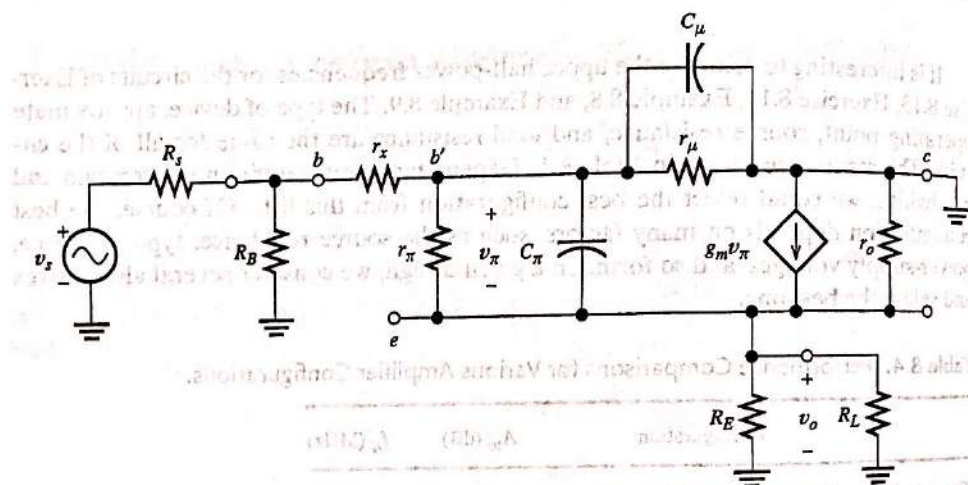
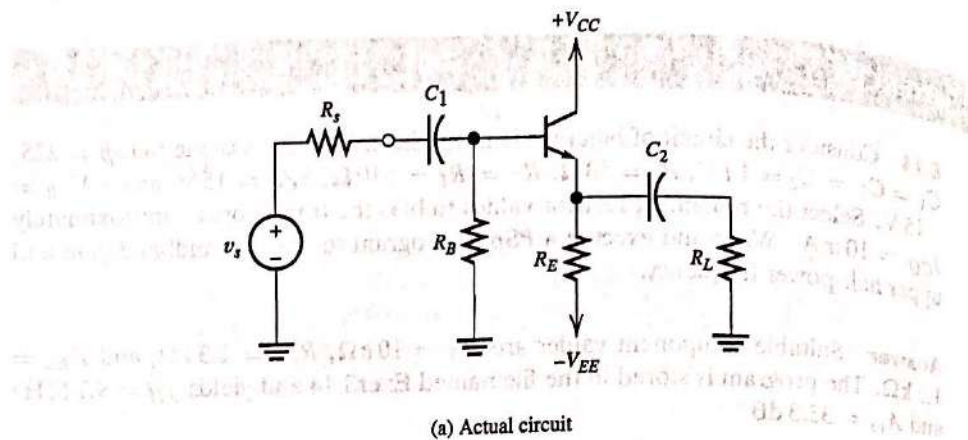


Figure 8.42 The emitter follower.

First, we simplify the circuit. We replace r_{μ} by an open circuit because the impedance of C_{μ} is much smaller than r_{μ} in the high-frequency range. The resistances r_o , R_E , and R_L are in parallel and can be represented by a single resistance

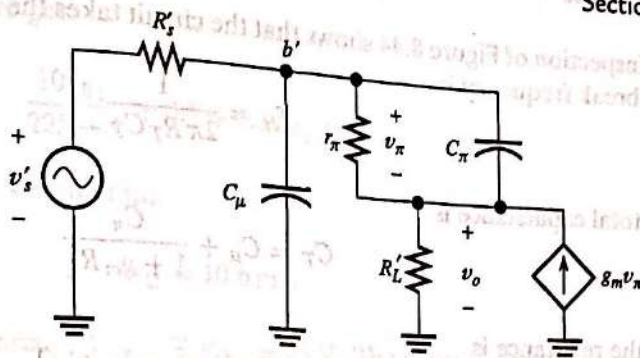
$$R'_L = r_o \parallel R_E \parallel R_L \quad (8.60)$$

Furthermore, the source, the resistance R_B , and the resistance r_x can be represented by a Thévenin equivalent circuit. The Thévenin resistance is

$$R'_s = r_x + (R_s \parallel R_B) \quad (8.61)$$

Making these changes results in the simplified equivalent circuit illustrated in Figure 8.43.

Figure 8.43
Simplified equivalent circuit for the emitter follower.



In the useful frequency range, the currents through r_π and C_π are small compared with the current of the controlled source. Therefore, the output voltage is approximately

$$v_o = g_m R'_L v_\pi \quad (8.62)$$

The voltage at terminal b' is

$$v_{b'} = v_\pi + v_o \quad (8.63)$$

Using Equation (8.62) to substitute for v_o in Equation (8.63), we obtain

$$v_{b'} = v_\pi + g_m R'_L v_\pi \quad (8.64)$$

Dividing the respective sides of Equations (8.62) and (8.64), we obtain the following expression for the voltage gain from point b' to the output:

$$A_{vb'} = \frac{v_o}{v_{b'}} = \frac{g_m R'_L}{1 + g_m R'_L} \quad (8.65)$$

Now we make use of the fact that r_π and C_π are connected from the input terminal b' to the output. According to the Miller effect, r_π and C_π can be replaced by equivalent components connected from terminal b' to ground. The resistance is divided by the factor

$$1 - A_{vb'} = \frac{1}{1 + g_m R'_L}$$

Similarly, C_π is multiplied by this factor. The resulting circuit is shown in Figure 8.44.

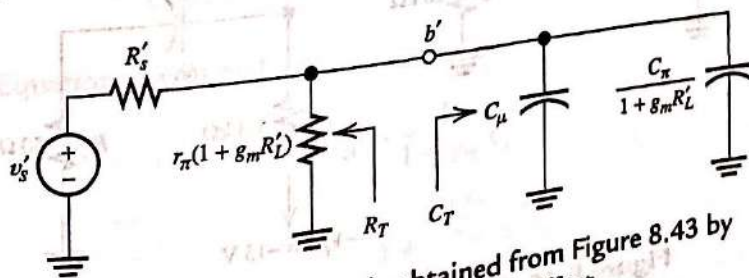


Figure 8.44 This circuit is obtained from Figure 8.43 by consideration of the Miller effect.

Inspection of Figure 8.44 shows that the circuit takes the form of a lowpass RC filter. The break frequency is

$$f_H = \frac{1}{2\pi R_T C_T} \quad (8.66)$$

The total capacitance is

$$C_T = C_\mu + \frac{C_\pi}{1 + g_m R'_L} \quad (8.67)$$

and the resistance is

$$R_T = R'_s \parallel [r_\pi (1 + g_m R'_L)] \quad (8.68)$$

Using Equation (8.61) to substitute for R'_s , we have

$$R_T = [r_x + (R_s \parallel R_B)] \parallel [r_\pi (1 + g_m R'_L)] \quad (8.69)$$

Example 8.10 High-Frequency Response of an Emitter Follower

Compute the upper half-power frequency of A_{vs} for the emitter follower illustrated in Figure 8.45. Assume that $\beta = 225$ for the 2N2222A transistor. Also, use the formulas from Section 4.8 to compute the midband values for input resistance, output resistance, and A_{vs} . Finally, use PSpice to check the results.

SOLUTION First, we find the bias point. The dc base current is $I_{EQ}/(\beta + 1)$ and flows through R_B . Writing a voltage equation around the loop containing R_B , the base-emitter junction, and R_E , we obtain

$$\frac{R_B I_{EQ}}{\beta + 1} + V_{BEQ} + R_E I_{EQ} = V_{EE}$$

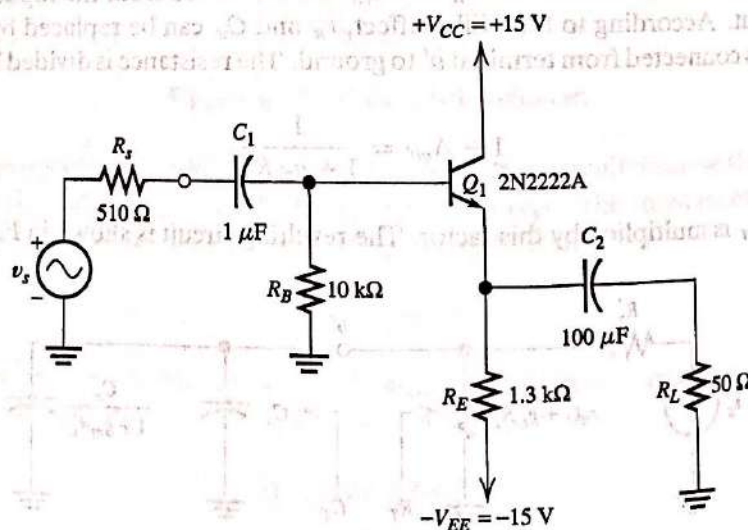


Figure 8.45 Emitter follower of Example 8.10.

Substituting values, we get

$$\frac{10I_{EQ}}{225 + 1} + 0.7 + 1.3I_{EQ} = 15$$

Solving the equation, we find that

$$I_{EQ} = 10.6 \text{ mA}$$

Furthermore, in this circuit, $V_{CEQ} \cong V_{CC} = 15 \text{ V}$. The hybrid- π equivalent circuit for the 2N2222A transistor at (approximately) this operating point is shown in Figure 8.31. The values of the hybrid- π parameters are as follows:

$$r_x = 19 \Omega$$

$$r_\pi = 585 \Omega$$

$$r_o = 22.5 \text{ k}\Omega$$

$$r_\mu = 1.5 \text{ M}\Omega$$

$$C_\pi = 196 \text{ pF}$$

$$C_\mu = 8 \text{ pF}$$

$$g_m = 0.385 \text{ S}$$

Now, from Equation (8.60), we have

$$\begin{aligned} R'_L &= r_o \parallel R_E \parallel R_L \\ &= 22.5 \text{ k}\Omega \parallel 1.3 \text{ k}\Omega \parallel 50 \Omega \\ &= 48.0 \Omega \end{aligned}$$

Equation (8.69) yields

$$\begin{aligned} R_T &= [r_x + (R_s \parallel R_B)] \parallel [r_\pi(1 + g_m R'_L)] \\ &= [19 + (510 \parallel 10 \text{ k}\Omega)] \parallel [585(1 + 0.385 \times 48)] \\ &= 483 \Omega \end{aligned}$$

From Equation (8.67), we have

$$\begin{aligned} C_T &= C_\mu + \frac{C_\pi}{1 + g_m R'_L} \\ &= 8 + \frac{196}{1 + 0.385 \times 48} \\ &= 18.1 \text{ pF} \end{aligned}$$

Finally, Equation (8.66) gives the break frequency

$$\begin{aligned} f_H &= \frac{1}{2\pi R_T C_T} \\ &= \frac{1}{2\pi 483 \times 18.1 \text{ pF}} \\ &= 18.2 \text{ MHz} \end{aligned}$$

Next, we use the formulas from Section 4.8 to compute the midband gain:

$$A_v = \frac{v_o}{v_{in}} = \frac{(\beta + 1)R'_L}{r_\pi + (\beta + 1)R'_L} = 0.949$$

$$R_{in} = \frac{v_{in}}{i_{in}} = R_B \parallel [r_\pi + (\beta + 1)R'_L] = 5.33 \text{ k}\Omega$$

$$A_{vs} = \frac{v_o}{v_s} = A_v \frac{R_{in}}{R_s + R_{in}} = 0.866$$

In decibels, we have $A_{vs} = -1.25 \text{ dB}$.

The circuit schematic is stored in the file named Fig8.45. We can obtain a plot of A_{vs} versus frequency by simulating the circuit and using Probe. The plot shows that the midband gain is -1.3 dB and the upper half-power frequency is 18.9 MHz . These values are close to the values obtained by the manual analysis. $\square$

Manual Analysis Versus SPICE Analysis

... in performing a manual analysis, one often gains a much better understanding of performance-limiting factors.

As usual, we find that the SPICE program gives answers for a particular circuit with very little effort. However, in performing a manual analysis, one often gains a much better understanding of performance-limiting factors. For example, in computing C_T for the emitter follower in Example 8.10, we find that the contributions from C_μ and C_π are roughly equal. Thus, if we wanted to increase the bandwidth of the circuit, we could look for a transistor having either a lower C_μ or a higher f_t (which implies a lower C_π).

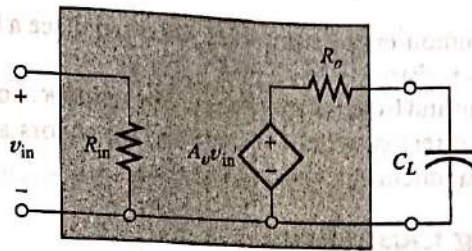
In other circuits, one of the capacitances can have the dominant effect in limiting bandwidth. For example, in a common-emitter amplifier with high gain magnitude, C_μ is more important than C_π . To increase the bandwidth of a common-emitter amplifier, we look for a transistor with a lower C_μ , and the value of f_t is less important. This is the type of insight afforded by manual analysis that SPICE does not readily provide.

Often, manual analysis using simplifying approximations provides a clearer understanding than either an exact theoretical development or a computer simulation.

Capacitive Loads

In some applications, the load is capacitive. The impedance of a capacitive load decreases with frequency, eventually causing gain to drop off. One example is a control grid of a television picture tube, which typically presents a load of 30 pF to the video amplifier.

Figure 8.46
The load capacitance C_L and the output resistance R_o form a low-pass filter.



Other examples are piezoelectric transducers and electrostatic loudspeakers, which can have capacitances of several thousand picofarads.

As shown in Figure 8.46, the output resistance of the amplifier and the capacitive load form a lowpass filter. The break frequency of the filter is

$$f_H = \frac{1}{2\pi R_o C_L} \quad (8.70)$$

Thus, to obtain a wide bandwidth with a large capacitive load, the amplifier should have low output impedance. This can best be achieved by using an emitter follower as the output stage.

When the load is a capacitance and extended high-frequency response is needed, a good choice for the output stage is the emitter follower, because it tends to have low output impedance.

EXERCISE

8.15 Suppose that we want to design a multistage amplifier. The load is a capacitance of $C_L = 400$ pF, and we want an upper half-power frequency of at least 5 MHz. What is the restriction on the output resistance of the amplifier? What configuration should we select for the output stage?

Answer The output resistance must be less than 79.6Ω . An emitter follower would be the best choice to achieve this relatively low output resistance.

8.8 LOW-FREQUENCY RESPONSE OF RC-COUPLED AMPLIFIERS

In this section, we will see that coupling and bypass capacitors cause the gain of RC-coupled amplifiers to decline, as the frequency is reduced below a certain value that depends on the component values and the configuration of the circuit under consideration.

The purpose of coupling capacitors is to prevent dc currents from flowing, while allowing ac signals to pass. In some applications, the signal source contains a large dc component that is not of interest, and we use a coupling capacitor to prevent the dc component from entering the amplifier. Also, in discrete amplifiers, we can use coupling capacitors between stages so that the bias points of the active devices can be set independently. An output coupling capacitor is useful when the output contains a dc bias voltage that we do not want to apply to the load. Bypass capacitors are used to provide a low impedance path in parallel with bias resistors for ac signal currents. For example, in a

discrete common-emitter amplifier, we often place a bypass capacitor in parallel with the emitter bias resistor.

Coupling and bypass capacitors are not practical on IC chips. Therefore, IC amplifiers are usually direct coupled. If coupling capacitors are necessary, they are provided as discrete components external to the chip.

Coupling Capacitors

First, we examine the effects of coupling capacitors. Consider the source, amplifier, and load illustrated in Figure 8.47. The source consists of V_s and the internal resistance R_s . The amplifier input resistance is R_{in} , the amplifier output resistance is R_o , and the load is R_L . The capacitor C_1 couples the source to the input of the amplifier, and C_2 couples the output signal to the load.

The overall voltage gain of the amplifier shown in Figure 8.47 is

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_x}{V_s} \times \frac{V_y}{V_x} \times \frac{V_o}{V_y} \quad (8.71)$$

In Example 8.2, we considered a circuit similar to the input circuit of Figure 8.47 (consisting of R_s , C_1 , and R_{in}), except that the components were labeled as R_1 instead of R_s , R_2 instead of R_{in} , and C instead of C_1 . The transfer function of the input circuit is given by Equation (8.23)—if the symbols representing the components are changed. Thus, we have

$$\frac{V_x}{V_s} = \frac{R_{in}}{R_s + R_{in}} \times \frac{j(f/f_1)}{1 + j(f/f_1)} \quad (8.72)$$

in which we have denoted the break frequency as f_1 . This frequency is given by Equation (8.22). With changes in notation to fit the present case, we have

$$f_1 = \frac{1}{2\pi(R_s + R_{in})C_1} \quad (8.73)$$

The output circuit of Figure 8.47 (consisting of R_o , C_2 , and R_L) also has the same configuration as the circuit of Example 8.2. Making the appropriate changes in notation in Equations (8.22) and (8.23), yields

$$\frac{V_o}{V_y} = \frac{R_L}{R_o + R_L} \times \frac{j(f/f_2)}{1 + j(f/f_2)} \quad (8.74)$$

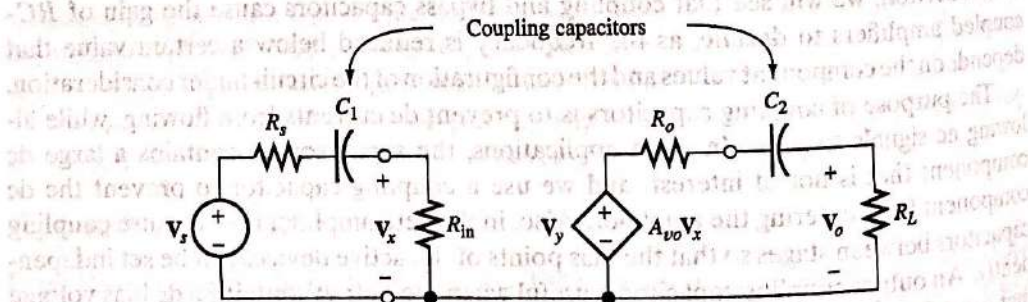


Figure 8.47 Amplifier with coupling capacitors.

and

$$f_2 = \frac{1}{2\pi(R_o + R_L)C_2} \quad (8.75)$$

The ratio of V_y to V_x is the open-circuit voltage gain of the amplifier:

$$A_{vo} = \frac{V_y}{V_x} \quad (8.76)$$

The following expression for the gain of the amplifier results from using Equations (8.72), (8.74), and (8.76) to make substitutions in Equation (8.71):

$$A_{vs} = \frac{R_{in}}{R_s + R_{in}} \times \frac{j(f/f_1)}{1 + j(f/f_1)} \times A_{vo} \times \frac{R_L}{R_o + R_L} \times \frac{j(f/f_2)}{1 + j(f/f_2)}$$

Let us define the midband gain as

$$A_{vsmid} = \frac{R_{in}}{R_s + R_{in}} \times A_{vo} \times \frac{R_L}{R_o + R_L} \quad (8.77)$$

Then the amplifier gain can be written as

$$A_{vs} = A_{vsmid} \times \frac{j(f/f_1)}{1 + j(f/f_1)} \times \frac{j(f/f_2)}{1 + j(f/f_2)} \quad (8.78)$$

Notice that A_{vsmid} is the voltage gain of the amplifier at midband frequencies for which the coupling capacitors can be treated as short circuits.

As we have seen in Example 8.2, the term

$$\frac{j(f/f_1)}{1 + j(f/f_1)}$$

contributes a 20-dB-per-decade roll-off for frequencies below the break frequency f_1 . This was illustrated in Figure 8.12. Similarly, the term

$$\frac{j(f/f_2)}{1 + j(f/f_2)}$$

contributes a 20-dB-per-decade roll-off for frequencies below f_2 .

A magnitude Bode plot of the voltage gain for the amplifier of Figure 8.47 is displayed in Figure 8.48. For illustration, we have assumed that f_2 is less than f_1 . For frequencies below f_2 , the slope of the roll-off is 40 dB per decade.

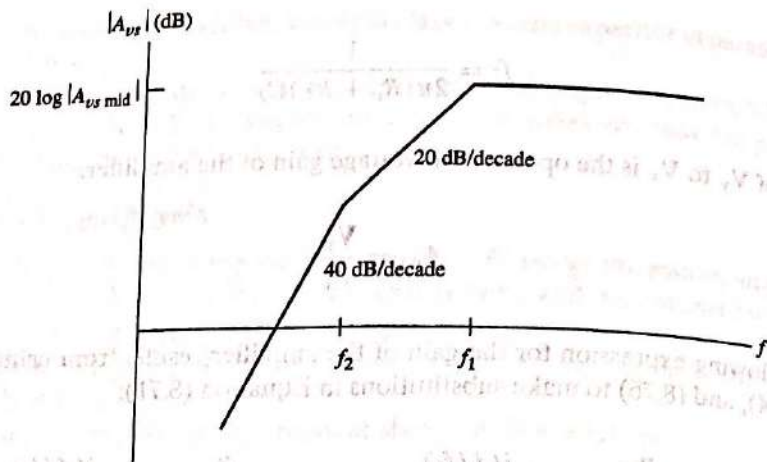


Figure 8.48 Magnitude Bode plot for the amplifier of Figure 8.47.

(We have assumed that $f_1 > f_2$.)

To obtain the magnitude Bode plot of a capacitively coupled amplifier, we need to find only the midband gain and the values of the break frequencies. Above the highest break frequency, the gain is constant. As we go lower in frequency, each break contributes 20 dB per decade to the slope of the roll-off. The midband gain is found by analyzing the circuit under the assumption that the coupling capacitors are short circuits.

For the circuit of Figure 8.47, the break frequencies are given by Equations (8.73) and (8.75). Notice that the break-frequency expressions are of the form

$$f_p = \frac{1}{2\pi(R_1 + R_2)C} \quad (8.79)$$

in which $R_1 + R_2$ is the total resistance in series with the coupling capacitor.

To summarize, the steps in analyzing the low-frequency response of a capacitively coupled amplifier similar to Figure 8.47 are as follows:

1. Analyze the circuit to find the midband gain, assuming that the coupling capacitors are shorts.
2. Determine the total resistance in series with each capacitor.
3. Calculate the break frequency for each coupling capacitor.
4. Draw the Bode plot of the amplifier gain.

Example 8.11 Low-Frequency Analysis of a Circuit with Coupling Capacitors

Draw the asymptotic magnitude Bode plot for $A_{vs} = V_o/V_s$ of the amplifier shown in Figure 8.49. Assume that the op amp is ideal.

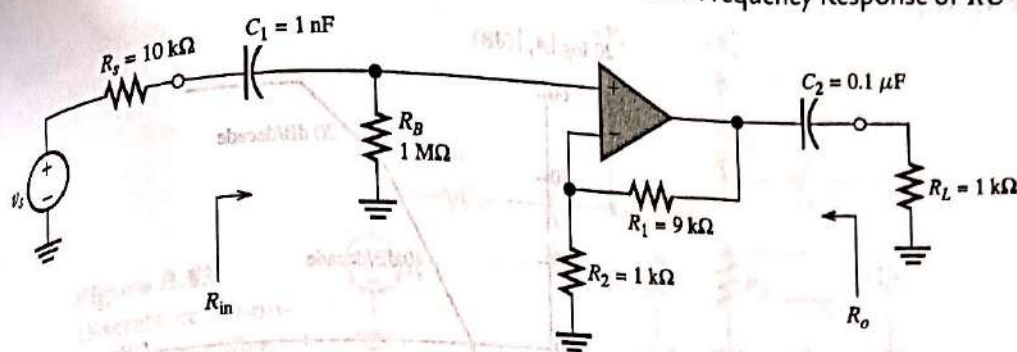


Figure 8.49 Amplifier of Example 8.11.

SOLUTION Assuming that the coupling capacitors are short circuits, we can use the op-amp principles from Chapter 2 to establish that

$$R_{in} = R_B = 1 \text{ M}\Omega$$

$$A_{vs\text{mid}} = 9.9 = 19.9 \text{ dB}$$

$$R_o = 0$$

Then, using Equations (8.73) and (8.75), we compute the break frequencies:

$$f_1 = \frac{1}{2\pi(R_s + R_{in})C_1} = \frac{1}{2\pi(10^4 + 10^6)10^{-9}} = 157.6 \text{ Hz}$$

$$f_2 = \frac{1}{2\pi(R_o + R_L)C_2} = \frac{1}{2\pi(0 + 10^3)10^{-7}} = 1592 \text{ Hz}$$

The asymptotic Bode plot for A_{vs} is illustrated in Figure 8.50.

Each coupling capacitor in an RC-coupled amplifier contributes a 20-dB-per-decade decline in gain at low frequencies. The break frequency for each capacitor is $f_{\text{break}} = 1/(2\pi RC)$, where R is the total equivalent resistance in series with the capacitor.

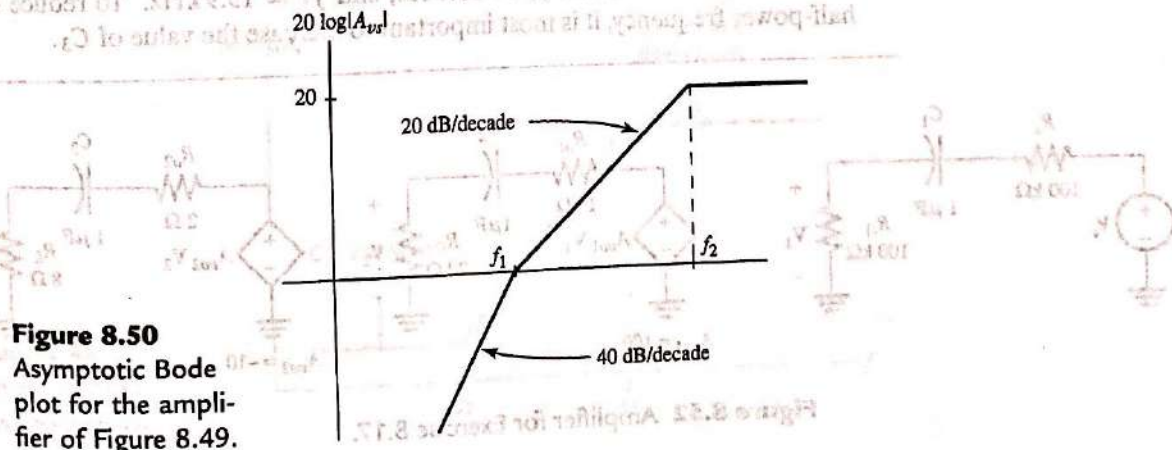


Figure 8.50 Asymptotic Bode plot for the amplifier of Figure 8.49.

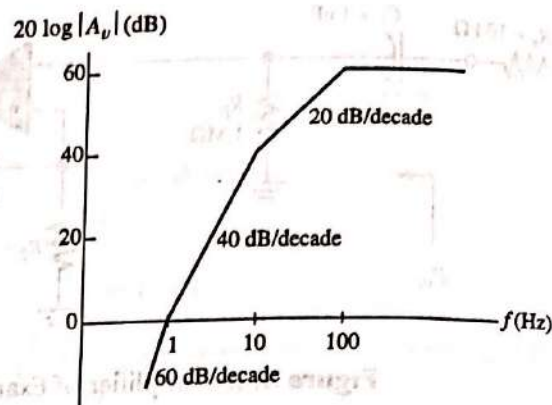


Figure 8.51
Answer for Exercise 8.16.

EXERCISE

8.16 A certain capacitively coupled amplifier has a midband gain of 1000. Three coupling capacitors are present, with break frequencies of 1 Hz, 10 Hz, and 100 Hz. Sketch the asymptotic magnitude Bode plot to scale. Estimate the lower half-power frequency.

Answer See Figure 8.51. $f_L \cong 100$ Hz.

EXERCISE

8.17 Find the break frequencies for the amplifier of Figure 8.52. If we want to reduce the lower half-power frequency of the amplifier, which capacitor is most critical? Should we increase or reduce its value?

Answer $f_1 = 0.796$ Hz, $f_2 = 53.1$ Hz, and $f_3 = 15.9$ kHz. To reduce the lower half-power frequency, it is most important to increase the value of C_3 .

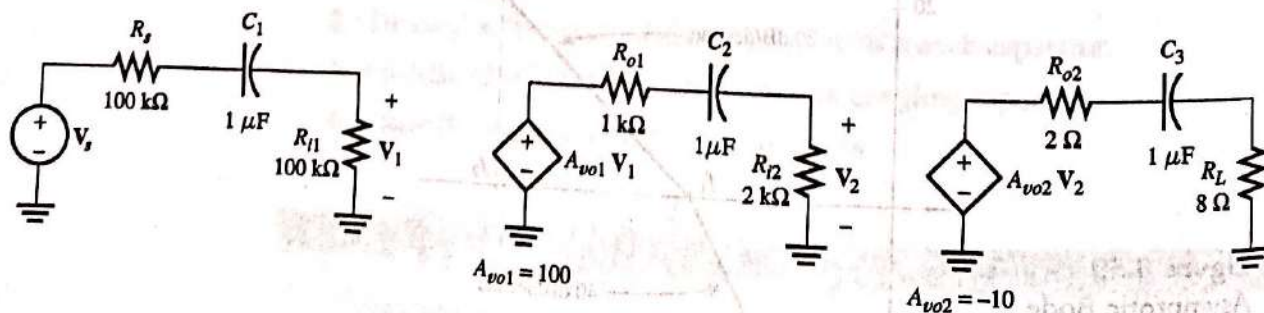
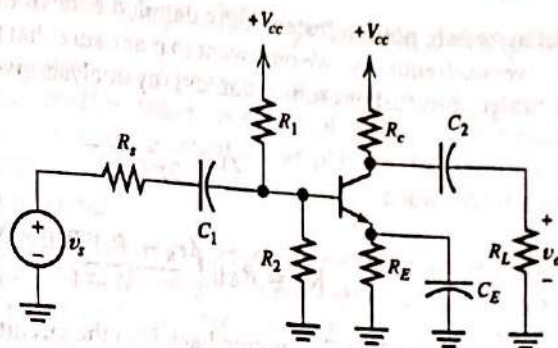


Figure 8.52 Amplifier for Exercise 8.17.

Figure 8.53
Discrete common-emitter amplifier.



Bypass Capacitors

Consider the common-emitter amplifier shown in Figure 8.53. Let us assume that the coupling capacitors (C_1 and C_2) are doing their jobs and act as short circuits at all frequencies of interest. Recall that the gain magnitude of a common-emitter amplifier becomes smaller when resistance appears in series with the emitter in the small-signal equivalent circuit. Also, notice that R_E and C_E are in parallel. Above a certain frequency f_1 , C_E acts approximately as a short circuit. Then the emitter is connected to ground, and the gain is high. On the other hand, below some frequency f_2 , C_E has a high impedance, and the impedance of the parallel combination is approximately equal to R_E . Then the gain is much smaller.

Thus the gain of the amplifier versus frequency takes the form shown in Figure 8.54. In the midband, the bypass capacitor acts as a short circuit, and the gain is constant versus frequency. As the frequency decreases below f_1 , the impedance of the bypass capacitor becomes significant, and gain falls off at 20 dB per decade. Finally, the capacitor impedance becomes larger than the emitter resistance, and the gain levels off. At low frequencies, the bypass capacitor acts as an open circuit, and the gain magnitude is determined by the resistance values.

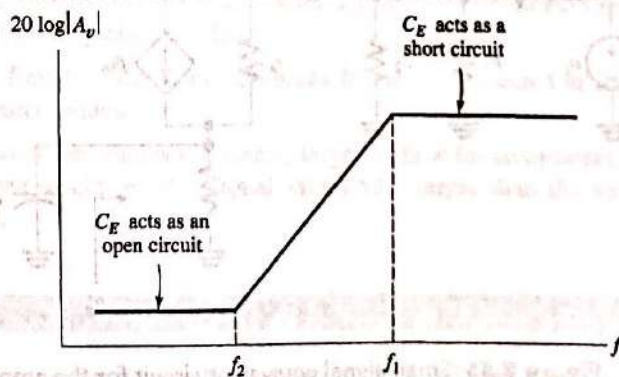


Figure 8.54
Gain magnitude
versus frequency.

Usually, we are not interested in the detailed behavior of the gain of an RC-coupled amplifier versus frequency. We only want to make sure that the frequency f_1 is sufficiently low. A straight forward but somewhat lengthy analysis gives

$$f_1 = \frac{1}{2\pi C_E R'_E} \quad (8.80)$$

where

$$R'_E = R_E \parallel \left(\frac{r_\pi + R_1 \parallel R_2 \parallel R_s}{\beta + 1} \right) \quad (8.81)$$

Bypass capacitors cause the gains of common-emitter or common-source amplifiers to decline at low frequencies. At very low frequencies, the gain again levels off. The break frequency at which the gain begins to fall is $f_1 = 1/(2\pi R'_E C_E)$, where R'_E is the resistance seen by the bypass capacitor.

is the resistance "seen" by C_E looking back into the circuit. As a general rule of thumb, the emitter bypass capacitor needs to be about β times the value of the input coupling capacitor for both to have about the same influence on the lower half-power frequency.

EXERCISE

8.18 Draw the small-signal equivalent circuit for the amplifier illustrated in Figure 8.53, assuming that C_1 and C_2 are short circuits. Then derive the expression given in Equation (8.81). (Hint: Replace V_s by a short circuit, and replace C_E by a test source V_x . Then $R'_E = V_x/I_x$, where I_x is the current delivered by V_x .)

Answer The small-signal equivalent circuit is shown in Figure 8.55.

EXERCISE

8.19 Determine the bias current I_{CQ} , the value of r_π , and the value of f_1 for the circuit of Figure 8.53, given that $R_1 = 10 \text{ k}\Omega$, $R_2 = 5 \text{ k}\Omega$, $R_s = 1 \text{ k}\Omega$, $R_E = R_C = R_L = 1 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, $C_E = 100 \text{ }\mu\text{F}$, $V_{BEQ} = 0.7 \text{ V}$, $V_T = 26 \text{ mV}$, and $\beta = 200$.

Answer $I_{CQ} = 4.2 \text{ mA}$, $r_\pi = 1235 \text{ }\Omega$, $R'_E = 9.87 \text{ }\Omega$, and $f_1 = 161 \text{ Hz}$.

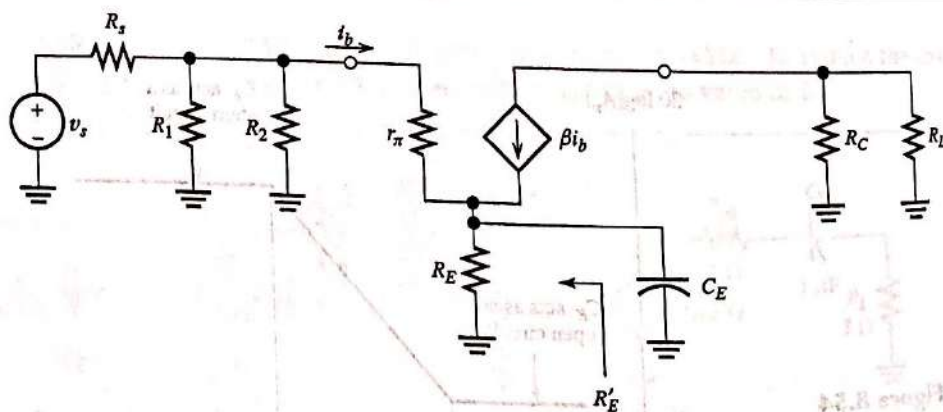


Figure 8.55 Small-signal equivalent circuit for the amplifier of Figure 8.53.

Design Considerations for Capacitively Coupled Amplifiers

Usually, in designing an RC-coupled amplifier, we want to ensure that the lower half-power frequency is less than a specified value. For example, in an audio amplifier, we generally want the lower half-power frequency of the amplifier to be less than the low-frequency capability of the loudspeakers. If that is the case, we know that the amplifier is not limiting the fidelity of the sound.

Of course, a very low value for f_L can be achieved simply by using very large values for the coupling and bypass capacitors. However, we must also consider factors such as the cost and the physical size of the capacitors, both of which increase as the capacitance value increases. Therefore, we want to choose the best (in terms of cost, size, etc.) values that allow the specification for f_L to be met. Furthermore, we should choose standard nominal values and allow sufficient margin so that the specification is met with nearly all combinations of components that are within their stated tolerances. When several coupling and bypass capacitors are present, we have several break frequencies—one for each capacitor. The overall lower half-power frequency of the amplifier is approximately equal to the sum of the break frequencies. Thus, if the individual break frequencies are $f_1, f_2, f_3, \dots, f_n$ the lower half-power frequency is approximately

The overall lower half-power frequency of an amplifier is approximately equal to the sum of the break frequencies.

$$f_L \cong f_1 + f_2 + f_3 + \dots + f_n \quad (8.82)$$

As a designer, when selecting values of coupling and bypass capacitors, it is a good approach to

1. Examine the circuit to see if any of the capacitors can be eliminated. Capacitors are relatively bulky and expensive—if any of them can be easily omitted, so much the better.
2. Determine the values of the resistances in series with each coupling capacitor and “seen” by each bypass capacitor. Treat all of the other capacitors as short circuits in determining the resistances. The break frequencies, capacitance values, and resistances are related by $f_{\text{break}} = 1/(2\pi RC)$, where R is the resistance in series with the capacitance. If it is practical to do so, redesign the circuit to increase the resistances so that smaller capacitances can be used.
3. Decide how to budget the desired lower half-power frequency between the various break frequencies. [Use Equation (8.82).]
4. Use the resistances found in Step 2 and the break frequencies selected in Step 3 to compute capacitance values.
5. Select standard capacitance values sufficiently large to allow for component tolerances. Usually, we would select nominal values 50% larger than the values computed in Step 4.

Example 8.12 Selecting Coupling Capacitor Values

Choose capacitance values for the amplifier of Figure 8.52 to achieve $f_L < 20$ Hz.

SOLUTION We follow the step-by-step design procedure given in this section:
 Step 1. No information is given concerning why the capacitors are included in Figure 8.52, so we assume that all three capacitors are needed. In a real design, we would have more information and might be able to eliminate one or more of the coupling capacitors.

Step 2. The total resistance in series with C_1 is

$$R_s + R_{i1} = 200 \text{ k}\Omega$$

For C_2 , the series resistance is

$$R_{o1} + R_{i2} = 3 \text{ k}\Omega$$

and for C_3 , the series resistance is

$$R_{o2} + R_L = 10 \Omega$$

We assume that these resistances cannot be changed by redesigning the amplifier.

Step 3. From Equation (8.82), we have

$$f_1 + f_2 + f_3 = f_L = 20 \text{ Hz}$$

Suppose, for now at least, that we choose $f_1 = f_2 = f_3 = 20/3 = 6.67 \text{ Hz}$.

(Later, we could investigate whether a different choice, such as $f_1 = 2 \text{ Hz}$, $f_2 = 2 \text{ Hz}$, and $f_3 = 16 \text{ Hz}$, leads to a more practical set of capacitor values.)

Because the resistance in series with C_3 is smallest, C_3 has the largest value.

Possibly allowing a larger value for f_3 would afford a savings of total cost and size.)

Step 4. The break frequencies are given by

$$f_1 = \frac{1}{2\pi(R_s + R_{i1})C_1}$$

$$f_2 = \frac{1}{2\pi(R_{o1} + R_{i2})C_2}$$

and

$$f_3 = \frac{1}{2\pi(R_{o2} + R_L)C_3}$$

Solving for the capacitances and substituting values results in

$$C_1 = 0.119 \mu\text{F}$$

$$C_2 = 7.959 \mu\text{F}$$

$$C_3 = 2388 \mu\text{F}$$

Either an exact analysis of the amplifier with these values or a SPICE simulation yields $f_L = 13.2 \text{ Hz}$ (instead of $f_L = 20 \text{ Hz}$), because Equation (8.82) gives a conservative estimate.

Step 5. We select standard capacitance values, allowing some margin for tolerances in the components. Assuming 20%-tolerance capacitors, we could choose the following values:

$$C_1 = 0.15 \mu\text{F}$$

$$C_2 = 10 \mu\text{F}$$

$$C_3 = 2700 \mu\text{F}$$

□

It is also good practice to allow for variations in the resistances that determine the break frequencies. These variations can be due to resistor tolerances, active-device parameters, and so forth.

SUMMARY

- On a logarithmic scale, the variable is multiplied by a constant for a given distance along the axis. On a linear scale, a constant is added to the variable for a given distance along the axis.
- For a decade of frequency, the higher frequency is 10 times the lower frequency. For an octave, the higher frequency is twice the lower.
- Network functions for lumped circuits can be expressed as a ratio of polynomials in the Laplace variable s . The roots of the numerator are called zeros, and the roots of the denominator are called poles.
- A Bode plot shows the magnitude in decibels or phase of a network function versus frequency—using a logarithmic scale for frequency.
- To attain a high value for the upper half-power frequency for a common-source amplifier, we should reduce the device capacitances C_{gs} and C_{gd} , reduce the source and load resistances R_{sig} and R_L , and reduce the gain magnitude. Reducing C_{gd} is more important than reducing C_{gs} .
- In an exact analysis of the high-frequency response of an amplifier we,
 1. draw the small-signal equivalent circuit,
 2. write circuit equations,
 3. use algebra to obtain the voltage gain V_o/V_s ,
 4. factor the numerator and denominator polynomials to determine break frequencies, and
 5. substitute values and draw the Bode plot.

- An impedance Z_f connected from the input to the output of an amplifier can be replaced by an impedance $Z_{in, Miller} = Z_f / (1 - A_v)$ across the input terminals and an impedance $Z_{out, Miller} = Z_f A_v / (A_v - 1)$. This is known as the Miller effect.
- The exact high-frequency analysis of amplifiers can be tedious. Approximate calculations based on the Miller approximation in which we ignore the effects of $Z_{out, Miller}$ are often useful.
- The hybrid- π model is useful in mathematical analysis of the high-frequency response of BJT amplifiers. The model parameters can often be calculated from the data published by manufacturers.
- The effect of C_μ on the high-frequency response of a high-gain common-emitter amplifier is greatly increased by the Miller effect. Bandwidth can be extended by reducing R_s or by reducing the midband gain (either by reducing R_L or by adding a small unbypassed emitter resistance).
- Some amplifier configurations that have improved high-frequency performance compared with the common-emitter stage are the common-base, the cascode connection, and the emitter-coupled differential pair. FET versions of these circuits are also useful.
- When the load is a capacitance and extended high-frequency response is needed, a good choice for the output stage is the emitter follower, because it tends to have low output impedance.
- Each coupling capacitor in an RC-coupled amplifier contributes a 20-dB-per-decade decline in gain at low frequencies. The break frequency for each capacitor is $f_{break} = 1 / (2\pi RC)$, where R is the total equivalent resistance in series with the capacitor.
- Bypass capacitors cause the gains of common-emitter or common-source amplifiers to decline at low frequencies. At very low frequencies, the gain again levels off. The break frequency at which the gain begins to fall is given by $f_{break} = 1 / (2\pi RC)$, where R is the resistance "seen" by the bypass capacitor.
- We can estimate the lower half-power frequency by first finding the break frequency for each coupling or bypass capacitor (while treating the other capacitors as short circuits) and then adding the resulting break frequencies:

$$f_L \cong f_1 + f_2 + f_3 + \dots + f_n$$

PROBLEMS

Section 8.1: Bode Plots

- 8.1. How is a logarithmic scale different from a linear scale?
- 8.2. What is a decade? What is an octave?
- 8.3. Describe in general terms the Bode magnitude plot for a network function. Repeat for the Bode phase plot.
- 8.4. What are the poles of a network function? What are the zeros?

8.5. Draw the circuit diagram of a single-pole RC lowpass filter. What is the rate of the roll-off of the voltage magnitude of this filter in the high-frequency region?

8.6. How many decades is the frequency range from 50 Hz to 2200 Hz? How many octaves?

8.7. Sketch the approximate magnitude and phase Bode plots for the following gain functions:

(a)
$$A(s) = \frac{10(s + 200\pi)}{s + 2000\pi}$$

$$(b) \quad A(s) = \frac{s - 200\pi}{s + 200\pi}$$

$$(c) \quad A(s) = \frac{4\pi^2 10^9}{s^2 + (5\pi 10^4)s + 4\pi^2 10^8}$$

(Hints: Replace s by $j2\pi f$ and divide by appropriate constants to put the expressions into forms similar to Equation (8.17) or Equation (8.23). For part (c), factor the denominator first.)

8.8. Prepare magnitude and phase Bode plots for each of the circuits shown in Figure P8.8.

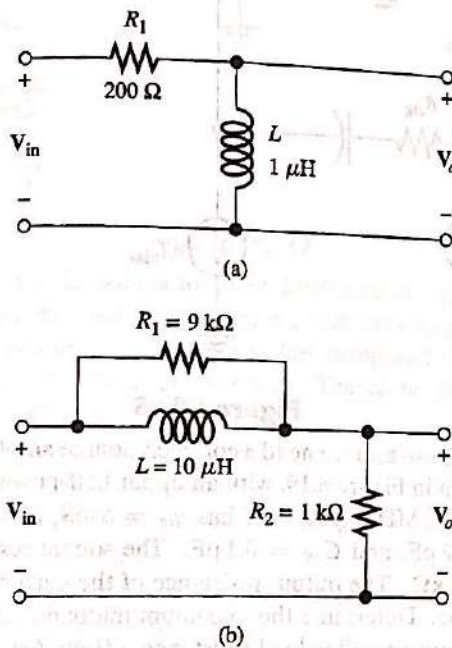


Figure P8.8

8.9. Consider the circuit illustrated in Figure P8.9. Assume that the amplifier has infinite input impedance and zero output impedance. Furthermore, the voltage gain of the amplifier is -1 .

- Derive an expression for the transfer function of the circuit, V_o/V_{in} , as a function of s .
- Find the poles and zeroes of the transfer function.
- Sketch the asymptotes for the Bode magnitude and phase plots.
- Suppose that $C = 470$ pF, the resistor R is variable from 0 to 1 k Ω , and the input voltage is a 1-MHz sine wave with unity amplitude and zero phase. Sketch the amplitude of the output voltage against R . Sketch the phase angle of the output voltage to scale against R .

This circuit is very useful when we need a circuit that can adjust the phase of a sinusoid without affecting its amplitude.

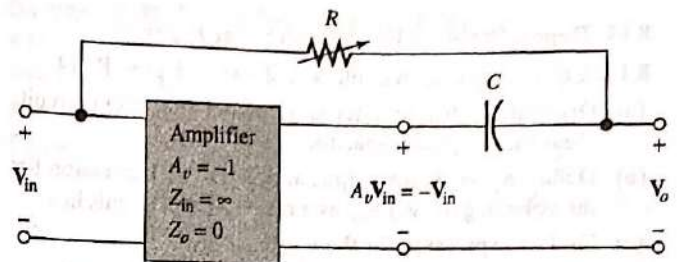


Figure P8.9 Variable-phase-shift circuit.

Section 8.2: The FET Common-Source Amplifier at High Frequencies

8.10. List the steps that need to be carried out for the exact high-frequency analysis of an amplifier.

8.11. What steps can be taken to increase the upper half-power frequency of a common-source amplifier?

8.12. Consider the common-source amplifier illustrated in Figure P8.12. Treat the 1- μ F coupling capacitor as a short circuit in the high-frequency equivalent circuit. The FET operates in the saturation region with $V_{DSQ} = 10$ V. The FET has $KP = 50 \mu\text{A}/\text{V}^2$, $W/L = (400 \mu\text{m})/(10 \mu\text{m})$, $V_{to} = 1$ V, $\lambda = 0.01$, $C_{gs} = 0.5$ pF, and $C_{gd} = 0.5$ pF. Determine the midband gain, the break frequencies, and the approximate upper half-power frequency for $A_v = V_o/V_{sig}$. Check the midband gain and upper half-power frequency by using PSpice.

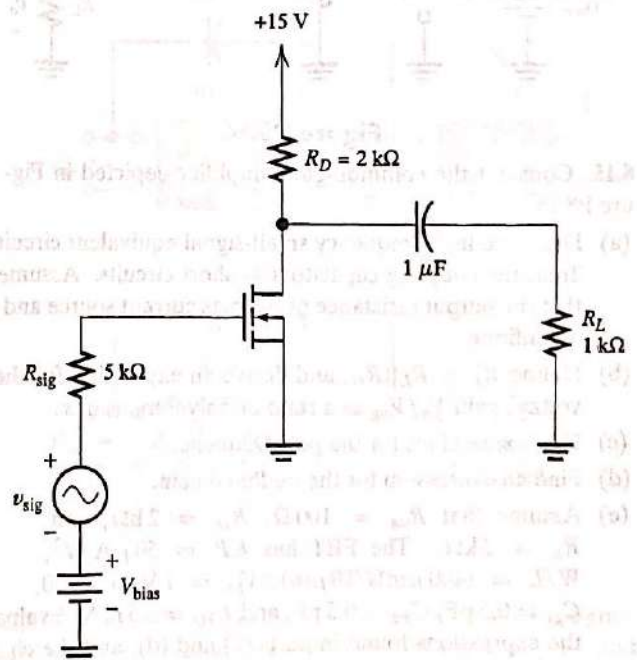


Figure P8.12

8.13. Repeat Problem 8.12, assuming that $R_{sig} = 0$.

8.14. Consider the source follower shown in Figure P8.14.

- Draw the high-frequency small-signal equivalent circuit. Treat the coupling capacitor as a short circuit.
- Define $R'_L = R_L || R_{bias} || r_d$, and derive an expression for the voltage gain V_o/V_{sig} as a ratio of polynomials in s .
- Find an expression for the midband gain.
- Assume that $R_{sig} = 10\text{ k}\Omega$, $R_{bias} = 2\text{ k}\Omega$, and $R_L = 2\text{ k}\Omega$. The FET has $KP = 50\text{ }\mu\text{A/V}^2$, $W/L = (400\text{ }\mu\text{m})/(10\text{ }\mu\text{m})$, $V_{io} = 1\text{ V}$, $\lambda = 0$, $C_{gs} = 0.5\text{ pF}$, $C_{gd} = 0.5\text{ pF}$, and $I_{DQ} = 2.5\text{ mA}$. Evaluate the expression found in part (c). Determine the pole and zero frequencies and estimate the half-power frequency.
- Check the results of part (d) by using PSpice.

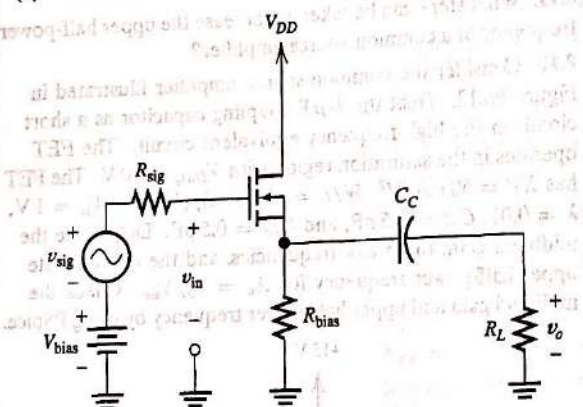


Figure P8.14

8.15. Consider the common-gate amplifier depicted in Figure P8.15.

- Draw the high-frequency small-signal equivalent circuit. Treat the coupling capacitors as short circuits. Assume that the output resistance of the bias current source and r_d are infinite.
- Define $R'_L = R_L || R_D$, and derive an expression for the voltage gain V_o/V_{sig} as a ratio of polynomials in s .
- Find expressions for the pole frequencies.
- Find an expression for the midband gain.
- Assume that $R_{sig} = 100\text{ }\Omega$, $R_D = 2\text{ k}\Omega$, and $R_L = 2\text{ k}\Omega$. The FET has $KP = 50\text{ }\mu\text{A/V}^2$, $W/L = (400\text{ }\mu\text{m})/(10\text{ }\mu\text{m})$, $V_{io} = 1\text{ V}$, $\lambda = 0$, $C_{gs} = 0.5\text{ pF}$, $C_{gd} = 0.5\text{ pF}$, and $I_{DQ} = 2.5\text{ mA}$. Evaluate the expressions found in parts (c) and (d), and sketch a Bode plot to scale.
- Check the results of part (e) by using PSpice.

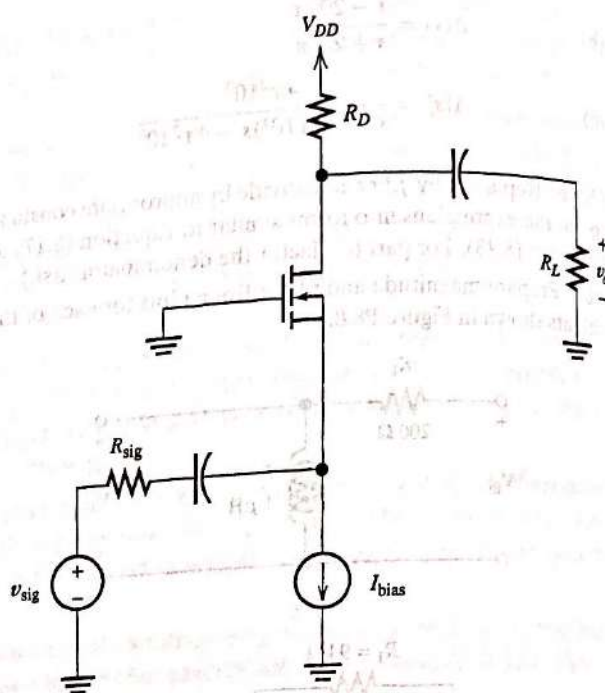


Figure P8.15

8.16. Suppose that we need a common-source amplifier like the one shown in Figure 8.19, with an upper half-power frequency of at least 1 MHz. The FET has $g_m = 5\text{ mS}$, $r_d = 100\text{ k}\Omega$, $C_{gs} = 0.2\text{ pF}$, and $C_{gd} = 0.1\text{ pF}$. The source resistance is $R_{sig} = 10\text{ k}\Omega$. The output resistance of the current source is $R_{bias} = \infty$. Determine the maximum midband gain allowed and the corresponding load resistance. (Hint: Assume that the upper half-power frequency is equal to the pole frequency f_{p1} .)

8.17. Consider the common-source amplifier shown in Figure P8.17. Assume that the load capacitance is sufficiently large that the upper half-power frequency is very low compared with that of the same circuit with a resistive load. Therefore, the device capacitances C_{gs} and C_{gd} can be ignored.

- Draw the high-frequency small-signal equivalent circuit.
- Define $R'_L = R_D || r_d$, and derive an expression for the voltage gain V_o/V_{sig} as a ratio of polynomials in s .
- Find an expression for the pole frequency.
- Find an expression for the midband gain.
- Assume that $R_{sig} = 100\text{ }\Omega$, $R_D = 2\text{ k}\Omega$, and $C_L = 2000\text{ pF}$. The FET has $KP = 50\text{ }\mu\text{A/V}^2$, $W/L = (400\text{ }\mu\text{m})/(10\text{ }\mu\text{m})$, $V_{io} = 1\text{ V}$, $\lambda = 0$, and $I_{DQ} = 2.5\text{ mA}$. Evaluate the expressions found in parts (c) and (d), and sketch a Bode plot to scale.
- Check the results of part (e) by using PSpice.

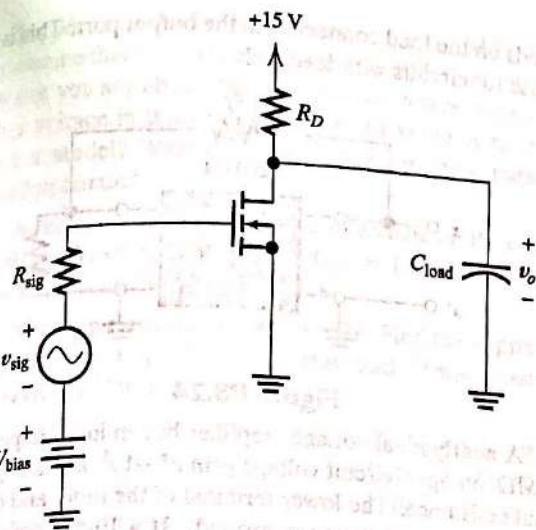


Figure P8.17

8.18. Consider the source follower illustrated in Figure P8.18. Assume that the load capacitance is sufficiently large that the upper half-power frequency is very low compared with that of the same circuit with a resistive load. Therefore, the device capacitances C_{gs} and C_{gd} can be ignored.

- Draw the high-frequency small-signal equivalent circuit. Assume that $R_{bias} = \infty$.
- Derive an expression for the voltage gain V_o/V_{sig} as a ratio of polynomials in s .
- Find an expression for the pole frequency.
- Find an expression for the midband gain.
- Assume that $R_{sig} = 10\text{ k}\Omega$ and $C_L = 2000\text{ pF}$. The FET has $KP = 50\text{ }\mu\text{A/V}^2$, $W/L = (400\text{ }\mu\text{m})/(10\text{ }\mu\text{m})$, $V_{to} = 1\text{ V}$, $\lambda = 0.01$, and $I_{DQ} = 2.5\text{ mA}$. Evaluate the expressions found in parts (c) and (d), and sketch a Bode plot to scale.
- Check the results of part (e) by using PSpice.

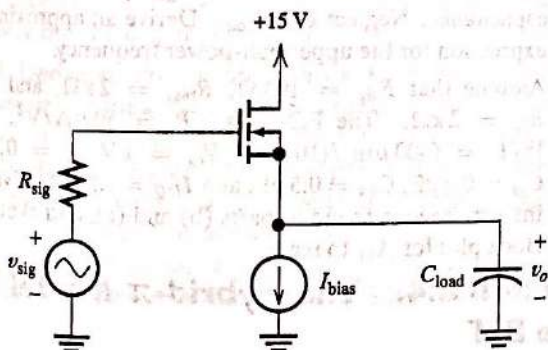


Figure P8.18

Section 8.3: The Miller Effect

8.19. How is the Miller effect applied in the high-frequency analysis of an amplifier such as the common-source stage?

8.20. Find the input impedance of each of the circuits shown in Figure P8.20. The amplifiers are ideal voltage amplifiers.

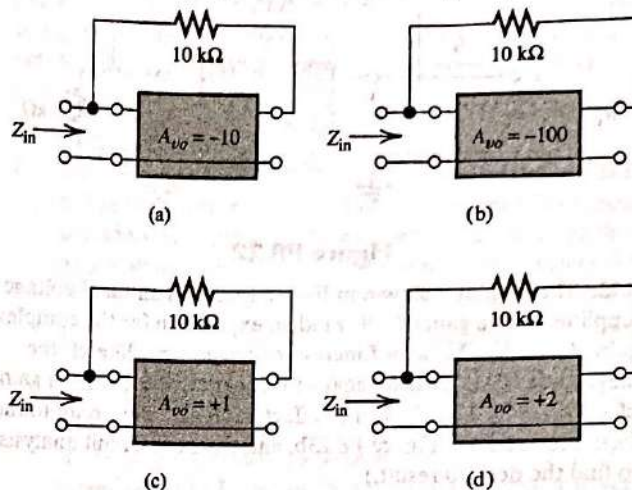


Figure P8.20

8.21. Find the input capacitance for each of the circuits displayed in Figure P8.21. The amplifiers are ideal voltage amplifiers.

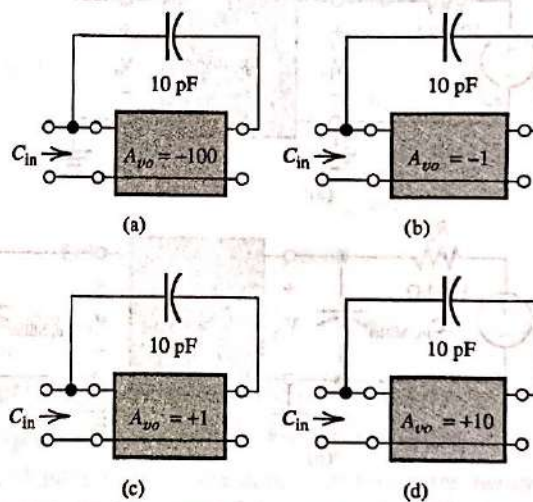


Figure P8.21

8.22. The amplifier illustrated in Figure P8.22 has an input resistance of $10\text{ k}\Omega$, an open-circuit voltage gain of -10 , and an output resistance of $1\text{ k}\Omega$. Find the resistance R_x seen from terminals $x-x'$. First, find an approximate value by assuming

that $R_{o, \text{Miller}} = R_f$. Second, do an exact analysis by writing circuit equations involving v_x and i_x and then solving for the ratio v_x/i_x . Compare the results found by each approach.

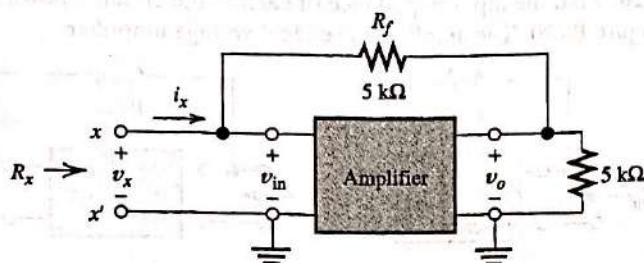


Figure P8.22

8.23. The amplifier shown in Figure P8.23a is an ideal voltage amplifier with a gain of -9 . Find an expression for the complex gain $A_s = V_o/V_s$ as a function of frequency. Sketch the magnitude of A_s to scale against frequency. Repeat for a gain of -99 . (Hint: Use the Miller effect to change the circuit to the form illustrated in Figure P8.23b, and then use circuit analysis to find the desired result.)

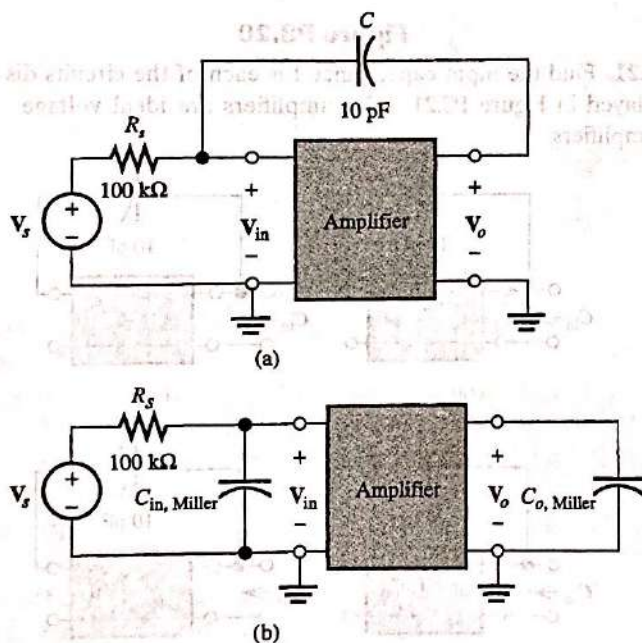


Figure P8.23

8.24. Find the input resistance seen at terminals $x-x'$ for the circuit of Figure P8.24 if $R_L = 10 \text{ k}\Omega$. The amplifier has an open-circuit voltage gain of -10 , input resistance of $100 \text{ k}\Omega$, and output resistance of $1 \text{ k}\Omega$. Repeat for $R_L = 1 \text{ k}\Omega$. Notice that the input impedance is not a constant parameter, but

depends on the load connected to the output port. This is often the case for circuits with feedback.

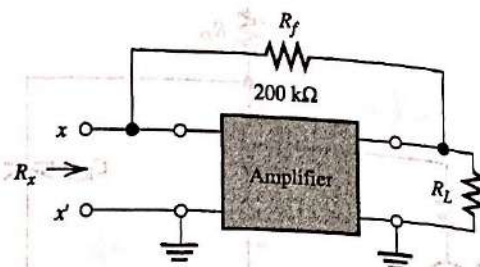


Figure P8.24

8.25. A nearly ideal voltage amplifier has an input impedance of $1 \text{ M}\Omega$, an open-circuit voltage gain of -10^5 , and a negligible output resistance. The lower terminal of the input and output ports are tied to a common ground. If a $10\text{-k}\Omega$ resistor is connected between the input and output, find the input impedance and output impedance of the circuit. Assume that the signal source is an ideal current source. Classify the resulting circuit as an approximate ideal amplifier and find the corresponding gain parameter.

8.26. Consider the common-source amplifier shown in Figure P8.12. Treat the $1\text{-}\mu\text{F}$ coupling capacitor as a short circuit in the high-frequency equivalent circuit. The FET operates in the saturation region with $V_{DSQ} = 10 \text{ V}$. The FET has $K_P = 50 \mu\text{A}/\text{V}^2$, $W/L = (400 \mu\text{m})/(10 \mu\text{m})$, $V_{to} = 1 \text{ V}$, $\lambda = 0.01$, $C_{gs} = 0.5 \text{ pF}$, and $C_{gd} = 0.5 \text{ pF}$. Use the Miller effect to determine the approximate upper half-power frequency.

8.27. Consider the source follower shown in Figure P8.14.

- Draw the high-frequency small-signal equivalent circuit. Treat the coupling capacitor as a short circuit.
- Define $R'_L = R_L || R_{\text{bias}} || r_d$ and derive an expression for the midband voltage gain $A_v = V_o/V_{\text{in}}$. Note that $A_{vs} = V_o/V_{\text{sig}} = A_v$ in the midband.
- Use the Miller effect to replace C_{gs} by its equivalent capacitance. Neglect $C_{\text{Miller, out}}$. Derive an approximate expression for the upper half-power frequency.
- Assume that $R_{\text{sig}} = 10 \text{ k}\Omega$, $R_{\text{bias}} = 2 \text{ k}\Omega$, and $R_L = 2 \text{ k}\Omega$. The FET has $K_P = 50 \mu\text{A}/\text{V}^2$, $W/L = (400 \mu\text{m})/(10 \mu\text{m})$, $V_{to} = 1 \text{ V}$, $\lambda = 0$, $C_{gs} = 0.5 \text{ pF}$, $C_{gd} = 0.5 \text{ pF}$, and $I_{DQ} = 2.5 \text{ mA}$. Evaluate the expressions found in parts (b) and (c), and sketch a Bode plot for A_{vs} to scale.

Section 8.4: The Hybrid- π Model for the BJT

8.28. Draw the hybrid- π model for the BJT and label the parameters.

8.29. Suppose that the Early voltage of a certain BJT is infinite. Also, assume that the currents through C_μ and r_μ are negligible. What can you say about collector current versus collector-to-emitter voltage in this case? What is the value of r_o in the hybrid- π model? What is the value of h_{oe} in the h -parameter equivalent circuit?

8.30. A certain npn BJT has an Early voltage of $V_A = 100$ V. Find the value of $r_o \cong 1/h_{oe}$ for $I_{CQ} = 1$ mA. Repeat for $I_{CQ} = 0.1$ mA and for $I_{CQ} = 10$ mA.

8.31. A certain transistor has $h_{fe} = 200$. Find the approximate value of h_{ie} for $I_{CQ} = 0.1$ mA, 1 mA, and 10 mA. Assume a temperature of 300 K.

8.32. The transistor illustrated in Figure P8.32 has $h_{re} = 10^{-4}$. Find the reading of the voltmeter in the ac mode. Assume that the ac base current is negligible (because of the high impedances of R_B and the voltmeter).

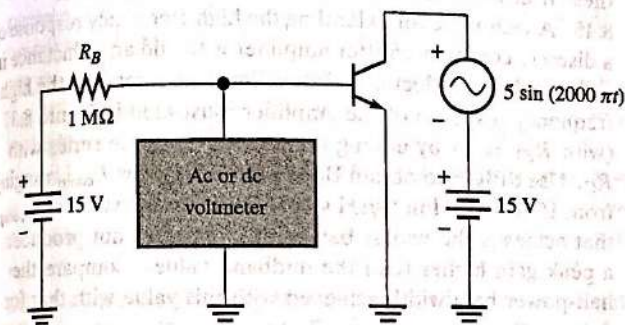


Figure P8.32

8.33. The transistor shown in Figure P8.32 has $h_{oe} = 10^{-4}$ S. Find the rms value of the ac collector current. Assume that the ac base current is negligible.

8.34. Consider the circuit shown in Figure P8.32. In the dc mode, the voltmeter gives a reading of 0.65 V. In the ac mode, the voltmeter gives a reading of 1 mV rms. The dc collector current is known to be $I_{CQ} = 5$ mA. The ac collector current is 0.1 mA rms. Find approximate values of h_{re} , h_{fe} , h_{oe} , and h_{ie} .

8.35. Derive an exact expression for h_{ie} in terms of the parameters of the hybrid- π model at low frequencies. Evaluate the exact expression to find h_{ie} from the 2N2222A equivalent circuit shown in Figure 8.31. What percentage error results if the approximation $h_{ie} = r_\pi$ is used? Is this error significant, considering the unit-to-unit variations of these devices? (Hint: At low frequencies, the capacitors C_μ and C_π are open circuits and can be neglected. From Equation (8.39), we have

$$h_{ie} = \frac{v_{be}}{i_b} \bigg|_{v_{ce}=0}$$

Thus, h_{ie} is the impedance seen looking into the base-emitter terminals of the small-signal equivalent circuit with the collector shorted to the emitter. Therefore, find the input impedance of the hybrid- π equivalent circuit under these conditions.)

8.36. Derive an exact expression for h_{oe} in terms of the parameters of the hybrid- π equivalent circuit. Find the value of h_{oe} for the transistor of Figure 8.31. (Hint: The method of attack for this problem is similar to that for Problem 8.35.)

8.37. Consider the hybrid- π model for the BJT with a short connected from the collector to the emitter.

- Derive an expression for the ratio of the collector current to the base current as a function of frequency. To simplify the analysis, replace r_μ by an open circuit and use the approximation $i_c \cong g_m v_\pi$. (In other words, neglect the current through C_μ in computing the collector current.)
- The transition frequency f_t is the frequency at which the short-circuit common-emitter current gain has a magnitude of unity. Use the expression found in part (a) for the current gain to obtain an expression for f_t in terms of the hybrid- π parameters. Show that your result is equivalent to Equation (8.44), assuming that β is very large compared to unity.

8.38. The data sheet for a certain transistor gives the following data for a Q-point of $V_{CEQ} = 10$ V and $I_{CQ} = 1$ mA:

$$h_{re} = 1 \times 10^{-5}$$

$$h_{fe} = 500$$

$$h_{oe} = 2 \times 10^{-5} \text{ S}$$

$$f_t = 400 \text{ MHz}$$

$$C_\mu = 2 \text{ pF}$$

$$\text{Collector-base time constant} = 20 \text{ ps}$$

Find values for the parameters of the hybrid- π equivalent circuit.

Section 8.5: Common-Emitter Amplifiers at High Frequencies

8.39. What happens to the upper half-power frequency of a common-emitter amplifier if R_L is increased? Why?

8.40. Consider the common-emitter amplifier illustrated in Figure P8.40. Assume that the transistor has $\beta = 100$ and $V_{BEQ} \cong 0.7$ V.

- Find the values of R_B and R_C for a bias point of $I_{CQ} = 1$ mA and $V_{CEQ} = 8$ V.

- (b) The transistor is specified to have $r_x = 50\ \Omega$, $C_\mu = 5\text{ pF}$, $r_o = 20\text{ k}\Omega$, and $f_t = 500\text{ MHz}$ at the bias point of part (a). Compute the upper half-power frequency for A_{vs} . Also, compute the midband magnitude of A_{vs} .

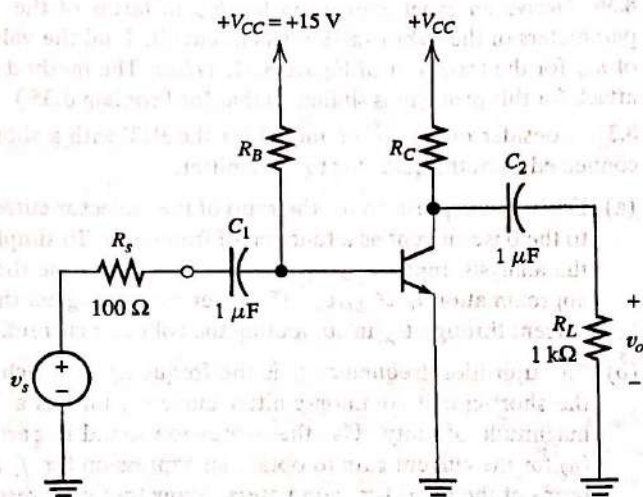


Figure P8.40

- 8.41.** Repeat Problem 8.40 if a 2N5089 transistor is used. Typical parameters for this transistor are $\beta = 700$, $C_\mu = 3\text{ pF}$, $f_t = 60\text{ MHz}$, $V_A = 50\text{ V}$, and $r_x = 50\ \Omega$. Check your results by using PSpice. A PSpice model for the 2N5089 transistor is included in the DEVICE.LIB file.
- D8.42. Common-emitter amplifier design.** Design a common-emitter amplifier using the 2N2222A transistor, biased at $I_{CQ} = 1\text{ mA}$ and $V_{CEQ} = 10\text{ V}$. The load resistance is $R_L = 100\text{ k}\Omega$ and the source resistance is $R_s = 1\text{ k}\Omega$. The input and the output must be ac coupled. The available power supply voltages are $V_{CC} = 15\text{ V}$ and $V_{EE} = -15\text{ V}$. Maximize $|A_{vs}|$ in a manner consistent with the other specifications. Use SPICE to find the midband gain and the upper half-power frequency for your design. Repeat the design for $I_{CQ} \cong 10\ \mu\text{A}$, and compare the midband gain magnitude and upper half-power frequency with those for $I_{CQ} = 1\text{ mA}$. First design the bias circuit. We are not concerned with the low-frequency performance, and coupling capacitors of $1\ \mu\text{F}$ will be adequate. Because of the variation of f_t , you will find that the gain-bandwidth product is much lower for the lower bias current.
- 8.43.** (a) Starting from the hybrid- π equivalent circuit for the common-emitter amplifier shown in Figure 8.33b, derive an expression for the midband voltage gain $A_v = v_o/v_{in}$. Of course, the capacitances C_μ and C_π should be treated as open circuits in the midband.
- (b) Use the expression found in part (a) to compute A_v (in the midband) for the circuit of Figure 8.37. Assume that

$R_{E1} = 0$. (The values of the hybrid- π parameters are shown in Figure 8.31.)

- (c) Use Equation (4.47) with $R_{E1} = 0$ to repeat the computation of part (b). Compare the results. Considering that, for a given type of transistor, β can vary by a ratio of three to one from unit to unit, is the increased accuracy afforded by the more complex equivalent circuit significant?

8.44. Recall that f_t is the frequency for which the short-circuit common-emitter current-gain magnitude is unity. "Short circuit" means that the collector is shorted to ground for ac signals, which is easily achieved by connecting the collector directly to a power supply. Devise a SPICE simulation of a circuit to obtain plots of the current gain of the 2N2222A transistor versus frequency for $V_{CEQ} \cong 10\text{ V}$ and $I_{CQ} \cong 10\ \mu\text{A}$, $100\ \mu\text{A}$, 1 mA , and 10 mA . From the plots, determine f_t at each current. Repeat for the 2N5210 transistor. Models for these transistors are included in the DEVICE.LIB file.

8.45. A technique for extending the high-frequency response of a discrete common-emitter amplifier is to add an inductance in series with the collector resistor. Consider extending the high-frequency response of the amplifier illustrated in Figure 8.37 (with $R_{E1} = 0$) by adding an inductor L_{comp} in series with R_C . Use SPICE to obtain Bode plots of A_{vs} for L_{comp} ranging from 15 to $40\ \mu\text{H}$ in $5\text{-}\mu\text{H}$ steps. Estimate the value of L_{comp} that achieves the widest bandwidth, but does not produce a peak gain higher than the midband value. Compare the half-power bandwidth achieved with this value with that for $L_{comp} = 0$.

Section 8.6: Common-Base, Cascode, and Differential Amplifiers

- 8.46.** Consider the common-emitter, common-base, cascode, and emitter-coupled differential BJT amplifiers discussed in this chapter. Which tends to have the lowest input impedance? Which are inverting? Which are noninverting? For which is the high-frequency response most limited by the Miller effect?
- 8.47.** Usually, a common-base amplifier is not suitable for use with a high-impedance source. Why not?
- 8.48.** Draw the circuit diagram of a cascode amplifier.
- D8.49. Common-base amplifier design.** Design a common-base amplifier using the 2N2222A transistor, biased at $I_{CQ} = 1\text{ mA}$ and $V_{CEQ} = 10\text{ V}$. The load resistance is $R_L = 100\text{ k}\Omega$ and the source resistance is $R_s = 1\text{ k}\Omega$. The input and the output must be ac coupled. The available power supply voltages are $V_{CC} = 15\text{ V}$ and $V_{EE} = -15\text{ V}$. Maximize $|A_{vs}|$ in a manner consistent with the other specifications. Use SPICE to find the midband gain and the upper half-power frequency for your design. Repeat the design for $I_{CQ} \cong 10\ \mu\text{A}$, and compare the midband gain magnitude and upper half-power frequency

with those for $I_{CQ} = 1$ mA. The circuit configuration is shown in Figure 8.39a. First select values for R_C and R_E to achieve the desired bias point. We are not concerned with the low-frequency response in this problem. $1\text{ }\mu\text{F}$ is a suitable value for the coupling capacitors.

D8.50. Cascode amplifier design. Design a cascode amplifier using 2N2222A transistors. Both transistors should be biased at $I_{CQ} = 1$ mA and $V_{CEQ} = 10$ V. The load resistance is $R_L = 100\text{ k}\Omega$ and the source resistance is $R_s = 1\text{ k}\Omega$. The input and the output must be ac coupled. The available power supply voltages are $V_{CC} = 15$ V and $V_{EE} = -15$ V. Maximize $|A_{vs}|$ in a manner consistent with the other specifications. Use SPICE to find the midband gain and the upper half-power frequency for your design. Repeat the design for $I_{CQ} \cong 10\text{ }\mu\text{A}$, and compare with those for $I_{CQ} = 1$ mA. The circuit configuration is shown in Figure 8.40. First select values for R_C , R_E , R_1 , and R_2 to achieve the desired bias points. We are not concerned with the low-frequency response in this problem. $1\text{ }\mu\text{F}$ is a suitable value for the coupling capacitors and $100\text{ }\mu\text{F}$ is suitable for the bypass capacitor.

D8.51. Emitter-coupled pair amplifier design. Repeat Problem D8.50 for a differential amplifier. In this case, V_{CEQ} will be higher than 10 V for one of the transistors. Design for $I_{CQ} = 1$ mA for both transistors. The circuit configuration is shown in Figure 8.41. First select values for R_C , R_{E1} , R_{E2} , and R_B to achieve the desired bias points. We are not concerned with the low-frequency response in this problem. Let $C_1 = C_2 = 1\text{ }\mu\text{F}$ and $C_E = 100\text{ }\mu\text{F}$.

D8.52. Common-gate amplifier design. Design a common-gate FET amplifier. The available FETs have $K_P = 50\text{ }\mu\text{A/V}^2$, $W/L = (400\text{ }\mu\text{m})/(10\text{ }\mu\text{m})$, $V_{to} = 1$ V, $\lambda = 0.01$, $C_{gs} = 0.5\text{ pF}$, and $C_{gd} = 0.5\text{ pF}$. Bias the FET at $I_{CQ} = 2.5\text{ mA}$ and $V_{DSQ} = 10$ V. The load resistance is $R_L = 100\text{ k}\Omega$ and the source resistance is $R_s = 1\text{ k}\Omega$. The input and the output must be ac coupled. The available power supply voltages are $V_{DD} = 15$ V and $V_{SS} = -15$ V. Maximize $|A_{vs}|$ in a manner consistent with the other specifications. Use SPICE to find the midband gain and the upper half-power frequency for your design. The circuit configuration for the common-gate amplifier is similar to that of the common-base amplifier shown in Figure 8.39a. Choose the resistors to achieve the desired bias point. We are not concerned with the low-frequency response in this problem. Let $C_1 = C_2 = 1\text{ }\mu\text{F}$.

D8.53. Cascode amplifier design. Repeat Problem 8.52 for a cascode configuration using FETs. The circuit configuration for the FET cascode amplifier is similar to that shown in Figure 8.40 for the BJT. Choose the resistors to achieve the desired bias point. We are not concerned with the low-frequency response in this problem. Let $C_1 = C_2 = 1\text{ }\mu\text{F}$ and $C_E = 100\text{ }\mu\text{F}$.

D8.54. FET source-coupled differential pair design. Repeat Problem 8.52 for a source-coupled differential pair. In this case,

V_{DSQ} will be higher than 10 V for one of the transistors. Design for $I_{CQ} = 2.5\text{ mA}$ for both transistors. The circuit configuration for the source-coupled pair is similar to that of the emitter-coupled pair shown in Figure 8.41. Choose the resistors to achieve the desired bias points. We are not concerned with the low-frequency response in this problem. Let $C_1 = C_2 = 1\text{ }\mu\text{F}$ and $C_E = 100\text{ }\mu\text{F}$.

Section 8.7: Emitter Followers

8.55. A wideband amplifier is to be designed that is required to have a voltage-gain magnitude $|A_{vs}|$ of approximately 10. The source resistance and the load resistance are both equal to $500\text{ }\Omega$. Which of the following circuit configurations are appropriate? Which are inappropriate? Explain. (a) Common base. (b) Common emitter. (c) Differential amplifier. (d) Cascode. (e) Emitter follower. (f) Emitter follower cascaded with a common emitter.

8.56. Derive expressions for the upper half-power frequency of A_{vs} for the source follower illustrated in Figure P8.56. Use the small-signal equivalent circuit shown in Figure 8.18. (Hint: Follow the approach used for the emitter follower in Section 8.7.) Evaluate the upper half-power frequency and midband value of A_{vs} for $R_{sig} = 5\text{ k}\Omega$, $R_G = 1\text{ M}\Omega$, $R_S = 5\text{ k}\Omega$, $r_d = 20\text{ k}\Omega$, $R_L = 2\text{ k}\Omega$, $C_{gs} = C_{gd} = 0.5\text{ pF}$, and $g_m = 5000\text{ }\mu\text{S}$.

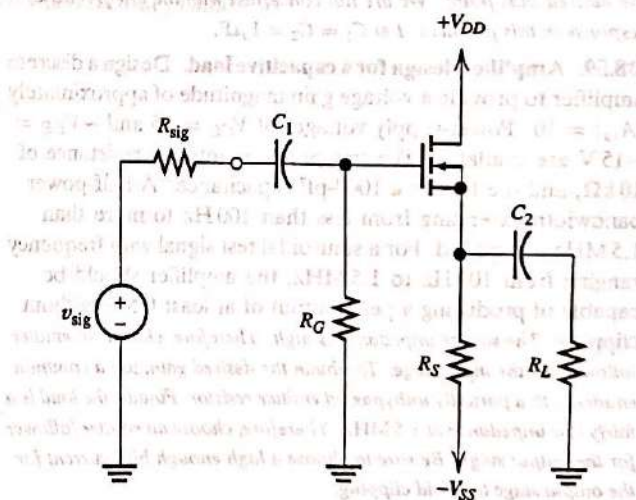


Figure P8.56 Source follower.

8.57. Compute the midband values of A_v , A_{vs} , and R_{in} for the emitter follower shown in Figure P8.57. Compute the upper half-power frequency for A_v and the upper half-power frequency for A_{vs} . The transistor has $\beta = 150$, $r_x = 30\text{ }\Omega$, $C_\mu = 5\text{ pF}$, $r_o = 100\text{ k}\Omega$, and $f_t = 500\text{ MHz}$.

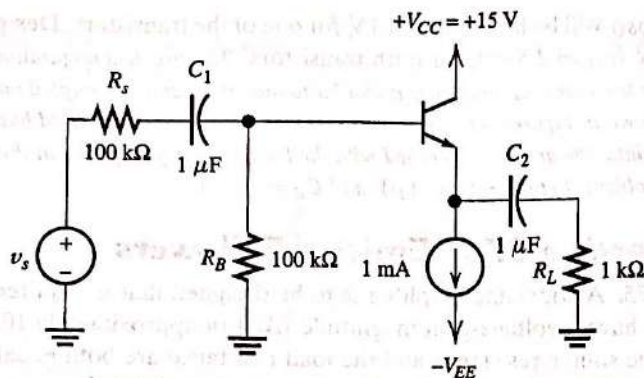


Figure P8.57

D8.58. Emitter follower design. Design an emitter follower using the 2N2222A transistor, biased at $I_{CQ} = 1$ mA and $V_{CEQ} > 10$ V. The load resistance is $R_L = 1$ kΩ and the source resistance is $R_s = 100$ kΩ. The input and the output should be ac coupled. The available power supply voltages are $V_{CC} = 15$ V and $-V_{EE} = -15$ V. Use a SPICE program to find the midband value of A_{vs} and the upper half-power frequency for your design. Repeat the design for $I_{CQ} \cong 10$ μA, and compare the midband gain magnitude and upper half-power frequency with those for $I_{CQ} = 1$ mA. The circuit configuration is shown in Figure 8.42a. First select values for R_E and R_B to achieve the desired bias point. We are not concerned with the low-frequency response in this problem. Let $C_1 = C_2 = 1$ μF.

D8.59. Amplifier design for a capacitive load. Design a discrete amplifier to provide a voltage gain magnitude of approximately $|A_{vs}| = 10$. Power-supply voltages of $V_{CC} = 15$ and $-V_{EE} = -15$ V are available. The source has an internal resistance of 10 kΩ, and the load is a 1000-pF capacitance. A half-power bandwidth extending from less than 100 Hz to more than 1.5 MHz is required. For a sinusoidal test signal with frequency ranging from 100 Hz to 1.5 MHz, the amplifier should be capable of producing a peak output of at least 0.5 V without clipping. The source impedance is high. Therefore, choose an emitter follower for the input stage. To obtain the desired gain, use a common emitter with a partially unbypassed emitter resistor. Finally, the load is a fairly low impedance at 1.5 MHz. Therefore, choose an emitter follower for the output stage. Be sure to choose a high enough bias current for the output stage to avoid clipping.

Section 8.8: Low-Frequency Response of RC-Coupled Amplifiers

- 8.60.** What is the main purpose of coupling capacitors? Of bypass capacitors?
- 8.61.** Give a formula for the break frequency associated with a coupling capacitor. Define the terms in the formula.
- 8.62.** In general, what effect does a coupling capacitor have on the magnitude Bode plot of the voltage gain of an amplifier?
- 8.63.** Outline the steps in choosing values for coupling capacitors.
- 8.64.** Determine the break frequency for each of the capacitors shown in the common-emitter amplifier of Figure 8.37 with $R_{E1} = 0$, $\beta = 225$, and $I_{CQ} \cong 10$ mA. In finding the break frequency for a given capacitor, assume that each of the other capacitors behaves as a short circuit. Estimate the lower 3-dB frequency. Check by using a SPICE simulation.
- 8.65.** Consider the cascode amplifier shown in Figure 8.40. Assume that $\beta = 225$, $R_C = R_L = R_E = 510$ Ω, $R_2 = 10$ kΩ, $R_1 = 6.8$ kΩ, $I_{CQ} = 10$ mA, $V_{CC} = 15$ V, and $-V_{EE} = -15$ V. Determine the capacitance values required so that each capacitor has a break frequency of 10 Hz. In finding the break frequency for a given capacitor, assume that each of the other capacitors behaves as a short circuit. Estimate the lower 3-dB frequency. Check by using a SPICE simulation.
- 8.66.** Consider the emitter-coupled differential pair displayed in Figure 8.41. Assume that $\beta = 225$, $R_s = 50$ Ω, $R_C = R_L = 510$ Ω, $R_B = 10$ kΩ, $R_{E1} = R_{E2} = 1.3$ kΩ, $I_{CQ1} = I_{CQ2} \cong 10$ mA, $V_{CC} = 15$ V, and $-V_{EE} = -15$ V. Determine the capacitance values required so that each capacitance has a break frequency of 10 Hz. In finding the break frequency for a given capacitor, assume that each of the other capacitors behaves as a short circuit. Estimate the lower 3-dB frequency. Check by using a SPICE simulation.
- 8.67.** Determine the break frequency for each of the capacitors shown in the emitter follower of Figure 8.45. The transistor has $\beta = 225$ and $I_{CQ} \cong 10$ mA. In finding the break frequency for a given capacitor, assume that each of the other capacitors behaves as a short circuit. Estimate the lower 3-dB frequency. Check by using a SPICE simulation.

Appendix A

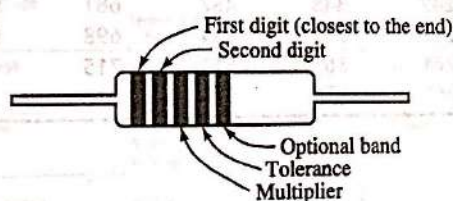
DISCRETE RESISTORS

Several types of resistors are available for use in electronic circuits. Carbon-composition resistors with tolerances of 5%, 10%, or 20% are available with various power ratings (such as 1/8, 1/4, and 1/2 watt). These resistors are used in noncritical applications such as biasing.

Metal-film 1%-tolerance resistors are used where greater precision is required. For example, we often choose metal-film resistors in applications such as the feedback resistors of an op amp or as the frequency-determining elements of an oscillator.

Wire-wound resistors are available with high power-dissipation ratings. Wire-wound resistors often have significant series inductance because they consist of resistance wire which is wound on a form, such as ceramic. Thus, they are not suitable for use as a resistance at high frequencies.

The value and tolerance are marked on 5%-, 10%-, and 20%-tolerance resistors by color bands, as shown in Figure A.1. The first band is closest to one end of the resistor. The first and second bands give the significant digits of the resistance value. The third band gives the exponent of the multiplier. The fourth band indicates the tolerance. The fifth band is optional and indicates whether the resistor meets certain military reliability specifications.



Digit	Color	Tolerance	Color
0	Black	2%	Red
1	Brown	5%	Gold
2	Red	10%	Silver
3	Orange	20%	No fourth band
4	Yellow		
5	Green		
6	Blue		
7	Violet		
8	Gray		
9	White		

Examples		
Yellow	Violet	Black = $47 \times 10^0 = 47 \Omega$
Yellow	Violet	Red = $47 \times 10^2 = 4700 \Omega$
Brown	Black	Yellow = $10 \times 10^4 = 100 \text{ k}\Omega$

Figure A.1

Table A.1 shows the combinations of significant figures available as nominal values for 5%-, 10%-, and 20%-tolerance resistors. Table A.2 shows the standard nominal significant digits for 1%-tolerance resistors.

Table A.1. Standard 5%-tolerance resistors.^a

10	16	27	43	68
11	18	30	47	75
12	20	33	51	82
13	22	36	56	91
15	24	39	62	

^a Resistors having tolerances of 10% and 20% are available only for the values given in boldface.

Table A.2. Standard values for 1%-tolerance metal-film resistors.

100	140	196	274	383	536	750
102	143	200	280	392	549	768
105	147	205	287	402	562	787
107	150	210	294	412	576	806
110	154	215	301	422	590	825
113	158	221	309	432	604	845
115	162	226	316	442	619	866
118	165	232	324	453	634	887
121	169	237	332	464	649	909
124	174	243	340	475	665	931
127	178	249	348	487	681	953
130	182	255	357	499	698	976
133	187	261	365	511	715	
137	191	267	374	523	732	

Appendix B

Data Sheet for the 2N2222A BJT. (Copyright of Motorola, Inc. Used by permission.)

MAXIMUM RATINGS

Rating	Symbol	2N2218 2N2222	2N2218A 2N2219A 2N2222A	Unit
Collector-Emitter Voltage	V_{CE}	30	40	Vdc
Collector-Base Voltage	V_{CB}	60	75	Vdc
Emitter-Base Voltage	V_{EB}	5.0	5.0	Vdc
Collector Current — Continuous	I_C	800	800	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	0.8 4.57	0.4 2.28	Watt mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	3.0 17.1	1.2 6.86	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N2218A 2N2219A	2N2222A	Unit
Thermal Resistance, Junction to Ambient	R_{JA}	219	146.8	°C/W
Thermal Resistance, Junction to Case	R_{JC}	58	437.5	°C/W

2N2218A, 2N2219A, A* 2N2222A, A*

2N2218, A/2N2219, A
CASE 79-04
TO-18 (TO-205AD)
STYLE 1



A/2N2222A
CASE 22-03
TO-18 (TO-206AA)
STYLE 1

GENERAL PURPOSE
TRANSISTORS
NPN SILICON

*2N2218A and 2N2222A
are Motorola designated
preferred devices.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 10 \text{ mAdc}, I_E = 0$)	$V_{(BR)CE}$	30 40	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A}, I_E = 0$)	$V_{(BR)CB}$	60 75	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}, I_C = 0$)	$V_{(BR)EB}$	5.0 5.0	—	Vdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}, V_{EB}(\text{off}) = 3.0 \text{ Vdc}$)	I_{CEX}	—	10	nA
Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}, I_E = 0$)	I_{CB}	—	0.01 0.01 10 10	μA
Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}, I_E = 0, T_A = 150^\circ\text{C}$)	I_{CB}	—	10	nA
Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}, I_E = 0, T_A = 150^\circ\text{C}$)	I_{CB}	—	10	nA
Emitter Cutoff Current ($V_{EB} = 3.0 \text{ Vdc}, I_C = 0$)	I_{EB}	—	10	nA
Base Cutoff Current ($V_{CE} = 60 \text{ Vdc}, V_{EB}(\text{off}) = 3.0 \text{ Vdc}$)	I_{BL}	—	20	nA
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.1 \text{ mA}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	20 35	—	—
($I_C = 1.0 \text{ mA}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	25 50	—	—
($I_C = 10 \text{ mA}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	35 75	—	—
($I_C = 10 \text{ mA}, V_{CE} = 10 \text{ Vdc}, T_A = -55^\circ\text{C}$)	h_{FE}	15 35	—	—
($I_C = 150 \text{ mA}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	40 100	120 300	—

MOTOROLA SMALL-SIGNAL TRANSISTORS, FETs AND DIODES

2N2218A/18/19A/22/22A

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Electrical Characteristics (continued)		Symbol	Min	Max	Unit
$I_C = 150 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$ (1)	2N2218A		20	—	
	2N2219A, 2N2222A		50	—	
$I_C = 500 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$ (1)	2N2219, 2N2222		30	—	
	2N2218A		25	—	
	2N2218A, 2N2222A		40	—	
Collector-Emitter Saturation Voltage(1) $I_C = 150 \text{ mAdc}$, $I_B = 15 \text{ mAdc}$	Non-A Suffix	$V_{CE(sat)}$	—	0.4	V_{dc}
	A-Suffix		—	0.3	
$I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$	Non-A Suffix		—	1.6	
	A-Suffix		—	1.0	
Base-Emitter Saturation Voltage(1) $I_C = 150 \text{ mAdc}$, $I_B = 15 \text{ mAdc}$	Non-A Suffix	$V_{BE(sat)}$	0.8	1.3	V_{dc}
	A-Suffix		0.6	1.2	
$I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$	Non-A Suffix		—	2.6	
	A-Suffix		—	2.0	

SMALL-SIGNAL CHARACTERISTICS

SMALL-SIGNAL CHARACTERISTICS		r_T	280 300	—	MHz
Current Gain — Bandwidth Product(2) ($I_C = 20$ mAdc, $V_{CE} = 20$ Vdc, $f = 100$ MHz)	All Types, Except 2N2219A, 2N2222A				
Output Capacitance(3) ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 1.0$ MHz)		C_{ob}	—	8.0	pF
Input Capacitance(3) ($V_{EB} = 0.5$ Vdc, $I_C = 0$, $f = 1.0$ MHz)	Non-A Suffix A-Suffix		— —	30 25	pF
Input Impedance ($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A	h_{ie}	1.0 2.0	3.5 8.0	kohms
($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A		0.2 0.25	1.0 1.25	
Voltage Feedback Ratio ($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A	h_{re}	— —	5.0 8.0	$\times 10^{-4}$
($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A		— —	2.5 4.0	
Small-Signal Current Gain ($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A	h_{fe}	30 50	150 300	—
($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A		50 75	300 375	
Output Admittance ($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A	h_{oe}	3.0 5.0	15 35	μ mhos
($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	2N2218A 2N2219A, 2N2222A		10 15	100 200	
Collector Base Time Constant ($I_E = 20$ mAdc, $V_{CB} = 20$ Vdc, $f = 31.8$ MHz)	A-Suffix	rb^*C_C	—	150	ps
Noise Figure ($I_C = 100$ μ A, $V_{CE} = 10$ Vdc, $R_g = 1.0$ kohm, $f = 1.0$ kHz)	2N2222A	NF	—	4.0	dB
Real Part of Common-Emitter High Frequency Input Impedance ($I_C = 20$ mAdc, $V_{CE} = 20$ Vdc, $f = 300$ MHz)	2N2218A, 2N2219A 2N2222A	$Re(h_{ie})$	—	80	ohms

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

(3) 2N5581 and 2N5582 are Limited C_{cb} and C_{cb} for these conditions and values.

MOTOROLA SMALL-SIGNAL TRANSISTORS, FETs AND DIODES

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